A Ultra-Low-Voltage LC-VCO with a Frequency Extension Circuit for Future 0.5-V Clock Generation

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Challenging for Clock Generator

<table>
<thead>
<tr>
<th>Year</th>
<th>CMOS</th>
<th>$V_{DD}$</th>
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<tbody>
<tr>
<td>2000</td>
<td>0.35,\mu m</td>
<td>3.3-V</td>
</tr>
<tr>
<td>2010</td>
<td>40nm</td>
<td>1.0-V</td>
</tr>
<tr>
<td>2024</td>
<td>8nm</td>
<td>0.5-V</td>
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</table>

Under low supply voltage

- **LC-VCO based**
  - Small jitter
  - Narrow tuning range

- **Ring oscillator based**
  - Large jitter
  - Wide tuning range
Proposed Architecture

CORE-VCO

Switchable
/2 OR /3 Div.

The First Divider

The Second Divider Chain

Freq (GHz)

BY- 3
BY- 2

0.05 to 3.2 GHz Band I

4.1 to 6.4 GHz Band II

f₀

f₀/N

f₀/N

f₀/2N

f₀/4N

f₀/64N
# Comparison of Low-voltage VCOs

<table>
<thead>
<tr>
<th>-</th>
<th>Unit</th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>This work</th>
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<tbody>
<tr>
<td>Topology</td>
<td>-</td>
<td>LC</td>
<td>LC</td>
<td>Ring</td>
<td>LC + Divider</td>
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<tr>
<td>( P_{\text{DC}} )</td>
<td>mW</td>
<td>3.0</td>
<td>0.365</td>
<td>1.157</td>
<td>0.75~1.0</td>
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<tr>
<td>Jitter</td>
<td>ps</td>
<td>&lt;1</td>
<td>&lt;1</td>
<td>&gt;15</td>
<td>&lt;1</td>
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<tr>
<td>Tuning Range</td>
<td>%</td>
<td>8.1</td>
<td>20</td>
<td>176</td>
<td>194</td>
</tr>
</tbody>
</table>

Conclusion

• The necessity of LC VCO for ultra-low-voltage clock generation is investigated in depth.

• A 0.5-V, 0.05-to-3.2 GHz, 4.1-to-6.4 GHz, LC-VCO for sub-picosecond-jitter clock generation is realized.