A 32Gbps Low Propagation Delay 4x4 Switch IC for Feedback-Based System in 0.13 μm CMOS Technology

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Network Router/Switch

- A router/switch is a network element with multiple input ports and output ports.
- $N \times N$ switch: $N$ input ports and $N$ output ports
- Basic functions:
  - table lookup
  - message copying

![Diagram of a network router/switch]

- Input ports: 1, 2, 3, 4
- Output ports: 1, 2, 3, 4

- $4 \times 4$ switch
- Local host, Server, Router, Internet
- HTTP, TCP, IP, Ether
Output Switch and Input Switch

- **Output-buffered switch:**
  - Feature: common shared memory, speedup of $N$ requirement
  - Problem: memory access limitation
  - Solution: parallel-buffered switch

- **Input-buffered switch:**
  - Feature: one buffer per input port
  - Problem: head-of-line blocking, 58% throughput
  - Solution: VOQ (virtual output queuing) technique

\[
\text{Memory} \\
\begin{array}{c}
\text{IN} \\
\text{Data Rate R} \\
\text{N users} \\
\text{OUT}
\end{array}
\]

\[
2 \cdot N \cdot R
\]
Load balanced Birkhoff-von Neumann Switch Architecture

- **Features:**
  - 100% throughput
  - scalability: $O(1)$, periodic, deterministic
  - lower average delay in heavy or burst traffic
  - better buffer utilization
  - lower hardware complexity

- **Problem:** out-of-sequence issue
Feedback-based System

Symmetric TDM Patterns

Motivation: switching packet directly in RF domain

• Low propagation delay in feedback system
Proposed Low Propagation Delay 4x4 Switch Architecture and Measurement Results

Overall Architecture

Pattern Generator

2x2 Switch

2x2 Switch

Pattern Generator

Divider N=2

Phase Sifter

Output Buffer

Die Photo

One of the Output Waveform

Measurement Eye Diagrams:

Jitter_{p-p} = 20ps @8Gbps.