A 65 nm Flip-Flop Array to Measure Soft Error Resiliency against High-Energy Neutron and Alpha Particle

- Process scaling makes LSI less reliable to soft errors
- Soft errors are caused by a particle hit
  - Flips stored value on a Flip-Flop (SEU)
  - Generates temporal pulse on a logic gate (SET)

#1D-6
Fabricate two FF Arrays in a 65nm process

1. Soft error hardened FFs to compare soft error rates
2. Standard FF to measure SEU and MCU rates

#1D-6
Conventional Soft Error Hardened FF

- Conventional DMR (BISER) is weak to SET on C-element
  - Two slave latches capture the SET pulse
Proposed Soft Error Hardened FF

- C-elements are duplicated, and weak keepers are cross-coupled
  - An SET from C-element cannot propagate into both slave latches

![Proposed Soft Error Hardened FF Diagram]

- BCDMR

![Soft Error Rate vs Clock Frequency Graph]

- BCDMR

Clock Frequency

Soft Error Rate

DMR

BCDMR

#1D-6
The BCDMR is better than DMR

- 150x better than conventional DMR at 160MHz
- DMR is weak to SET pulse on C-element

Standard FF = 700,000
Conclusion

- Propose a soft error hardened FF
  - Based on DMR (BISER)

- Measured Soft Error Rates by alpha particles
  - 150x better soft error resilience than DMR at 160MHz
  - DMR has lower error resilience at 160MHz

- Measure MCUs on standard FF by neutron
  - MCU rate depends on distance from tap-cell