Geyser-2: The Second Prototype CPU with Fine-grained Run-time Power Gating

Z.Lei, D.Ikebuchi, Y.Saito, M.Kamata, N.Seki, Y.Kojima, H.Amano (Keio Univ.)
S.Koyama, T.Hashida, Y.Umahashi, H.Masuda, K.Usami (Shibaura Inst. of Tech.)
K.Kmura, M.Namiki (Tokyo Univ. of Agriculture and Technology)
M.Kondo (The Univ. of Electro-Communication)
S.Takeda, H.Nakamura (Univ. of Tokyo)
Background: Geyser Project

- Aims to establish cross-over techniques for low leakage processor design with integration of architecture, circuits and system software (supported by JST-CREST)

- **Geyser-1**

  - 5-stage standard MIPS R3000 pipeline
  - 4 functional units are implemented with fine-grained run-time PG
  - Off-chip caches/TLB
  - 3% ~ 28% leakage saving with benchmark programs
  - 10% area overheads
  - 60MHz maximum clock frequency
Fine-grained Run-time PG on Functional Units

- A function unit stays in the active mode only when being used.
- The pre-decoder in IF stage creates the wake-up signal.
- After the operation, the unit will be turned to sleep automatically.

MIPS R3000 pipeline
Geyser-2 Structure

- **R3000 Core**
- **Inst. Cache (8KB, 2Way)**
- **Data Cache (8KB, 2Way)**
- **TLB**
- **MMU**
- **FPGA**
- **SDRAM**
- **ALU**
  - **CLU**
  - **Shifter**
  - **Mult**
  - **Div**
- **Sleep Controller**
- **IO, etc**
- **Board**

Clock Rates:
- 210MHz
- 105MHz
Geyser-2 Layout

Pin-limited design and only half of die area is utilized
Highlights

• Max clock frequency: 210MHz
  – The wakeup latency of all four functional units is less 5ns
• Break Even Time aware leakage control mechanisms:
  – Cooperate with compiler and OS
  – Different leakage control policy at different temperature
• Leakage saving of the processor core: > 60%
  – When all functional units are power-gated
• Area overheads with PG: < 15%
• Leakage saving with benchmark programs is on the way

Please come to the poster