An Implementation of an Asynchronous FPGA Based on LEDR/Four-Phase-Dual-Rail Hybrid Architecture

Yoshiya Komatsu
Shota Ishihara
Masanori Hariyama
Michitaka Kameyama

Graduate School of Information Sciences
Tohoku University
Background

Reconfigurable VLSIs: FPGA, etc.

Users can program the function on FPGAs without fabrication but FPGAs have a complex structure to achieve programmability.

Advantages
- Low cost for small volume products
- Short time-to-market

Disadvantage
- Larger power consumption than ASICs about 10 times
Advantages of Asynchronous FPGAs

Handshake protocol for data transfer

Advantages:

- Low power consumption
  - No dynamic power in inactive circuits
- Less emission of electro-magnetic interference (EMI)
  - PEs tend to operate at random points in time
- Robustness
  - Automatically adaptive to delay variations
LED/Four-Phase-Dual-Rail Hybrid Architecture

Four-Phase-Dual-Rail encoding:
- Small areas for function unit

LED encoding:
- High throughput, low power for data transfer
Evaluation

Process: 65nm CMOS
Delay time: 1.15ns (1cell)
Equivalent to 870MHz synchronous FPGA

Compared to
- 4-phase-dual-rail-based FPGA
  - Throughput: 51% up
  - Energy: 8% down

- LEDR-based FPGA
  - Transistor count: 47% down

- Synchronous FPGA
  - Power: 53% down
    (Workload: 10%)