Selectively Patterned Masks: Structured ASIC with Asymptotically ASIC Performance

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Introduction

Selectively patterned masks (SPM)
  - Concept
  - Pattern transfer process
  - Analysis: mask cost, throughput

Structured ASIC using SPM
  - Tile design
  - Logic synthesis
  - Routing architecture

Experimental results

Conclusion
ASIC Has Been Slowed Down

- New design starts decrease
- Global alliance of foundries emerges
- Increasing mask cost is one of reasons

![Graph showing trends in ASIC design costs](image)

<table>
<thead>
<tr>
<th>Process (μ)</th>
<th>2.0</th>
<th>0.8</th>
<th>0.6</th>
<th>0.36</th>
<th>0.25</th>
<th>0.18</th>
<th>0.13</th>
<th>0.10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single Mask cost ($K)</td>
<td>1.5</td>
<td>1.5</td>
<td>2.5</td>
<td>4.5</td>
<td>7.5</td>
<td>12</td>
<td>40</td>
<td>60</td>
</tr>
<tr>
<td># of Masks</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>16</td>
<td>20</td>
<td>26</td>
<td>30</td>
<td>34</td>
</tr>
<tr>
<td>Mask Set cost ($K)</td>
<td>18</td>
<td>18</td>
<td>30</td>
<td>72</td>
<td>150</td>
<td>312</td>
<td>1,000</td>
<td>2,000</td>
</tr>
</tbody>
</table>

EETimes, 2002
Structured ASIC

- Programmable device: a solution for mask cost

- Structured ASIC
  - Gate array has evolved into structured ASIC
  - Makes only contact/via masks for programming
    ↔ all metal and via masks in gate array

[N. Shenoy, DAC 2004]

- 2 MUX tree, 2 local inverters
- A F/F with set/reset/enable/scan

Prefabricated IO  processor core

RAM cores
Structured ASIC

- Introduced in 1999
- Big success was expected
- Many companies jumped in the business in early 2000
- Not very successful
  - Not competitive to ASIC (area: 3 ~ 7 times, delay: 2 ~ 6 times)

![Gartner Dataquest, 2006](image)

5/23
Structured ASIC

- Current SA: only one type of “tile”
  - Tile must be designed to implement any logic: too much redundancy

- Is it possible to have multiple tiles?
  - Different designs would need different mix of tiles
    → Have to make ALL masks!
Selectively Patterned Masks (SPM)

- Tile masks: homogeneous just like SA, but more than one tiles
- **Masking masks**: used to selectively pattern tiles
Selectively Patterned Masks (SPM)

- How to selectively pattern? Method I: tile and masking masks together during lithography

- But, practical limitation...
  - Current lithography equipment does not support
  - Light through two masks become weaker
Selectively Patterned Masks (SPM)

- Method II: **double exposure**
Mask Design in Double Exposure

- **Boundary margin** to accommodate
  - Light diffraction
  - Mask misalignment

\[
x \geq y - 5, \quad x + y - 5 \geq 80
\]

\[
x \geq y + 5, \quad x + y + 5 \geq 80
\]
Structured ASIC Using SPM

- **Mask sets, metal masks**: pre-fabricated
- **Contact/via masks**: fabricated for each design, used to program tiles & make connection
- **Masking masks**: fabricated for each design, but cheap

![Mask sets, Metal masks, Masking masks, Contact/via masks, Design diagram]
Analysis of Mask Cost

- Cost model is similar to that of standard SA

<table>
<thead>
<tr>
<th></th>
<th>Pre-fabricated</th>
<th>Newly fabricated</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASIC</td>
<td>All masks</td>
<td></td>
</tr>
<tr>
<td>Standard SA</td>
<td>One tile mask set</td>
<td>Contact &amp; via masks</td>
</tr>
<tr>
<td>SA with SPM</td>
<td>Multiple tile mask sets</td>
<td>Contact &amp; via masks + Masking masks</td>
</tr>
</tbody>
</table>

Mask costs [M$] vs # of designs

12/23
Analysis of Manufacturing Throughput

- Use of masking masks and multiple tiles increase manufacturing time

<table>
<thead>
<tr>
<th></th>
<th>Exposure</th>
<th>Etching</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard patterning</td>
<td>One time</td>
<td>One time</td>
</tr>
<tr>
<td>Selective patterning</td>
<td># of tiles × 2</td>
<td># of tiles</td>
</tr>
</tbody>
</table>

33% of degradation
Structured ASIC Using SPM

RTL

Logic synthesis

Gate library

Tile design

Packing

Initial placement

T₂ packing

T₁ packing

Placement

Routing
**Tile Design**

- Three tile architectures
  - $T_1$: three basic logic gates
  - $T_2$: two complex gates
  - $T_3$: F/F (with set/reset)
Logic Synthesis

- **Gate library**: models each “gate” (NOT tile)
- **Logic synthesis**
  1. Initial netlist is made such that each gate occupies one tile
Logic Synthesis

2. Initial placement
3. Locate T2 \(\rightarrow\) merge with nearest T1
Logic Synthesis

4. Merge adjacent “three” $T_1$s $\leftrightarrow$ scan tiles from bottom-left to upper-right of placement
Routing Architecture

- **A grid** (made of M3+M4) is placed on top of each tile (two grids for T3)
- Programmable via is used for inter-tile connection
Experimental Results

• Area-optimized design
  – SPM/ASIC = 2 ↔ 3 ~ 7 in conventional SA
  – Why area increases? → tile height & tile utilization
Experimental Results

- Delay-optimized design
  - SPM/ASIC = 1.2 ↔ 2 ~ 4 in conventional SA
  - Why delay increases? → lack of gates & routing arch.

![Graph showing delay comparison between ASIC and SPM](image-url)
Experimental Results

• Design space (area vs. delay curve)
  – Delay opt.  →  SPM/ASIC = 1.26 (delay), 1.69 (area)
  – Area opt.  →  SPM/ASIC = 0.9 (delay), 2.1 (area)
  – Why large gap occur?  →  lack of gates & tile regularity
Conclusion

• Current structured ASIC (SA)
  – Performance limited due to “regularity”

• SPM
  – Allows “irregular” structured ASIC with similar mask cost as SA
  – Prototype SA using SPM was demonstrated

• Future works
  – Logic synthesis
  – Routing algorithm