A Resilient Router Design Through Data Path Salvaging

Cheng Liu, Lei Zhang, Yinhe Han, Xiaowei Li
Key Lab of Computer System and Architecture
Institute of Computing Technology
Chinese Academy of Sciences
Outline

- Background
- Motivation
- Resilient NoC Design
- Experiments
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Reliability Challenge

- Technique keeps on scaling down.
- The chip is getting larger.
- Applications require more powerful chip.

There are more transistors on a single chip.

Manufacture defect increases. Wear-out appears frequently.
NoC Reliability Influence on a SoC
Related work

- Vicis: A Reliable Network for Unreliable Silicon [Fick09]
  - Port swapping, ECC, fault tolerance routing algorithm
- A Lightweight Fault-Tolerant Mechanism for Network-on-Chip [Koibuchi 08]
  - Default bypass backup
- Bulletproof: A defect-tolerant CMP switch architecture [Constantinides 06]
  - Redundancy and share
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Conventional Router Architecture
Fault rate $p$, Component area $A$

$A \rightarrow p$

$2A \rightarrow 1-(1-p)^2 \approx 1-(1-2p)=2p$

$nA \rightarrow 1-(1-p)^n \approx 1-(1-np)=np$
Data Path Slice Reuse
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Resilient NoC Design Scheme

<table>
<thead>
<tr>
<th>Module</th>
<th>RC</th>
<th>PR</th>
<th>Arbiter</th>
<th>CR</th>
<th>Buffer</th>
<th>Link</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>Small</td>
<td>Medium</td>
<td>Small</td>
<td><strong>Medium</strong></td>
<td>Large</td>
<td>Large</td>
</tr>
<tr>
<td>Method</td>
<td>Redundancy</td>
<td>ECC</td>
<td>Redundancy</td>
<td><strong>Slice Reuse</strong></td>
<td>Slice Reuse</td>
<td>Slice Reuse</td>
</tr>
</tbody>
</table>
Slice Reuse Principle
Slice Reuse Structure
Intermittent Transmission
Slice Pipeline Transmission
Slice Reuse

Data transmission direction

Intermittent Transmission  Slice pipeline transmission

Pipeline slices are correlated: n1 >= n2 >= n3
The correlations are limited: n0>n1, n0=n1, n0<n1
The correlations are dynamic regarding to different pipelines
Extension to Virtual Channel Router

The diagram illustrates a router with three virtual channels (VC1, VC2, VC3) connected through a multiplexer (MUX) and a demultiplexer (DEMUX). The configure vector (CR) is shown at the input, controlling the allocation of packets to the virtual channels. The output is directed through the configured virtual channels to efficiently handle data traffic.
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Design Choice (slice granularity)
Design Choice (redundancy granularity)
Design Choice (redundancy scale)

![3D graph showing the relationship between fault rate, logic block area, and functional probability, with different redundancy levels (No Protection, 1:1 Redundancy, 2:1 Redundancy).]
Area Overhead

![Area Overhead Chart]
Reliability
Reliability

![Graph showing reliability over fault number]

- Functional Rate
- Fault Number
- Points along the graph show the decreasing reliability with increasing fault number.
Performance

![Graph showing average latency against injection rate for different fault types: Fault 0, Buffer Fault 48, Buffer Fault 24, Buffer Fault 12, Buffer Fault 6, Link Fault 48, Link Fault 24, Link Fault 12, Link Fault 6. The x-axis represents injection rate (flits/node/cycle) ranging from 0.05 to 0.4, and the y-axis represents average latency (cycles) ranging from 0 to 200. Different colors and markers are used to distinguish between fault types.](image-url)
Questions?
Thanks!