A Self-Testing and Calibration Method for Embedded Successive Approximation Register ADC

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Outline

- *Introduction*
- Preliminaries
- The proposed Technique
- Simulation Results
- Conclusion
The successive approximation register (SAR) ADC is widely used in modern mixed-signal SOC designs

- High power efficiency and low area overhead
- Component mismatch limits its performance

ADC testing in SOC design is difficult

- Requires high quality test stimulus
- Lengthy testing
- I/O accessibility is limited
Previous Works

- **Testing [Goyal, ITC 2005]**
  - Selective code testing to reduce test time
  - Incapable of handling missing code issue
  - The required test ramp is impractical for on-chip generation

- **Calibration [Liu, ISSCC 2009]**
  - Employs a slow but accurate reference ADC and LMS technique to perform background calibration
  - The reference ADC usually incurs significant area overhead
  - The LMS algorithm demands intensive computation and lengthy calibration time
The Proposed Technique

- This paper presents a self-testing and calibration technique for embedded SAR ADC
  - Test the SAR ADC by measuring the major carrier transitions (MCTs) of its DAC capacitor array
  - Calibrate the SAR ADC by eliminating all the missing codes digitally

- The MCTs of the DAC capacitor array are directly generated and measured by
  - The comparator in the SAR ADC
  - An additional DfT DAC (d-DAC)
The Advantages and Contributions

- The ideal MCT voltage is just 1 LSB
  - The required analog measurement range is small
  - Simplifies the d-DAC implementation

- The control signals and test responses are all-digital
  - One can reuse the on-chip digital resources for test result analysis and missing code calibration
  - This further reduces the incurred design and area overhead
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Basic SAR ADC Structure

- The SAR ADC is consisted of
  - Binary-weighted DAC capacitor array
  - Comparator
  - SAR Control logic

\[ C_i = 2^i \cdot C_0 \]
\[ C_r = C_0 \]
Conversion 1: Sample Mode

- Sample the input voltage into the capacitors
Conversion 2: Hold Mode

- $S_g$ open, and all the top plates are connected to ground

$$V_X = -V_{in}$$
Conversion 3: Redistribution Mode (1/2)

- Iterative binary search process (from MSB to LSB)
- First, the top plate of $C_3$ is connected to $V_{ref}$

$$V_x = -V_{in} + \frac{C_3}{C_{total}} V_{ref} = -V_{in} + \frac{1}{2} V_{ref}$$
Conversion 3: Redistribution Mode (2/2)

- $V_x$ is then compared to ground
  - $V_x > 0$, $D_3=0$ and the top plate of $C_3$ will reconnect to ground
  - $V_x < 0$, $D_3=1$

- After $D_3$ is resolved, the process moves down to next bit.
  - $N$ iterations is required for $N$-bit ADC

- Let $C_H(i)$ denote the capacitance connected to $V_{ref}$,
  - $V_x$ in $i$-th iteration can be expressed as
    \[
    V_x = -V_{in} + \frac{C_H(i)}{C_{total}} V_{ref}
    \]
DAC MCT Testing (1/3)

- SAR ADC linearity can be characterized by measuring the major carrier transitions (MCTs) of the DAC.

- The code transition level \( V_T \) of \( D_{N-1} \cdots D_1 D_0 \):

\[
V_T (D_{N-1} \cdots D_1 D_0) = \frac{\sum_{i=0}^{N-1} D_i \cdot C_i}{C_{total}} \cdot V_{ref}
\]

- For the ADC code in the form of \( 2^i - 1 \), the code width is:

\[
V_{CW}(2^i - 1) = V_T (2^i) - V_T (2^i - 1) = \frac{C_i - \sum_{j=0}^{i-1} C_j}{C_{total}} \cdot V_{ref}
\]
All the code widths can be expressed by $V_{cw}(2^i - 1)$

$V_{cw}(2^i - 1)$ is also known as the major carrier transition of the DAC

Many code transitions share the same capacitor switching activities
# DAC MCT Testing (3/3)

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**S1**

- 0000: 0
- 0001: 1
- 0010: 2
- 0011: 3
- 0100: 4
- 0101: 5
- 0110: 6
- 0111: 7
- 1000: 8
- 1001: 9
- 1010: 10
- 1011: 11
- 1100: 12
- 1101: 13
- 1110: 14
- 1111: 15

**S2**

- 0000: 0
- 0001: 1
- 0010: 2
- 0011: 3
- 0100: 4
- 0101: 5
- 0110: 6
- 0111: 7
- 1000: 8
- 1001: 9
- 1010: 10
- 1011: 11
- 1100: 12
- 1101: 13
- 1110: 14
- 1111: 15

**S3**

- 0000: 0
- 0001: 1
- 0010: 2
- 0011: 3
- 0100: 4
- 0101: 5
- 0110: 6
- 0111: 7
- 1000: 8
- 1001: 9
- 1010: 10
- 1011: 11
- 1100: 12
- 1101: 13
- 1110: 14
- 1111: 15
Errors in SAR ADC

- Comparator offset
  - Causes global shift to the transfer curve
  - Can be compensated by auto-zeroing techniques

- Capacitor mismatch
  - Affect the code width

\[ V_{CW} (2^i - 1) = \frac{C_i - \sum_{j=0}^{i-1} C_j}{C_{total}} \cdot V_{ref} \]
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The Proposed DfT Architecture
MCT Generation

- The SAR ADC linearity can be derived by measuring the DAC MCTs

- The most straightforward way is to use a precise ramp to stimulate the ADC and observe the output codes
  - Long conversion time (N+2 cycles for each AD conversion)

- Here, we directly control the DAC to generate the MCTs for measurement
  - Only three cycles for each MCT generation
Connect the top plates of LSB capacitors to $V_{ref}$.
S\(_g\) open, and all the top plates are connected to ground

\[ V_X = -V_T(0111) = -\frac{\sum_{j=0}^{2} C_j}{C_{total}} \cdot V_{ref} \]
The top plate of $C_3$ is connected to $V_{\text{ref}}$

\[ V_x = V_{cw}(0111) = V_T(1000) - V_T(0111) = \frac{C_3 - \sum_{j=0}^{2} C_j}{C_{\text{total}}} \cdot V_{\text{ref}} \]
MCT Characterization

- MCTs are measured by a short linear ramp together with the internal comparator
  - The test ramp is generated by d-DAC
  - FSR is 4 LSBs of the ADC
  - The resolution is 6-bit
The Testing Flow

Start

Comparator Offset Measurement

Next bit $i$ ?

Set $m_i=0$

Force the DAC capacitor array to generate $V_T(2^i) - V_T(2^i-1-m_i)$

$V_T(2^i) < V_T(2^i-1-m_i)$ ?

Measure $V_{CW}(2^i-1-m_i)$ and record $m_i$

$V_T(2^i) < V_T(2^i-1-m_i)$ ?

$m_i=m_i+1$

Construct the ADC I/O transfer curve

Quantization error removal

DNL/INL Analysis

End

No

Yes

No

Yes

Comparer Offset Measurement

DNL/INL Analysis

End
Quantization Error Removal

- Calculate the difference between the actual ADC FSR and its ideal value, and linearly scale back this difference to all the existing codes

\[ \delta = \frac{FSR_{est} - FSR_{ideal}}{n_{code}} \]

\[ V_{CW}(i)' = V_{CW}(i) - \delta, \text{ if } V_{CW}(i) \neq 0 \]
Compensation codes are computed according to $m_i$’s.

The calibrated code is obtained by subtracting the compensation code from the raw code.

$$C_{cmp} = \begin{cases} 
m_{N-1} + 2m_{N-2}, & \text{if } D_{n-1}D_{n-2} = 11 
m_{N-1} + m_{N-2}, & \text{if } D_{n-1}D_{n-2} = 10 
m_{N-2}, & \text{if } D_{n-1}D_{n-2} = 01 
0, & \text{if } D_{n-1}D_{n-2} = 00 
\end{cases}$$
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Simulation Setup

- 10-bit SAR ADC with conversion radix set to 1.95
  - Capacitor mismatch is set within 5%
  - Comparator offset is set within 1 LSB

- A 6-bit DAC is designed for test stimulus generation
  - The FSR is only 4 LSBs of the ADC
  - 2 LSBs for analog measurement and 2 LSBs for offset tolerance

- Noise on the signal path is Gaussian with 0.1 LSB standard deviation
Testing Results

- Histogram testing results
  - Noise free
  - Average code hit is 16
  - The required test cycles is about 160K
  - DNL/INL: -1/-16.53 LSB

- The proposed technique
  - Gaussian noise with 0.1 LSB standard deviation
  - Each MCT is sampled 10 times
  - The required test cycles is about 0.5K
  - DNL/INL: -1/-16.53 LSB

Test errors are all less than 0.1 LSB
Calibration Results

- **Before Calibration**
  - DNL/INL: -1/-16.53 LSB

- **After Calibration**
  - DNL/INL: -0.42/-0.57 LSB

All of the missing codes are eliminated
Massive Simulation

- The proposed technique is applied to 1000 SAR ADCs
- The DNL/INL test errors are all within 0.1/0.3 LSB
- The average DNL/INL are improved from 1/16.75 LSB to 0.61/0.48 LSB
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This paper presents a simple yet efficient technique for testing and calibrating the embedded SAR ADC.

Simulation results validate the effectiveness and robustness of the proposed technique.

A prototype is currently being designed for further silicon validation.