Design Constraint for Fine Grain Supply Voltage Control LSI

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Atsuki Inoue

Platform Technologies Laboratories
Fujitsu Laboratories Ltd.
Agenda

- Background
  - Fine grain supply voltage control
- Energy gain concept
- Power gating case
  - Various energy losses
  - Results with simple assumption
  - Modification for actual devices
  - Comparison with simulation results
  - Minimum sleep duration time
- DVFS* case (results only)
- Summary

*DVFS: Dynamic Voltage and Frequency Scaling
General expectation for fine grain supply control

Concept of supply voltage control:
- Collaboration between power supply unit and user circuit optimizes energy consumption
- Power gating and DVFS are typical controls.

Two types of grain size
- Grain size in time domain
- Grain size in space domain

General expectation
- Fine grain control will improve power efficiency.

We will discuss the time domain control in this paper.
Fine grain supply control in time domain

More frequent controls are expected to reduce leakage power.

(power gating case)
Energy gain concept to derive design constraint

\[ E_a \]
Dissipated energy when supply voltage control technique is applied.

- Energy for circuit operation itself
- Energy overhead for changing supply voltage

\[ E_{na} \]
Dissipated energy when supply voltage control technique is not applied.

- Energy for circuit operation itself

Energy gain: \( n = \frac{E_{na}}{E_a} > \] necessary condition

Design constraint
Power gating case
Energy losses at power gating

(a) Switching energy of gating transistor
(b) Switching energy of isolation gates
(c) Storing/restoring energy for internal information
(d) Charging/discharging energy of virtual power line

Only (d) is dependent of sleep duration time
(a)-(c) is independent of sleep duration time.
Start with simple assumptions

Start with the following simple assumptions.

1. Leakage current is independent on drain voltage.
2. Consider charging energy of virtual power line only.
   (Other energy losses (a)-(c) are ignored.)

Then we modify the theory excluding these assumptions

![Diagram showing power gating control signal, virtual power supply voltage, and time durations.](image)
Energy losses for charging virtual power line

Energy with power gating: \[ E_a = E_1 + E_2 + E_3 \]
Energy without power gating: \[ E_{na} = I_{off} V_{dd} \tau = I_{off} V_{dd} (\tau_1 + \tau_2 + \tau_{flat}) \]
Minimum sleep duration time

Case I

Virtual power line voltage

\[ V_{dd} \]

\[ \text{gnd} \]

\[ \tau_1 \quad \tau_2 \]

\[ E_{na} = E_a \]

Case II

Virtual power line voltage

\[ V_{dd} \]

\[ \text{gnd} \]

\[ \tau_1 \quad \tau_{flat} \quad \tau_2 \]

\[ E_{na} > E_a \]

Case III

Virtual power line voltage

\[ V_{dd} \]

\[ \text{gnd} \]

\[ \tau_1 \quad \tau_2 \]

\[ E_{na} < E_a \]

(if other energy losses exist)

Minimum sleep duration time:

\[ \tau_{min}^0 = \frac{C_p V_{dd}}{I_{off} \@ V_{dd}} \]
Leakage current dependence on drain voltage

Actual transistors have DIBL* effects and leakage current does depend on drain voltage.

\[ I_{off}(V_{ds}) = A e^{nv_i} e^{\frac{\lambda V_{ds}}{V_{ds}}} (1 - e^{\frac{V_{ds}}{v_i}}), \quad v_i = \frac{kT}{q} \]

DIBL effect term

We assume

\[ I_{off}(V_{ds}) \propto V_{ds}^\beta \]

\[ \beta = 1 \sim 2 \]

DIBL: Drain Induced Barrier Lowering
$E_{ov}$ : Other energy loss

- Other energy loss $E_{ov}$ is **independent** of sleep duration time.
- (a) & (c) are proportional to decoupling capacitor $C_p$
  - Total load capacitance of power domain $C_L$ is proportional to $C_p$ due to power line noise constraint.
  - Capacitance of gating Tr. $C_x$ is proportional to $C_L$ due to IR drop voltage limitation.
  - Capacitance of storage elements is proportional to total load capacitance $C_L$.
- (b) is small enough to be ignored for usual cases.

We can assume other energy loss $E_{ov}$ is proportional to $C_p$.

$$E_{ov} = z \times C_p V_{dd}^2$$

$z = 20\%$ typical

$z$ : Energy overhead factor
Energy gain diagram for power gating

Including other energy loss and non-constant leakage current effect

Energy with power gating: \( E_a = E_1 + E_2 + E_3 + E_{ov} \)

Energy without power gating: \( E_{na} = I_{off} V_{dd} \tau = I_{off} V_{dd} (\tau_1 + \tau_2 + \tau_{flat}) \)

The modified theory predicts:

- Longer sleep time gives higher energy gain.
  
  When \( \tau \to \infty, \quad n \to \infty \)

- Stronger DIBL effect gives higher gain and shorter minimum sleep duration time.

\[ \tau_{\text{min}} = F_{\text{leak}} \tau_{\text{min}}^0 \]

When \( \beta \) is larger, \( F_{\text{leak}} \) is smaller.

\[ F_{\text{leak}} = 0.56 \sim 0.7 \quad (1 < \beta < 2) \]

(Correction factor)
Comparison with simulation results

Target circuit: 1.1K gates

Technology A
- \( I_{on}/I_{off} = 1.2 \times 10^3 \)
- \( \tau_{min}^0 = 3.24 \mu s \)
- \( \beta \approx 1 \) (weak DIBL)

Technology B
- \( I_{on}/I_{off} = 1.0 \times 10^3 \)
- \( \tau_{min}^0 = 0.26 \mu s \)
- \( 1 < \beta < 2 \) (strong DIBL)

\[ z = 20\% \quad \tau_{min} = F_{leak} \tau_{min}^0 \]
Minimum duration

\[
\tau_{\text{min}}^0 = \frac{C_p V_{dd}}{I_{\text{off}} (V_{dd})}
\]

- Discharging time from \( V_{dd} \) to gnd.
- It does not depend on power domain size.

Design dependent

Technology dependent

\[
\tau_{\text{min}}^0 \approx \left( \frac{C_p}{C_L} \right)_{\text{gate}} \times \left( \frac{I_{\text{on}}}{I_{\text{off}}} \right)_{\text{Tr.}} \times \tau_g
\]

\( \tau_g \): Average gate delay

\( C_p \): Virtual power line cap.

\( C_L \): Average load cap.
Evaluation of $\tau_{\text{min}}^0$ value

\[
\left( \frac{C_p}{C_L} \right)_{\text{gate}} \approx 5
\]

Restriction of supply voltage fluctuation

Ex. Activity factor $\alpha=25\%$, $\Delta V/V_{dd} = 5\%$

\[
\left( \frac{I_{on}}{I_{off}} \right)_{\text{Tr.}} \approx 1 \times 10^7 - 3 \times 10^7 \rightarrow 1 \times 10^5 - 3 \times 10^5
\]

*Low standby power technology 2010-2020

Assume process/temperature coefficient to be 100

$\tau_g \approx 8\, ps - 40\, ps$

*Low standby power technology 2010-2020

\[
\therefore \tau_{\text{min}}^0 \approx 5\, \mu s - 60\, \mu s
\]

Relatively long time constant compared with clock cycle time

* From ITRS roadmap 2009
Minimum sleep cycle number

\[ \tau_0^{\text{min}} \approx \frac{1}{N_g} \left( \frac{C_p}{C_L} \right)_{\text{gate}} \times \left( \frac{I_{\text{on}}}{I_{\text{off}}} \right)_{\text{Tr.}} \times T_{\text{cycle}} \]

\[ N_g : \text{Gate number per one pipeline stage} \]

When

\[ N_g = 18 \quad FO4 \text{ (Power performance optimized design*)} \]

\[ \tau_0^{\text{min}} \approx (3 \sim 8) \times 10^4 T_{\text{cycle}} \]

DVFS case (results only)
Minimum DVFS cycles exist.

\[ N > N_{\text{min}}^0 = \frac{C_p}{\alpha C_L} \]

- \( \alpha \): Activity factor
- \( C_L \): Total load capacitance
- \( C_p \): Total power line capacitance

Simple assumption:
Leakage current is ignored and efficiency of power supply unit is ideal.
Power configuration

\[ N > N_{\text{min}}^0 = \frac{C_p}{\alpha C_L} \]

(a) External power supply
- Larger \( C_p \), Larger \( N_{\text{min}}^0 \)
- Higher efficiency of power supply

(b) On-chip regulator and external power supply
- Smaller \( C_p \), Smaller \( N_{\text{min}}^0 \)
- Lower efficiency of power supply
Energy gain diagram for DVFS

10^3 – 10^5 Cycles are required to obtain energy gain larger than unity.

External power supply

\( C_p / C_L = 5000 \)

External power supply + regulator

\( C_p / C_L = 500 \)

\[ x = \frac{V_{low}}{V_{dd}} = 0.7 \]

\( k = 0.3 \)

\( \eta_d = 0.9 \)

\( \eta_l = 0.8 \)

\( \beta = 2 \)
### Summary

<table>
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<th>Minimum sleep duration</th>
<th>Correction factor</th>
<th>Maximum energy gain</th>
<th>Important design parameters</th>
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<tr>
<td>$\tau_{min}^0 = \frac{C_p V_{dd}}{I_{off}}$</td>
<td>$F_{leak} = 0.56 \sim 0.70$</td>
<td>$n \to \infty$</td>
<td>$\frac{I_{on}}{I_{off}}, \tau_g$</td>
</tr>
</tbody>
</table>
| $N_{min}^0 = \frac{C_p}{\alpha C_L}$ | $F_{leak} = 0.56 \sim 0.86$ | $n \to \frac{x+k}{x(1+k)} \frac{1}{x^2}$ | 1. Power supply configuration $C_p$
|                     | $F_{supply} = 1 \sim \infty$ | , when $N \to \infty$ | 2. Efficiency $\eta_{d,l}$ |
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