Post-Routing Layer Assignment for Double Patterning

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Outline

1. Single Layer Double Patterning
2. Post-Routing Layer Assignment
3. Layer Assignment for Double Patterning
4. Experimental Results
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Double Patterning Lithography

- As feature sizes keep shrinking, single exposure cannot support any more.
- Extra one time of exposure is used to get the fine line in Double Patterning Lithography.
Layout Decomposition

- During decomposing dense layout onto two masks, pattern can be split to resolve conflicts, which results in stitch
- Pattern split cannot resolve all conflicts
- Stitch has influence on electrical connection of the circuit
- The number unresolvable conflicts and stitches should be minimized in double patterning problem
Graph $G = (V, E)$ is constructed by nodes indicating rectangles and edges indicating electrical connections or adjacency between rectangles:

- Electrical connection corresponds to touching edge, which has negative weight
- Adjacency corresponds to conflict edge, which has positive weight

A bi-coloring solution is needed to decomposing the layout

Max-Cut problem
It is obvious that double patterning problem is NP

Double patterning problem is at most NP-complete
- Reduce from 4-degree Max-Cut problem to a special case of single layer double patterning
  - 4-degree Max-Cut is NP-complete
  - The reduction is polynomial time achievable
  - There is mapping relation between the Max-Cut and the double patterning solution
Reduction

- Mesh drawing of any 4-degree undirected graph
- Cross point substitution with gadget

0 line width, $\sqrt{2}$ double patterning conflict length, mesh based layout
- Black lines and nodes in gadget can be viewed as layout pattern
- Red lines in gadget are conflict edges
Each gadget substitution makes 8 edges contribution on Max-Cut in generated layout.
Outside of the gadget, the edges are subdivided

- Turn an edge into $2i$ pattern sections, which are connected by $2i - 1$ double patterning edges
- They make $2i - 2$ edges contribution on Max-Cut in generated layout
Single layer double patterning problem in NP-complete

When Manhattan distance is considered as double patterning conflict distance
- The double patterning conflict graph is always planar
- Max-Cut problem on it is not NP-hard
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Multi Layer Assignment

- In multi-layer interconnection, wire sections must connect to some and must not connect to some others.
  - Node: wire section, via candidate
  - Crossing edge: overlap sections from different net
  - Continuation edge: electrically connected sections
Layer Assignment for Via Minimization

- Layer assignment for each node
- Weight vector for each via candidate node
  - The number of layers this via goes through under this assignment
- Weight matrix for each edge
  - Whether short circuit happens on crossing edge ($\infty$ or 0)
  - Whether open circuit happens on continuation edge ($\infty$ or 0)

- When the graph is tree, dynamic programming can find the layer assignment to minimize the total weight
- Heuristic
  - Begin from a feasible layout
  - Randomly choose root node to expend a tree in the graph
  - Dynamic programming on the tree
  - Iteratively repeat until no more improvement is made
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The double patterning conflict can be resolved if we change the layer assignment of a rectangle.
Graph Construction

- Consider double patterning distance in the multi layer graph
- Double patterning edge: adjacent sections from different net, whose distance from each other is smaller than double patterning conflict distance and not zero.
Weight Matrix on Double Patterning Edge

- If the layer assignments of two nodes has common metal layer, double patterning conflict would happen.
- Otherwise, zero weight.
- Similar as crossing edge, the difference is the penalty value.
Similar dynamic programming strategy is used to solve the weight minimization problem.

Single layer double patterning algorithms can be used on each reassigned metal layers separately.

In the weight minimization problem, the double patterning edge number is optimized instead of unresolvable conflict.

One more step to reduce the redundant vias is needed.
Via Reduction

- Color information assigned in single layer double patterning is also considered into multi layer graph.
- If changing a rectangle’s layer can result in via reduction without increase of unresolvable conflict, we would accept that change.
- Weight matrix on double patterning edge indicates unresolvable conflict number.
- Weight matrix on continuation edge indicates stitch number.
- Dynamic programming on the updated graph.
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Unresolvable Conflict and Stitch Improvement

- Implemented in C++, tested on CBL testcases and compared with [Xu and Chu ICCAD09] and [Chang and Cong TCAD99]

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<th>#URC</th>
<th>#Stitch</th>
<th>#Via</th>
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Improvement on bottom two metal layers

- Usually only the lowest two metal layers are double patterning layers
- Conduct the algorithm only on the bottom two layers

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Conclusions

- Single layer double patterning problem is NP-complete
- Layer assignment can be employed to reduce the number of unresolvable conflicts and stitches
- The three step algorithm we proposed is effective
Thank you!