16th Asia and South Pacific Design Automation Conference

Session 9D: Friday, January 28, 16:00-18:00 @ Room 416+417
Panel Discussion: Advanced packaging and 3D Technologies

3D packaging is a key technology to satisfy a growing demand to realize highly integrated system and memory. The panel session explores the technologies of three dimensional stacked chips and discusses the challenges to design and test of such integrated chips.
## Time Table

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<th>Contents</th>
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<tr>
<td>5 min</td>
<td>Introductory talk - Basic 3D integration</td>
<td>Moderator</td>
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<td>15 min</td>
<td>Position talk - 3D technology - Situation in Europe</td>
<td>Dr. Plas Imec</td>
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<td>15 min</td>
<td>Position talk - 3D technology - Situation in Asia</td>
<td>Dr. Ezawa Toshiba</td>
</tr>
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<td>15 min</td>
<td>Position talk - 3D technology - Situation in U.S.A</td>
<td>Dr. Orii IBM</td>
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<td>15 min</td>
<td>Position talk - Package technology for 3D integration</td>
<td>Dr. Hiruta J-DEVICES</td>
</tr>
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<td>15 min</td>
<td>Position talk - EDA technology for 3D integration</td>
<td>Dr. Cheung Cadence</td>
</tr>
<tr>
<td>35 min</td>
<td>Discussion</td>
<td>All</td>
</tr>
<tr>
<td>5 min</td>
<td>Summary</td>
<td>Moderator</td>
</tr>
</tbody>
</table>
# 3D vertical integration

## TSV (Through-Silicon-Via)
- TSV
- Thinned Si

## Wire bond
- Wire
- Si

## PoP (Package-on-Package)
- Bump
- Thinned Si

### Benefits
- Small size / High density
- High bandwidth
- Heterogeneous-chip combination
- Low power
- Short time to market

### Applications
- DRAM, Flash, FPGA
- CPU + Memory
- Sensor + DSP

### Questions
Where the market is for 3D ICs with TSVs?
When the 3D-TSV production starts on a large scale?
3D integration process options using TSV

**TSV process flow**

- (1) Via-first
- (2) Via-middle
- (3) Via-last

**TSV interconnect methods**

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td><strong>Pros</strong></td>
<td>Flexible Use of KGD</td>
<td>Flexible Use of KGD</td>
<td>High throughput</td>
</tr>
<tr>
<td><strong>Cons</strong></td>
<td>Handling, Bonding</td>
<td>Handling, Bonding</td>
<td>Same chip size, Yield</td>
</tr>
</tbody>
</table>
Supply chain for 3D integration

- 3D IC integration process needs various expertise techniques.
  => To make 3D ICs widely used, new supply chain infrastructure must be built.

Example of supply chain for heterogeneous chips using wafer-to-wafer stacking

- Supply chain depends on
  - TSV process flow, (via first, middle, last)
  - Interconnect methods (wafer to wafer, wafer to chip, chip to chip)
- Supply chain needs EDA and test

**Question**
Who leads the supply chain to be built for 3D TSV production?
IDM (Integrated Device Manufacturer)? foundry? packaging house?
OSAT (Outsourced Semiconductor Assembly and Test)? EDA vendor?
3D-INTEGRATION: STATUS, CHALLENGES AND OPPORTUNITIES

Geert Van der Plas, Paul Marchal

3D Program IMEC

IMEC, Kapeldreef 75, B-3001, Leuven, Belgium
**TECHNOLOGY STATUS: 3D’S COMING SOON**

**Stacking**

**Key features**
- TSV Via middle
- CuSn & CuCu bonding

**Table: Key Parameters**

<table>
<thead>
<tr>
<th></th>
<th>CuCu</th>
<th>CuSn</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer Ø</td>
<td>200mm</td>
<td>300mm</td>
</tr>
<tr>
<td>Cu TSV Ø Si Via</td>
<td>5µm</td>
<td>5µm</td>
</tr>
<tr>
<td>Height</td>
<td>25µm</td>
<td>50µm</td>
</tr>
<tr>
<td>TSV pitch</td>
<td>10µm</td>
<td>40µm → 20µm</td>
</tr>
</tbody>
</table>
HIGH ASPECT RATIO TSVS on 300mm

via etch

oxide liner

barrier seed

Cu ECD Fill

TSV anneal & CMP

Top

Middle

Bottom
3D STACKING APPROACHES


- Process of Record: Cu/Sn
  - Scaling: 40 → 20µm
  - Cu/Sn Transient-Liquid-Phase, TLP, (250°C)
  - Diffusion bonding (150°C)
CHALLENGES & OPPORTUNITIES ?
ELECTRICAL, THERMAL & THERMO-MECHANICAL CHALLENGES FOR 3D INTEGRATION

Impact of Flip Chip Package on 3D chip-stack (CPI)
- Stress induced by Cu-pillars on low-K
- Stress induced by overmold, laminates CTE mismatch
- Thermal: cooling solutions
- Electrical: power delivery, EMI, ...

Heat dissipation & DRAM operation:
Affected by packaging, mbump placement, underfill, ...

Impact of TSV on dies
- Built-in stress
- Stress varies as function of temperature
- ...

3D Test
- System testability
- KGD testing, physical probing

Test

Reliability
TSV INDUCED STRESS – LIMITING RELIABILITY

A 24x24 matrix of TSV at minimal pitch, causing systematically cracks
DRAM ON LOGIC: THERMAL SIMULATION RESULTS

Temperature distribution in M2

Hot spots

Effect of TSVs and micro bumps

Cu pillars act as local heat sinks
PATHFINDING FLOW: ELECTRICAL, MECHANICAL AND THERMAL AWARE HIGH-LEVEL DESIGN TOOL

- Quick and dirty design flow” providing early assessment of timing/power/area/cost of 3D product ideas
Current status of the PathFinding Flow

System Definition

Virtual Prototyping

Virtual Synthesis, Place & Route

Die Planning

3D-Stack Organization

Package Planning

Timing/Power/Area Analysis

Compact thermal & mechanical models

Power analysis Power/Signal Integrity

Design authoring

Process data

Package data
Die Planning — Illustration

System Definition

Memory

Logic

Virtual prototype — after virtual synthesis, place & route

Bottom tier

Top tier

Constraints

Figures of Merit

1. Area/power

2. Timing analysis

3. TSV displacement maps

4. Thermal maps

5. Cost
Package Planning — Illustration

Virtual die prototype

Virtual package prototype

Figures of Merit

Static voltage drop map

IR drop fix: adding extra power pads/straps

Wire/via currents

Electro-migration

Better via distribution
I. IEEE STANDARDIZATION STUDY GROUP ON 3D-TEST
SSG ON 3D-TEST

Charter

▸ Inventorize need for and timeliness of standards in 3D test and DfT
▸ If appropriate, formulate Project Authorization Requests (PARs) for starting up an IEEE Standard Development Working Group (SDWG)

• Organization & Participation
  – Sponsored by IEEE Test Technology Standards Committee (TTSC)
  – 54 participants from companies/institutes around the globe
  – Chair: Erik Jan Marinissen (IMEC)

• Activities to date
  – Active per January 2010
  – Web site and e-mail reflector for internal communication
  – Weekly WebEx conference calls (provided by Cisco Systems)
  – First formal report due at TTSC meeting at VTS’10, April 20
1. IEEE STANDARDIZATION STUDY GROUP ON 3D-TEST

PARTICIPATING COMPANIES

- Agilent Technologies
- ANALOG DEVICES
- ARM
- AMD
- Cadence
- CASCADE MICROTECH
- CISCO
- IBM
- Infineon
- Intellitech
- NXP
- Oasys
- Panasonic
- Q-STAR TEST
- NECODERA
- QUALCOMM
- ST
- ST ERICSSON
- SYNOPSYS
- TEL
- TEXAS INSTRUMENTS
- TSMC
- VERIGY
- VIRAGE
- Logic

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IEEE STANDARDIZATION STUDY GROUP ON 3D-TEST
INSTITUTES, UNIVERSITIES, AND CONSULTANTS

TU Delft
DfT Solutions Ltd
Friedrich-Alexander-Universität Erlangen-Nürnberg
eda2asic
edacentrum

IMMS
ITRI
Industrial Technology Research Institute
LANCASTER UNIVERSITY
UNIVERSITÄT SIEGEN

TEI
CNRS - Grenoble INP - UJF
POLITECNICO DI TORINO
TTÜ 1918

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During the SSG discussions, the following standardization needs were identified:

- **Die and Stack Test**
  1. DfT test access architecture
  2. Wafer probe interface

- **Access for Board-Level Users**
  3. Board-level interconnect test
  4. Access to embedded instruments

- **Test Data Formats**
  5. Wafer map and device tracking
  6. Standard Test Data Format (STDF)
2. IMEC PROPOSAL FOR 3D DFT TEST ACCESS ARCHITECTURE

LEVERAGING EXISTING DESIGN-FOR-TEST

Functional Design
- ≥2 stacked dies, possibly core-based
- Inter-connect: TSVs
- Extra-connect: pins

Existing Design-for-Test
- Core: internal scan, TDC, LBIST, MBIST; IEEE 1500 wrappers, TAMs
- Product: IEEE 1149.1
2. IMEC PROPOSAL FOR 3D DFT TEST ACCESS ARCHITECTURE

3D DFT ARCHITECTURE – OVERVIEW

Functional Design

- ≥2 stacked dies, possibly core-based
- Inter-connect: TSVs
- Extra-connect: pins

Existing Design-for-Test

- Core: internal scan, TDC, LBIST, MBIST; IEEE 1500 wrappers, TAMs
- Product: IEEE 1149.1

3D DfT Architecture

Test wrapper per die

- Based on IEEE Std 1500
- Two entry/exit points per die:
  1. Pre-bond : extra probe pads
  2. Post-bond : extra TSVs

Board
3. PRE-BOND TEST
FRONT-SIDE vs. BACK-SIDE PROBING

Front-Side of Thick Wafer

- **Benefits**
  - Handling full-thickness wafer easier

- **Drawbacks**
  - Defects due to thinning not covered
  - TSVs not exposed yet; testing them requires expensive DfT / test time

Back-Side of Thinned Wafer

- **Benefits**
  - Test can also cover thinning defects
  - Dual-side access on subset of TSVs

- **Drawbacks**
  - Thinned wafer on carrier: no front-side access
  - Probe force might damage intra-die circuitry
SUMMARY

• Status
  – 3D-SIC TSVs mature
  – Stacking solutions available

Challenges
▷ Reliability
▷ CPI
▷ Thermal
▷ Test

Opportunities for EDA
▷ Pathfinding flow
▷ DfT & infrastructure
3D ecosystem at imec

- Panasonic
- Intel
- Samsung
- Micron
- Foundries
- SAT
- Fabless
- Qualcomm
- Xilinx
- EDA
- Synopsys
- Cadence
- ATRENTA

3D Program

Equipment & Materials Suppliers

- Applied Materials
- SEMITool
- Lam Research
- SUSS MicroTec
- Ultratech
- NEXX
- Tokio Electron
- Nanda Tech
- DISCO
- PVA TePla

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TECHNOLOGICAL RULE CHANGING - 3D & MOBILE VIDEO SERVICES

HD mobile video

E.g. full HD lifecast (lifecast.com, utube, ...)

With an expected ~130% CAGR, Service Providers would commit murder for this technology!!!
ASP-DAC 2011 Panel discussion: Advanced Packaging and 3D Technologies

“Packaging trends towards 3D integration and synergies between wafer process and packaging”

Hirokazu Ezawa
Advanced Packaging Engineering Dept.
Toshiba Corporation Semiconductor Company
2011, January 28th
### Current technology platforms for chip-stacking

<table>
<thead>
<tr>
<th>Process technologies for 3D TSV stacking</th>
<th>CMOS imager WLP</th>
<th>BSI</th>
<th>Chip-on-Chip Logic on Memory</th>
<th>NAND Chip stacking</th>
</tr>
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<tbody>
<tr>
<td>Carrier substrate bonding</td>
<td>+</td>
<td>+</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wafer thinning, cleaning</td>
<td>+</td>
<td>+</td>
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<td>+</td>
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<tr>
<td>TSV etching</td>
<td>+</td>
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<tr>
<td>Fine pitch RDL</td>
<td>+</td>
<td>+</td>
<td></td>
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<tr>
<td>Low temp. curable DL</td>
<td></td>
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</tr>
<tr>
<td>Micro bumping</td>
<td></td>
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<td>+</td>
<td></td>
</tr>
<tr>
<td>Fine pitch solder joining</td>
<td></td>
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<tr>
<td>Juggling thinned chips</td>
<td></td>
<td></td>
<td>+</td>
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</tbody>
</table>

* + qualified for mass production in Toshiba*
Chip-stacking and TSV : Current Status

- **NAND flash memory modules**
  - <30um thick Si chip
  - Stacking 17 chips in a package

- **System LSI modules**
  - Stacking logic on large-scale DRAM
  - Higher data rate has been realized while power consumption is kept lower.

- **CMOS image sensor modules (8 inch)**
  - Reflowable WLP using TSV
  - The worldwide first mass production supplier
Toshiba Launches Industry's Largest[1] Embedded NAND Flash Memory Modules

Toshiba is the first company to combine its sixteen-kilobit NAND flash chips, and adopt advanced thin film thinning and low temperature process technologies to stack them in a unique design known as the 'wire bonding method.'

TOKYO—Toshiba Corporation (TOKYO: 6502) today announced the launch of a 128-gigabyte (GB) embedded NAND flash memory module, the highest capacity yet achieved in the industry. The module is fully compliant with the latest e-MMC™ standard, and is designed for application in a wide range of digital consumer products, including smartphones, tablet PCs and digital video cameras. Samples will be available from September, and mass production will start in the fourth quarter (October to December) of 2010.

The new 128GB embedded device integrates sixteen 64GB (equal to 90B) NAND chips fabricated with Toshiba's cutting-edge 32nm process technology and a dedicated controller into a small package only 17 x 14 x 1.0mm.3 Toshiba is the first company to introduce eighteen-kilobit (8K-bit) NAND flash chips, and is planning advanced thin film thinning and low temperature process technologies to stack them in a unique design known as the 'wire bonding method.'

1 Toshiba's 128GB embedded NAND flash module achieves a world record for the largest capacity available in an eMMC module.

3 Toshiba plans to introduce 8K-bit (16GB) and 32K-bit (64GB) NAND flash chips in late 2010.
Structure of SiP with CoC technology

- Stacking memory chip on logic chip

- Stacking logic chip on larger-size memory chip
  RDLs on memory route signal I/Os from logic chip to peripheral pads on memory chip

Chip size: Logic > Memory

Chip size: Memory > Logic
Chip-stacking instead of e-DRAM

Logic wafer

10um pitch
Cu RDL wiring

40um pitch
Micro-bumping

DRAM wafer

BSG Sawing

RDL

Processor

SCS-DRAM

Mold resin

DDR-SDRAM

Au wire

PKG Substrate

Solder ball

CoC joining

SiP
Chip scale camera module

- Reduction of package size using TSV
- Cost reduction

Current technology

CSCM technology

Cu RDL through TSV

- 10μm
- 50～60um
- 70um
- 100um
Chip-stacking and TSV: Challenges from now on

■ NAND flash memory modules
  - <20um thick Si chip
  - Low power consumption
  How thick would be allowed for proper functionality?
  What makes TSV stacking affordable?

■ System LSI modules
  - 20um pitch bumping and CoC joining
  - Hetero-integration (RF, Analog, Memory, Sensors, MEMS)
  What facilitates synergies between WLCSP and TSV?

■ CMOS image sensor modules
  - Wafer level lens
  How strong would be affinity of TSV for BSI?
Manage to narrow TSV process options

■ Via-middle (Metal filling after FEOL)

- Existing tools available in Si CR.
- No need of low temp. liner-CVD

Concerns:
- TSV process impacts on BEOL.
- Metal contamination when via reveal.

■ Back-side via (Metal filling after Si thinning)

- Separate TSV line from Si fab

Concerns:
- Adhesive limits TSV process temp.
- Need of back-side aligning litho.
- Carrier selection is critical.
TSV stacking as of today and PKG challenges

Key equipments and materials for TSV mass production
Still under basic development
- BSG/CMP/Wet-clean integrated tool
- Temporary bonding adhesives and their relevant bonding/de-bonding HVP tool
- 12inch WTW bonding tool. Yield allowance.
- Inspection tool (via voids…)
- Sawing tool for thinned wafer instead of blade.

Cost-reduced 3D packaging
- Wire free
- Organic substrate free
- Fine pitch RDL on Fan-Out WLCSP
FAQ

■ Where do you allocate TSV production?
  - TBD.

■ When would TSV products sprout up?
  - Depends on the market providing novel values.

■ What are dominant factors affecting TSV process cost?
  - Thinner Si would be preferred.
    Specific design for thinned Si?

  - Throughput of multi-chip stacking
    W-to-W bonding would be preferred.
    Specific design dedicated to its stacking?

Any other vying technologies for 3D integration?...
Thank you.
Future Challenges for 3D-IC Packaging
Panel Discussion: Advanced Packaging & 3D Technologies

Electronic & Optical Packaging, IBM Research Tokyo
Yasumitsu Orii
Our world is becoming interconnected.

All of those instrumented and interconnected things are becoming intelligent. They are being linked to powerful new backend systems that can process all that data, and to advanced analytics capable of turning it into real insight, in real time.
Internet of Things
More Powerful Computer System for Smarter Planet

- Sensors are being embedded everywhere: in cars, appliances, cameras, roads, pipelines...
- The oceans of data to be produced.
- All of those instrumented and interconnected things are becoming intelligent. They are being linked to powerful new backend systems that can process all that data, and to advanced analytics capable of turning it into real insight, in real time.

World First PFLOPS Super Computer:
1.03 PFLOPS (Jun/2008)

Exascale computing system

System Performance

- At double the speed/2 years
- At four times the speed/2 years
- In a conventional manner

Sensors are being embedded everywhere: in cars, appliances, cameras, roads, pipelines…
The oceans of data to be produced.
All of those instrumented and interconnected things are becoming intelligent. They are being linked to powerful new backend systems that can process all that data, and to advanced analytics capable of turning it into real insight, in real time.
Technical Challenges for 3D-IC

1. Die to Die Interconnection
2. Die to Die underfill
Configurations of IMC Bonding Evaluation Test Vehicles

Configuration-A : Si on Si
- Underfill
- Top die
- Low-volume solder joint (IMC bonding)
- Silicon Interposer
- Cu/Ni/In bump
- W-filled TSV

Configuration-B : Si on Si + Organic
- Underfill
- Top die
- Low-volume solder joint (IMC bonding)
- Silicon Interposer
- Pre-solder
- Organic Substrate

60th ECTC, 2010, K. Sakuma, Y. Orii et al.
Joint Materials Comparison: Cu/Sn and Cu/Ni/In

Configuration-A: Si on Si

Joint's Stress
Cu/Sn
- Top die
- Cu
- Cu-Sn IMC
- Silicon interposer

Cu/Ni/In
- Top die
- Cu
- In
- Cu
- Silicon interposer

DTC

<table>
<thead>
<tr>
<th>Test</th>
<th>Stress Conditions</th>
<th>Cycle time (min)</th>
<th>Number of cycles completed</th>
</tr>
</thead>
<tbody>
<tr>
<td>DTC</td>
<td>-55°C to +125°C</td>
<td>35</td>
<td>1,000</td>
</tr>
</tbody>
</table>

60th ECTC, 2010, K. Sakuma, Y. Orii et al.,

- Stress on the joints is greater for the Cu/Sn joint than the Cu/Ni/In joint.
- A gradual increase in electrical resistance observed for the Si die stack samples with Cu/Sn joints.
Reliability Results of 3D Chip on Organic sub. with IMC Bonding

Configuration-B : Si on Si + Organic

Deep Thermal Cycle (DTC) results for stacked samples

DTC Condition: -55 to +125°C, 15min/15min (Δ T = 180°C)
Time of exposure at min and max T: 10min

- The mechanical stress during thermal cycling has a significant impact on the bonding interconnections.

Cu/Sn joint

Cu/Ni/In joint
The stress on the joints increases with decreasing Si IP thickness.
The stress on the joints increases with increasing top Si chip thickness for thin Si IP, but the effect becomes less significant as the Si IP thickness increases.
Future Underfill Requirements for 3D-IC

- **New requirements for Inter Chip Fill**
  - Higher thermal conductivity
  - Lower stress & high reliability
    - *Lower cure shrinkage*
    - *Lower thermal expansion (low CTE)*
    - *Not high modulus (for stress reduction)*
    - High insulation and low ion content
  - Good 3D chip assemble capability for many-layers stack
    - *Stack Joining process (Patented)*

![Diagram showing interchip fill process]

- **Align and "place" chips sequentially**
- **Temporally stack @ ~150deg.C**
- **Join solder bumps of "all" chips together**
- **All chip joining @ 250deg.C**

Resin shrinkage has serious effect on device performance of thin silicon chip.
C4 Non-Wets in the chip attach process occurs due to the warpage of an organic substrate.

The warpage of an organic substrate can be predicted based on the circuit design.

SEM-DICM can detect the fine pitch interconnection displacement with 0.02μm resolution.

Types of DICM (Digital Image Correlation Method)

<table>
<thead>
<tr>
<th>Resolution (μm)</th>
<th>Conventional</th>
<th>Laser Microscope, SEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.02 - 0.05</td>
<td></td>
</tr>
</tbody>
</table>

We are aiming to detect the displacement of 10μm pitch interconnection.

Crystal orientation in fine pitch interconnection may have an impact on the reliability.

- The number of crystals in 10μm pitch interconnection is only 10-20.
- Strain distribution may be dependent on the crystal orientation.

High strain area reaches the outer surface and when a crack exists here, the interconnection can fail immediately.

Ex. Measured displacement of 100μm pitch interconnection by laser microscope DICM

Ex. Simulated strain distribution, considering the orientation of 20 crystals.
Thank for your attention.
Advanced Packaging and 3D Technologies

~Packaging Technology~

YOICHI HIRUTA

http://www.j-devices.co.jp

Feb. 28, 2011
Memory Assembly & System Application

- Wide Band
  - Large Capacity
  - SCS (Stacked Chip SOC)

- PoP/Module/External
  - Graphic

- High End SoC

- DTV

- SiP (C2C)

- SiP (SBB)

- DSC

- eDRAM

- Logic Size

- Memory Size

- Graphic

- DVC

- Telecom LCDC

- Telecom

- DVC

- TV LCDC

- Telecom

- Graphic

- SiP (C2C)

- SiP (SBB)

- DSC

- eDRAM

- Memory Assembly & System Application
Die Stacking Technology

8M SRAM
128M SDRAM
Spacer
256M NAND
128M NOR
Spacer
128M NOR
Spacer
128M NOR
Substrate

Package Thickness 1.4mm
Die Stacking Technology

60um Pitch Micro Bump

- DDR Memory (256M)
- Custom DRAM (48M)
- Logic Chip
- Substrate

Cross section of inter-connection
Highly Integrated BGA (Embedded HS & CoC Interconnect)

- **HS Attach Paste**
- **Spacer with DAF**
- **Embedded Heat Spreader**
- **Mold Resin**
- **B’g Wire**
- **Die Attach Paste**
- **Substrate (2/4 Layer)**
- **Solder Ball**

### θ Ja vs Heat Slug Size

- **Ref. normal HSBGA**: 9.8W/mK (HS 27.7sq.mm, Mold resin 3.1W/mK)

- **Lower θ Ja @ Same mold resin**

- **Reduce HS size @ Same θ Ja**
Interconnection Roadmap

Wire Bonding (US+Thermo-compression)

SBB (Stud Bump Bonding)

Pad Pitch [μm]

μ Interconnect

J-DEVICES CORPORATION 株式会社 ジェイデバイス
Design Issue in 3D

Peripheral I/F

2D I/F

Input

Processing

Output
Design Issue in 3D

Peripheral I/F

2D I/F

✓ Floor Plan
✓ Optimizing the Design
✓ Linkage with Packaging
ASP-DAC 2011 Panel Discussion: Advanced Packaging and 3D Technologies

Chris Cheung
Engineering Director
Silicon-Package-Board
Cadence Design Systems

Jan 28, 2011
Challenges in 3D-IC & Packaging Design

- Mixed Technologies
  - Flip chip, Wire bond, stacked (face to face) or Side by side, with or without Silicon Interposer, SiP (System in Package), PoP (Package-on-Package)
  - Digital vs Mixed Signal designs
  - Net list, Physical Implementation (DRC and manufacturing requirements)
  - Electrical, Power and Thermal Analysis
Challenges in 3D-IC & Packaging Design

• Multiple factors to consider in today’s Product Design
  – Chip set proliferation may require a “reference board” design
    • Ease of adoption
    • Reference guide
  – Time to market pressure may influence your design choice
    • Buy (or re-use) vs “Start from scratch”
  – True cost and performance has to take a system view
    • Chip, Package and Board

• “Distributed” Design
  – Teams may be at different locations and time zones
  – Co-Planning / Co-Design / Co-Analysis
  – Manage data exchange (Between design teams, vendors)
Technologies at Cadence: “Prototyping for 3D Packaging”

• The ability to view and prototype the entire product (chip, package and/or board) in an “integrated” environment.
• For rapid prototyping one must be able to optimize chip, package and board for routability and layer utilization, constraint budgeting across the design fabrics.
  – Signal traversed through the entire “system”, thus delay has to be measured from chip to chip.
  – Consider different design options to identify a design choice or at least narrow down to couple options for further analysis
  – An interesting application may be “RFQ” (Request for Quote)
Technologies at Cadence: “Prototyping for 3D Packaging”

• Results from prototype may be disseminated to design teams for implementation
  – Net lists, constraints, stack-ups, “rough” physical layouts
  – Data flows from prototype into design tools

• ECO Management
  – Be able to resolve design conflicts or changes during implementation phase

• Final Design Verification
  – Does your final design met the original specification?
  – Cost analysis
Technologies at Cadence: Considerations in “3D Packaging Prototype”

• Obviously: Planar and 3D viewing of the design
  – Picture worth a thousand words

• For Prototyping to be effective, all design fabrics must be integrated into the same environment
  – One tool, one window and one UI
  – Each fabric must maintains its own net list, substrate layers and design units, design rules.

• Prototype system must integrate seamlessly with design tools
  – Who is the typical owner of the prototype?
  – Support distributed design teams
Idea to Reality?

• Example of a reference board with a co-design package + co-design die. The board contains additional standard parts.

• Flight lines showing possible routing congestions, results of net assignments and placement.
Future of 3D Packaging …

- EDA company’s goal is to provide solutions for electronic designs
  - EDA company must listen to and understand customers’ needs
  - EDA company must provide leading edge solutions
  - EDA company need to partner when a solution requires multiple technology disciplines
- We are here to listen!