ASP-DAC 2011 Advance Program

16th Asia and South Pacific Design Automation Conference
Date: January, 25-28, 2011
Place: Pacifico Yokohama, Yokohama, Japan

http://www.aspdac.com/

Highlights

Opening and Keynote I

Wednesday, January 26, 8:30-10:00

Takayuki Kawahara (Hitachi, Japan) *"Non-Volatile Memory and Normally-Off Computing"*

Keynote II

Thursday, January 27, 9:00-10:00

Ajoy Bose (Atrenta Inc., U.S.A.) *"Managing Increasing Complexity through Higher-Level of Abstraction: What the Past Has Taught Us about the Future"*

Keynote III

Friday, January 28, 9:00-10:00

Subhasish Mitra (Stanford Univ., U.S.A.) *"Robust Systems: From Clouds to Nanotubes"*

Special Sessions

1D: University LSI Design Contest (Presentation + Poster Discussion)

Wednesday, January 26, 10:20-12:20

2D: Emerging Memory Technologies and Its Implication on Circuit Design and Architectures

Wednesday, January 26, 13:40-15:40

2D-1: Meng-Fan Chang (National Tsing Hua Univ., Taiwan), Pi-Feng Chiu, Shyh-Shyuan Sheu (ITRI, Taiwan) *"Circuit Design Challenges in Embedded Memory and Resistive RAM (RRAM) for Mobile SoC and 3D-IC"*

3C: Post-Silicon Techniques to Counter Process and Electrical Parameter Variability

Wednesday, January 26, 16:00-18:00

3C-1: Ming Gao, Peter Lisherness, Kwang-Ting (Tim) Cheng (Univ. of California, Santa Barbara, U.S.A.) *"Post-silicon Bug Detection for Variation Induced Electrical Bugs"*

3D: Recent Advances in Verification and Debug

Wednesday, January 26, 16:00-18:00

3D-1: Miroslav N. Velev, Ping Gao (Aries Design Automation, U.S.A.) *"Automatic Formal Verification of Reconfigurable DSPs"*

4D: Advanced Patterning and DFM for Nanolithography beyond 22nm

Thursday, January 27, 10:20-12:20

4D-1: Soichi Inoue, Sachiko Kobayashi (Toshiba, Japan) *"All-out Fight against Yield Losses by Design-manufacturing Collaboration in Nano-lithography Era"*

7D: Virtualization, Programming, and Energy-Efficiency Design Issues of Embedded Systems

Friday, January 28, 10:20-12:20

7D-1: Tatsuo Nakajima, Yuki Kinebuchi, Hiromasa Shimada, Alexandre Courbot, Tsung-Han Lin (Waseda Univ., Japan) *"Temporal and Spatial Isolation in a Virtualization Layer for Multi-core Processor based Information Appliances"*

Designers' Forum

5D: (Panel Discussion) C-P-B Co-design/Co-verification Technology for DDR3 1.6G in Consumer Products

Thursday, January 27, 13:40-15:40

Organizer: Koji Kato (Sony, Japan)
Moderator: Makoto Nagata (Kobe Univ., Japan)
Panelists:
Keisuke Matsunami (Sony, Japan)
Yoshinori Fukuba (Toshiba, Japan)
Ji Zheng (Apache Design Solutions, U.S.A.)
Jen-Tai Hsu (Global Unichip Corp., U.S.A.)
CP Hung (ASE, Taiwan)

6D: (Invited Talks) Emerging Technologies for Wellness Applications

Thursday, January 27, 16:00-18:00

6D-1: Masaharu Imai, Yoshinori Takeuchi, Keishi Sakanushi, Hirofumi Iwato (Osaka Univ., Japan) *"Biological Information Sensing Technologies for Medical, Health Care, and Wellness Applications"*

6D-2: Srinivasa R. Sridhara (Texas Instruments, Inc., U.S.A.) *"Ultra-Low Power Microcontrollers for Portable, Wearable, and Implantable Medical Electronics"*

6D-3: Valer Pop, Ruben de Francisco, Hans Pflug, Juan Santana, Huib Visser, Ruud Vullers, Harmke de Groot, Bert Gyselinckx (IMEC, Netherlands) *"Human++: Wireless Autonomous Sensor Technology for Body Area Networks"*

6D-4: Koji Ara, Tomoaki Akitomi, Nobuo Sato, Satomi Tsuji, Miki Hayakawa, Yoshihiro Wakisaka, Norio Ohkubo, Rieko Otsuka, Fumiko Beniyama, Norihiko Moriwaki, Kazuo Yano (Hitachi, Ltd., Japan) *"Healthcare of an Organization: Using Wearable Sensors and Feedback System for Energizing Workers"*

8D: (Invited Talks) State-of-The-Art SoCs and Design Methodologies

Friday, January 28, 13:40-15:40

8D-1: Takao Suzuki (Panasonic Corp., Japan) *"Advanced System LSIs for Home 3D System"*

8D-2: Yoshiyuki Kitasho, Yu Kikuchi, Takayoshi Shimazawa, Yasuo Ohara, Masafumi Takahashi, Yoshio Masubuchi, Yukihito Oowaki (Toshiba Corp. Semiconductor Company, Japan) *"Development of Low Power and High Performance Application Processor (T6G) for Multimedia Mobile Applications"*

8D-3: Atsuki Inoue (Platform Technologies Laboratories, Japan) *"Design Constraint of Fine Grain Supply Voltage Control LSI"*

8D-4: Masaru Takahashi (Renesas Electronics Corp., Japan) *"FPGA Prototyping using Behavioral Synthesis for Improving Video Processing Algorithm and FHD TV SoC Design"*

8D-5: Nobuyuki Nishiguchi (STARC, Japan) *"An RTL-to-GDS2 Design Methodology for Advanced System LSI"*

9D: (Panel Discussion) Advanced Packaging and 3D Technologies

Friday, January 28, 16:00-18:00

Organizer: Yoshio Masubuchi (Toshiba, Japan)
Moderator: Yaoko Nakagawa (Hitachi, Japan)
Panelists:
Geert Van der Plas (IMEC, Belgium)
Hirokazu Ezawa (Toshiba, Japan)
Yasumitsu Orii (IBM, Japan)
Yoichi Hiruta (J-Devices, Japan)
Chris Cheung (Cadence Design Systems, U.S.A.)

Two Full-Day and Four Half-Day Tutorials

FULL-DAY Tutorials:

Tutorial 5: Post Silicon Debug

Tuesday, January 25, 9:30-12:30, 14:00-17:00

Organizer:
Subhasish Mitra (Stanford University, USA)
Speakers:
Rand Gray (Intel, USA)
Nagib Hakim (Intel, USA)
Sascha Junghans (IBM, Germany)

Tutorial 6: MPSoC: Multiprocessor System on Chip

Tuesday, January 25, 9:30-12:30, 14:00-17:00

Organizer:
Ahmed Amine Jerraya (CEA-LETI, France)
Speakers:
Takashi Miyamori (Toshiba, Japan)
Rephael David (LIST, France)
Sani Nassif (IBM, USA)
Sungjoo Yoo (Postech, Korea)

HALF-DAY Tutorials:

Tutorial 1: Advanced CMOS Device Technologies (1)

Tuesday, January 25, 9:30-12:30

Tutorial 2: Advanced CMOS Device Technologies (2)

Tuesday, January 25, 14:00-17:00

Organizer:
Ken Uchida (Tokyo Institute of Technology, Japan)
Speakers:
Paul C. McIntyre (Stanford University, USA)
Shinichi Takagi (The University of Tokyo, Japan)
Toshiro Hiramoto (The University of Tokyo, Japan)
Arvind Kumar (IBM, USA)

Tutorial 3: 3D Integration (1)

Tuesday, January 25, 9:30-12:30

Tutorial 4: 3D Integration (2)

Tuesday, January 25, 14:00-17:00

Organizer:
Hideki Asai (Shizuoka University, Japan)
Speakers:
Joungho Kim (KAIST, Korea)
Hideki Asai (Shizuoka University, Japan)
G. Van der Plas (IMEC, Belgium)
Erping Li (A-STAR IHPC, Singapore)

Tuesday, January 25, 2011

Registration (8:00 -)				
9:30	**Tutorial 1: Advanced CMOS Device Technologies (1) [Half day]** Organizer: Ken Uchida (Tokyo Inst. of Tech., Japan) 1. "Gate Stack of Advanced CMOS Devices: High-k/Metal-Gate Technologies" Paul C. McIntyre (Stanford Univ., USA) 2. "Channel/Stress Engineering for Advanced CMOS Devices: Performance Booster Technologies" Shinichi Takagi (Univ. of Tokyo, Japan)	**Tutorial 3: 3D Integration (1) [Half day]** Organizer: Hideki Asai (Shizuoka Univ., Japan) 1. "Signal Integrity of TSV Based 3D IC" Joungho Kim (KAIST, Korea) 2. "Advanced PI/SI/EMI Simulation Technology for 3D Co-Design" Hideki Asai (Shizuoka Univ., Japan)	**Tutorial 5: Post Silicon Debug [Full day]** Organizer: Subhasish Mitra (Stanford Univ., USA) 1. "Introduction" 2. "Logical Errors" Sascha Junghans (IBM, Germany)	**Tutorial 6: MPSoC: Multiprocessor System on Chip [Full day]** Organizer: Ahmed Jerraya (CEA-LETI, France) 1. "Energy Efficient Multicore (MPSoC) Architectures" Takashi Miyamori (Toshiba, Japan) 2. "Software Architecture for Energy Efficient Execution of Multicore Systems" Rephael David (LIST, France)
12:30				
Lunch Break [coupon] (12:30 - 14:00)				
14:00	**Tutorial 2: Advanced CMOS Device Technologies (2) [Half day]** Organizer: Ken Uchida (Tokyo Inst. of Tech., Japan) 1. "Variability and Device/Circuit Co-Design with Planar Bulk MOSFETs" Toshiro Hiramoto (Univ. of Tokyo, Japan) 2. "Three-Dimensional Devices for 22nm and Beyond" Arvind Kumar (IBM, USA)	**Tutorial 4: 3D Integration (2) [Half day]** Organizer: Hideki Asai (Shizuoka Univ., Japan) 1. "3D Cu TSV Technology" Geert Van der Plas (IMEC, Belgium) 2. "Signal Integrity and Power Integrity Modeling in High Speed Electronic Integration" Erping Li (A-STAR IHPC, Singapore)	3. "Electrical Errors" 4. "Research Topics" Rand Gray (Intel, USA) Nagib Hakim (Intel, USA)	3. "Fabrication Technology Implications on MPSoC" Sani Nassif (IBM, USA) 4. "Challenges and Trends for MPSoC Design" Sungjoo Yoo (Postech, Korea)
17:00				

Wednesday, January 26, 2011

Registration (7:00 -)

8:30 – 10:00

1K: Opening and Keynote Session I

Chair: Kunihiro Asada (Univ. of Tokyo, Japan)

Takayuki Kawahara (Hitachi, Japan) *"Non-Volatile Memory and Normally-Off Computing"*

Coffee break (10:00 - 10:20)

10:20 – 12:20

1A: Analog, Mixed-Signal & RF Verification, Abstraction and Analysis	**1B: Emerging Memories and System Applications**	**1C: Advances in Model Order Reduction and Extraction Techniques**	**1D: University LSI Design Contest**
Chairs: Eric Keiter (Sandia National Labs, U.S.A.), Chin-Fong Chiu (National Chip Implementation Center, Taiwan)	Chairs: Mehdi Tahoori (Karlsruhe Inst. of Tech., Germany), Chun-Ming Huang (National Chip Implementation Center, Taiwan)	Chairs: Sheldon X.-D. Tan (Univ. of California, Riverside, U.S.A.), Genichi Tanaka (Renesas, Japan)	Chairs: Masanori Hariyama (Tohoku Univ., Japan), Hiroshi Kawaguchi (Kobe Univ., Japan)
1A-1: Ying-Chih Wang, Anvesh Komuravelli, Paolo Zuliani, Edmund M. Clarke (Carnegie Mellon Univ., U.S.A.) *"Analog Circuit Verification by Statistical Model Checking"*	**1B-1:** Miao Hu, Hai Li (Polytechnic Institute of New York Univ., U.S.A.), Yiran Chen (Univ. of Pittsburgh, U.S.A.), Xiaobin Wang (Seagate Technology, U.S.A.), Robinson Pino (AFRL/RITC, U.S.A.) *"Geometry Variations Analysis of TiO_2 Thin-Film and Spintronic Memristors"*	**1C-1:** Zheng Zhang (Massachusetts Inst. of Tech., U.S.A.), Qing Wang, Ngai Wong (Univ. of Hong Kong, Hong Kong), Luca Daniel (Massachusetts Inst. of Tech., U.S.A.) *"A Moment-Matching Scheme for the Passivity-Preserving Model Order Reduction of Indefinite Descriptor Systems with Possible Polynomial Parts"*	(The titles of the presentations are listed in the next page)
1A-2: Chenjie Gu, Jaijeet Roychowdhury (Univ. of California, Berkeley, U.S.A.) *"FSM Model Abstraction for Analog/Mixed-Signal Circuits by Learning from I/O Trajectories"*	**1B-2:** Xiangyu Dong, Yuan Xie (Pennsylvania State Univ., U.S.A.) *"AdaMS: Adaptive MLC/SLC Phase-Change Memory Design for File Storage"*	**1C-2:** Xiang Wang, Qing Wang, Zheng Zhang, Quan Chen, Ngai Wong (Univ. of Hong Kong, Hong Kong) *"Balanced Truncation for Time-Delay Systems Via Approximate Gramians"*	
1A-3: Xue-Xin Liu (Univ. of California, Riverside, U.S.A.), Hao Yu (Nanyang Technological Univ., Singapore), Jacob Relles, Sheldon X.-D. Tan (Univ. of California, Riverside, U.S.A.) *"A Structured Parallel Periodic Arnoldi Shooting Algorithm for RF-PSS Analysis based on GPU Platforms"*	**1B-3:** Joonsoo Kim, Joonsoo Lee, Jacob A. Abraham (Univ. of Texas, Austin, U.S.A.) *"System Accuracy Estimation of SRAM-based Device Authentication"*	**1C-3:** Yu Bi (Delft Univ. of Tech., Netherlands), Pieter Harpe (Holst Centre/IMEC, Netherlands), Nick van der Meijs (Delft Univ. of Tech., Netherlands) *"Efficient Sensitivity-Based Capacitance Modeling for Systematic and Random Geometric Variations"*	
1A-4: Hui Xu, Guoyong Shi, Xiaopeng Li (Shanghai Jiao Tong Univ., China) *"Hierarchical Exact Symbolic Analysis of Large Analog Integrated Circuits By Symbolic Stamps"*	**1B-4:** Wulong Liu, Yu Wang, Wei Liu, Yuchun Ma (Tsinghua Univ., China), Yuan Xie (Pennsylvania State Univ., U.S.A.), Huazhong Yang (Tsinghua Univ., China) *"On-Chip Hybrid Power Supply System for Wireless Sensor Nodes"*	**1C-4:** Wenjian Yu, Chao Hu (Tsinghua Univ., China), Wangyang Zhang (Carnegie Mellon Univ., U.S.A.) *"Parallel Statistical Capacitance Extraction of On-Chip Interconnects with an Improved Geometric Variation Model"*	

Lunch Break / University LSI Design Contest Discussion (12:20 - 13:40)

10:20 **1D: University LSI Design Contest**

Chairs: Masanori Hariyama (Tohoku Univ., Japan), Hiroshi Kawaguchi (Kobe Univ., Japan)

1D-1: Cheng-An Chien, Yao-Chang Yang, Hsiu-Cheng Chang, Jia-Wei Chen, Cheng-Yen Chang, Jiun-In Guo, Jinn-Shyan Wang (National Chung Cheng Univ., Taiwan), Ching-Hwa Cheng (Feng Chia Univ., Taiwan) *"A H.264/MPEG-2 Dual Mode Video Decoder Chip Supporting Temporal/Spatial Scalable Video"*

1D-2: Benjamin Devlin, Makoto Ikeda, Kunihiro Asada (Univ. of Tokyo, Japan) *"A Gate-level Pipelined 2.97GHz Self Synchronous FPGA in 65nm CMOS"*

1D-3: Dan Bao, Chuan Wu, Yan Ying, Yun Chen, Xiao Yang Zeng (Fudan Univ., China) *"A 4.32 mm^2 170mW LDPC Decoder in 0.13μm CMOS for WiMax/Wi-Fi Applications"*

1D-4: Jaehyun Jeong, Tetsuya Iizuka, Toru Nakura, Makoto Ikeda, Kunihiro Asada (Univ. of Tokyo, Japan) *"All-Digital PMOS and NMOS Process Variability Monitor Utilizing Buffer Ring with Pulse Counter"*

1D-5: Takehiko Amaki, Masanori Hashimoto, Takao Onoye (Osaka Univ., Japan) *"Jitter Amplifier for Oscillator-Based True Random Number Generator"*

1D-6: Jun Furuta (Kyoto Univ., Japan), Chikara Hamanaka, Kazutoshi Kobayashi (Kyoto Inst. of Tech., Japan), Hidetoshi Onodera (Kyoto Univ., Japan) *"A 65nm Flip-Flop Array to Measure Soft Error Resiliency against High-Energy Neutron and Alpha Particles"*

1D-7: Yu-Tzu Tsai, Cheng-Chih Tsai (Feng Chia Univ., Taiwan), Cheng-An Chien (National Chung Cheng Univ., Taiwan), Ching-Hwa Cheng (Feng Chia Univ., Taiwan), Jiun-In Guo (National Chung Cheng Univ., Taiwan) *"Dual-Phase Pipeline Circuit Design Automation with a Built-in Performance Adjusting Mechanism"*

1D-8: Lei Zhao, Daisuke Ikebuchi, Yoshiki Saito, Masahiro Kamata, Naomi Seki, Yu Kojima, Hideharu Amano (Keio Univ., Japan), Satoshi Koyama, Tatsunori Hashida, Yusuke Umahashi, Daiki Masuda, Kimiyoshi Usami (Shibaura Inst. of Tech., Japan), Kazuki Kimura, Mitaro Namiki (Tokyo Univ. of Agri. and Tech., Japan), Seidai Takeda, Hiroshi Nakamura (Univ. of Tokyo, Japan), Masaaki Kondo (Univ. of Electro-Communications, Japan) *"Geyser-2: The Second Prototype CPU with Fine-grained Run-time Power Gating"*

1D-9: Yoshiya Komatsu, Shota Ishihara, Masanori Hariyama, Michitaka Kameyama (Tohoku Univ., Japan) *"An Implementation of an Asychronous FPGA Based on LEDR/Four-Phase-Dual-Rail Hybrid Architecture"*

1D-10: Shuming Chen, Xiaowen Chen, Yi Xu, Jianghua Wan, Jianzhuang Lu, Xiangyuan Liu, Shenggang Chen (National Univ. of Defense Tech., China) *"Design and Chip Implementation of a Heterogeneous Multi-core DSP"*

1D-11: Yu-Tzu Tsai, Cheng-Chih Tsai (Feng Chia Univ., Taiwan), Cheng-An Chien (National Chung Cheng Univ., Taiwan), Ching-Hwa Cheng (Feng Chia Univ., Taiwan), Jiun-In Guo (National Chung Cheng Univ., Taiwan) *"A Low-Power Management Technique for High-Performance Domino Circuits"*

1D-12: Tomoyuki Nakabayashi, Takahiro Sasaki, Kazuhiko Ohno, Toshio Kondo (Mie Univ., Japan) *"Design and Evaluation of Variable Stages Pipeline Processor Chip"*

1D-13: Shuo-Hung Chen, Hsiao-Mei Lin, Ching-Chou Hsieh, Chih-Tsun Huang, Jing-Jia Liou, Yeh-Ching Chung (National Tsing Hua Univ., Taiwan) *"TurboVG: A HW/SW Co-Designed Multi-Core OpenVG Accelerator for Vector Graphics Applications with Embedded Power Profiler"*

1D-14: Yu-Han Yuan, Wei-Ming Chen, Hsi-Pin Ma (National Tsing Hua Univ., Taiwan) *"Design and Implementation of a High Performance Closed-Loop MIMO Communications with Ultra Low Complexity Handset"*

1D-15: Ahmed Musa, Rui Murakami, Takahiro Sato, Win Chiavipas, Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan) *"A 58-63.6GHz Quadrature PLL Frequency Synthesizer Using Dual-Injection Technique"*

1D-16: Wei Deng, Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan) *"An Ultra-low-voltage LC-VCO with a Frequency Extension Circuit for Future 0.5-V Clock Generation"*

1D-17: Yu-Hao Hsu, Yang-Syu Lin, Ching-Te Chiu, Jen-Ming Wu, Shuo-Hung Hsu, Fan-Ta Chen, Min-Sheng Kao, Wei-Chih Lai, YarSun Hsu (National Tsing Hua Univ., Taiwan) *"A 32Gbps Low Propagation Delay 4x4 Switch IC for Feedback-Based System in 0.13μm CMOS Technology"*

1D-18: Nguyen Ngoc Mai Khanh, Masahiro Sasaki, Kunihiro Asada (Univ. of Tokyo, Japan) *"A Fully Integrated Shock Wave Transmitter with an On-Chip Dipole Antenna for Pulse Beam-Formability in 0.18-μm CMOS"*

1D-19: Xin Zhang, Koichi Ishida, Makoto Takamiya, Takayasu Sakurai (Univ. of Tokyo, Japan) *"An On-Chip Characterizing System for Within-Die Delay Variation Measurement of Individual Standard Cells in 65-nm CMOS"*

1D-21: Wen Fan, Chiu-Sing Choy (Chinese Univ. of Hong Kong, Hong Kong) *"Robust and Efficient Baseband Receiver Design for MB-OFDM UWB System"*

1D-22: Yuji Osaki, Tetsuya Hirose, Nobutaka Kuroki, Masahiro Numa (Kobe Univ., Japan) *"A 95-nA, 523ppm/$^\circ$C, 0.6-μW CMOS Current Reference Circuit with Subthreshold MOS Resistor Ladder"*

1D-23: Ting Gao, Wei Li, Ning Li, Junyan Ren (Fudan Univ., China) *"A 80-400 MHz 74 dB-DR Gm-C Low-Pass Filter With a Unique Auto-Tuning System"*

1D-24: Chenchang Zhan, Wing-Hung Ki (Hong Kong Univ. of Science and Tech., Hong Kong) *"An Adaptively Biased Low-Dropout Regulator with Transient Enhancement"*

1D-25: Dong Qiu, Ting Yi, Zhiliang Hong (Fudan Univ., China) *"A Low-Power Triple-Mode Sigma-Delta DAC for Reconfigurable (WCDMA/TD-SCDMA/GSM) Transmitters"*

1D-26: Mohiuddin Hafiz, Nobuo Sasaki, Kentaro Kimoto, Takamaro Kikkawa (Hiroshima Univ., Japan) *"A Simple Non-coherent Solution to the UWB-IR Communication"*

12:20

Lunch Break / University LSI Design Contest Discussion (12:20 - 13:40)

13:40

2A: Scheduling Techniques for Embedded Systems

Chairs: Dip Goswami (Tech. Univ. of Munich, Germany), Naehyuck Chang (Seoul National Univ., Republic of Korea)

2A-1: Pratyush Kumar, Lothar Thiele (ETH Zürich, Switzerland) *"Thermally Optimal Stop-Go Scheduling of Task Graphs with Real-Time Constraints"*

2A-2: Yazhi Huang, Tiantian Liu, Jason Xue (City Univ. of Hong Kong, Hong Kong) *"Register Allocation for Write Activity Minimization on Non-volatile Main Memory"*

2A-3: Vivek Chaturvedi, Gang Quan (Florida International Univ., U.S.A.) *"Leakage Conscious DVS Scheduling for Peak Temperature Minimization"*

2A-4: Hessam Kooti, Deepak Mishra, Eli Bozorgzadeh (Univ. of California, Irvine, U.S.A.) *"Reconfiguration-aware Real-Time Scheduling under QoS Constraint"*

15:40

2B: Memory Architecture and Buffer Optimization

Chairs: Yu Wang (Tsinghua Univ., China), Yinhe Han (Chinese Academy of Sciences, China)

2B-1: Bin Li, Zhen Fang, Ravi Iyer (Intel Corp., U.S.A.) *"Template-based Memory Access Engine for Accelerators in SoCs"*

2B-2: Abdul Naeem, Xiaowen Chen, Zhonghai Lu, Axel Jantsch (Royal Inst. of Tech., Sweden) *"Realization and Performance Comparison of Sequential and Weak Memory Consistency Models in Network-on-Chip based Multi-core Systems"*

2B-3: Wan-Ting Su, Jih-Sheng Shen, Pao-Ann Hsiung (National Chung Cheng Univ., Taiwan) *"Network-on-Chip Router Design with Buffer-Stealing"*

2B-4: Tae-ho Shin (Seoul National Univ., Republic of Korea), Hyunok Oh (Hanyang Univ., Republic of Korea), Soonhoi Ha (Seoul National Univ., Republic of Korea) *"Minimizing Buffer Requirements for Throughput Constrained Parallel Execution of Synchronous Dataflow Graph"*

2C: Modeling for Signal and Power Integrity

Chairs: Hideki Asai (Shizuoka Univ., Japan), Kimihiro Ogawa (STARC, Japan)

2C-1: Mysore Sriram (Intel Corp., India) *"A Fast Approximation Technique for Power Grid Analysis"*

2C-2: Khaled Salah Mohamed (Mentor Graphics, Egypt), Hani Ragai (Ain-Shams Univ., Egypt), Yehea Ismail (Nile Univ., Egypt), Alaa El Rouby (Mentor Graphics, Egypt) *"Equivalent Lumped Element Models for Various n-Port Through Silicon Vias Networks"*

2C-3: Xuchu Hu, Matthew R. Guthaus (Univ. of California, Santa Cruz, U.S.A.) *"Clock Tree Optimization for Electromagnetic Compatibility (EMC)"*

2C-4: Sangmin Kim, Inhak Han, Seungwhun Paik, Youngsoo Shin (KAIST, Republic of Korea) *"Pulser Gating: A Clock Gating of Pulsed-Latch Circuits"*

2D: Special Session: Emerging Memory Technologies and Its Implication on Circuit Design and Architectures

Chairs: Hideki Asai (Shizuoka Univ., Japan), Kimihiro Ogawa (STARC, Japan)

2D-1: Meng-Fan Chang (National Tsing Hua Univ., Taiwan), Pi-Feng Chiu, Shyh-Shyuan Sheu (ITRI, Taiwan) *"Circuit Design Challenges in Embedded Memory and Resistive RAM (RRAM) for Mobile SoC and 3D-IC"*

2D-2: Yiran Chen (Univ. of Pittsburgh, U.S.A.), Hai Li (Polytechnic Institute of New York Univ., U.S.A.) *"Emerging Sensing Techniques for Emerging Memories"*

2D-3: Guangyu Sun, Dimin Liu, Jin Ouyang, Yuan Xie (Pennsylvania State Univ., U.S.A.) *"A Frequent-Value Based PRAM Memory Architecture"*

2D-4: Wei Lu, Kuk-Hwan Kim, Ting Chang, Siddharth Gaba (Univ. of Michigan, U.S.A.) *"Two-Terminal Resistive Switches (Memristors) for Memory and Logic Applications"*

Coffee break (15:40 - 16:00)

16:00

3A: High-Level Embedded Systems Design Techniques

Chairs: Yuko Hara-Azumi (Ritsumeikan Univ., Japan), Yiran Chen (Univ. of Pittsburgh, U.S.A.)

3A-1: Dip Goswami, Reinhard Schneider, Samarjit Chakraborty (Tech. Univ. of Munich, Germany) *"Co-design of Cyber-Physical Systems via Controllers with Flexible Delay Constraints"*

3A-2: Ang-Chih Hsieh, Chun-Cheng Liu, TingTing Hwang (National Tsing Hua Univ., Taiwan) *"Enhanced Heterogeneous Code Cache Management Scheme for Dynamic Binary Translation"*

3A-3: Deepak Gangadharan (National Univ. of Singapore, Singapore), Samarjit Chakraborty (Tech. Univ. of Munich, Germany), Roger Zimmermann (National Univ. of Singapore, Singapore) *"Fast Hybrid Simulation for Accurate Decoded Video Quality Assessment on MPSoC Platforms with Resource Constraints"*

3A-4: Marisha Rawlins, Ann Gordon-Ross (Univ. of Florida, U.S.A.) *"On the Interplay of Loop Caching, Code Compression, and Cache Configuration"*

18:00

3B: Timing, Power, and Thermal Issues

Chair: Deming Chen (Univ. of Illinois, Urbana-Champaign, U.S.A.)

3B-1: Jaeyong Chung (Univ. of Texas, Austin, U.S.A.), Jinjun Xiong, Vladimir Zolotov (IBM, U.S.A.), Jacob A. Abraham (Univ. of Texas, Austin, U.S.A.) *"Path Criticality Computation in Parameterized Statistical Timing Analysis"*

3B-2: Pratyush Kumar, David Atienza (EPFL, Switzerland) *"Run-Time Adaptable On-Chip Thermal Triggers"*

3B-3: Kan Wang, Yuchun Ma, Sheqin Dong, Yu Wang, Xianlong Hong (Tsinghua Univ., China), Jason Cong (Univ. of California, Los Angeles, U.S.A.) *"Rethinking Thermal Via Planning with Timing-Power-Temperature Dependence for 3D ICs"*

3B-4: Jun Zhou, Senthil Jayapal, Jan Stuyt, Jos Huisken, Harmke de Groot (Holst Centre/IMEC, Netherlands) *"The Impact of Inverse Narrow Width Effect on Sub-threshold Device Sizing"*

3C: Special Session: Post-Silicon Techniques to Counter Process and Electrical Parameter Variability

Chair: Jing-Jia Liou (National Tsing Hua Univ., Taiwan)

3C-1: Ming Gao, Peter Lisherness, Kwang-Ting (Tim) Cheng (Univ. of California, Santa Barbara, U.S.A.) *"Post-silicon Bug Detection for Variation Induced Electrical Bugs"*

3C-2: Jing-Jia Liou, Ying-Yen Chen, Chun-Chia Chen, Chung-Yen Chien, Kuo-Li Wu (National Tsing Hua Univ., Taiwan) *"Diagnosis-assisted Supply Voltage Configuration to Increase Performance Yield of Cell-Based Designs"*

3C-3: Masanori Hashimoto (Osaka Univ. & JST, CREST, Japan) *"Run-Time Adaptive Performance Compensation using On-chip Sensors"*

3C-4: David Brooks (Harvard Univ., U.S.A.) *"The Alarms Project: A Hardware/Software Approach to Addressing Parameter Variations"*

3D: Special Session: Recent Advances in Verification and Debug

Chair: Chung-Yang (Ric) Huang (National Taiwan Univ., Taiwan)

3D-1: Miroslav N. Velev, Ping Gao (Aries Design Automation, U.S.A.) *"Automatic Formal Verification of Reconfigurable DSPs"*

3D-2: Chung-Yang Huang, Yu-Fan Yin, Chih-Jen Hsu (National Taiwan Univ., Taiwan), Thomas B. Huang, Ting-Mao Chang (InPA Systems, Inc., U.S.A.) *"SoC HW/SW Verification and Validation"*

3D-3: Masahiro Fujita (Univ. of Tokyo and CREST, Japan) *"Utilizing High Level Design Information to Speed up Post-silicon Debugging"*

3D-4: Andreas Veneris, Brian Keng (Univ. of Toronto, Canada), Sean Safarpour (Vennsa Technologies, Inc., Canada) *"From RTL to Silicon: The Case for Automated Debug"*

3D-5: Rainer Dömer, Weiwei Chen, Xu Han (Univ. of California, Irvine, U.S.A.), Andreas Gerstlauer (Univ. of Texas, Austin, U.S.A.) *"Multi-Core Parallel Simulation of System-Level Description Languages"*

Thursday, January 27, 2011

Registration (7:30 -)

9:00 – 10:00

2K: Keynote Session II

Chair: Kunihiro Asada (Univ. of Tokyo, Japan)

Ajoy Bose (Atrenta Inc., U.S.A.) *"Managing Increasing Complexity through Higher-Level of Abstraction: What the Past Has Taught Us about the Future"*

Coffee break (10:00 - 10:20)

10:20 – 12:20

4A: Design Automation for Emerging Technologies	**4B: Novel Network-on-Chip Architecture Design**	**4C: Architecture Design and Reliability**	**4D: Special Session: Advanced Patterning and DFM for Nanolithography beyond 22nm**
Chairs: Hai Li (Polytechnic Institute of New York Univ., U.S.A.), Yu Wang (Tsinghua Univ., China)	Chairs: Yoshinori Takeuchi (Osaka Univ., Japan), Hao Yu (Nanyang Technological Univ., Singapore)	Chairs: Shigeru Yamashita (Ritsumeikan Univ., Japan), Rolf Drechsler (Univ. of Bremen, Germany)	Organizer: David Z. Pan (Univ. of Texas, Austin, U.S.A.)
4A-1: Masoud Zamani (Northeastern Univ., U.S.A.), Mehdi B. Tahoori (Karlsruhe Inst. of Tech., Germany) *"Variation-aware Logic Mapping for Crossbar Nano-architectures"*	**4B-1:** Sudeep Pasricha, Shirish Bahirat (Colorado State Univ., U.S.A.) *"OPAL: A Multi-Layer Hybrid Photonic NoC for 3D ICs"*	**4C-1:** Jason Anderson (Univ. of Toronto, Canada), Qiang Wang (Xilinx, Inc., U.S.A.) *"Area-Efficient FPGA Logic Elements: Architecture and Synthesis"*	**4D-1:** Soichi Inoue, Sachiko Kobayashi (Toshiba, Japan) *"All-out Fight against Yield Losses by Design-manufacturing Collaboration in Nano-lithography Era"*
4A-2: Tan Yan, Qiang Ma, Scott Chilstedt, Martin Wong, Deming Chen (Univ. of Illinois, Urbana-Champaign, U.S.A.) *"Routing with Graphene Nanoribbons"*	**4B-2:** Jin Ouyang, Yuan Xie (Pennsylvania State Univ., U.S.A.) *"Enabling Quality-of-Service in Nanophotonic Network-on-Chip"*	**4C-2:** Donkyu Baek, Insup Shin, Seungwhun Paik, Youngsoo Shin (KAIST, Republic of Korea) *"Selectively Patterned Masks: Structured ASIC with Asymptotically ASIC Performance"*	**4D-2:** Sam Sivakumar (Intel Corp., U.S.A.) *"EUV Lithography: Prospects and Challenges"*
4A-3: Chia-Jen Chang, Pao-Jen Huang, Tai-Chen Chen, Chien-Nan Jimmy Liu (National Central Univ., Taiwan) *"ILP-Based Inter-Die Routing for 3D ICs"*	**4B-3:** Cheng Liu, Lei Zhang, Yinhe Han, Xiaowei Li (Chinese Academy of Sciences, China) *"Vertical Interconnects Squeezing in Symmetric 3D Mesh Network-on-Chip"*	**4C-3:** Shao-Lun Huang, Chi-An Wu, Kai-Fu Tang, Chang-Hong Hsu, Chung-Yang (Ric) Huang (National Taiwan Univ., Taiwan) *"A Robust ECO Engine by Resource-Constraint-Aware Technology Mapping and Incremental Routing Optimization"*	**4D-3:** Jack J.H. Chen, Faruk Krecinic, Jen-Hom Chen, Raymond P.S. Chen, Burn J. Lin (Taiwan Semiconductor Manufacturing Company, Taiwan) *"Future Electron-Beam Lithography and Implications on Design and CAD Tools"*
4A-4: Shashikanth Bobba (Swiss Inst. of Tech. Lausanne (EPFL), Switzerland), Ashutosh Chakraborty (Univ. of Texas, Austin, U.S.A.), Olivier Thomas, Perrine Batude, Thomas Ernst, Olivier Faynot (LETI, France), David Z. Pan (Univ. of Texas, Austin, U.S.A.), Giovanni De Micheli (Swiss Inst. of Tech. Lausanne (EPFL), Switzerland) *"CELONCEL: Effective Design Technique for 3-D Monolithic Integration targeting High Performance Integrated Circuits"*	**4B-4:** Wenmin Hu (National Univ. of Defense Tech., China), Zhonghai Lu, Axel Jantsch (Royal Inst. of Tech., Sweden), Hengzhu Liu (National Univ. of Defense Tech., China) *"Power-efficient Tree-based Multicast Support for Networks-on-Chip"*	**4C-4:** Chi-Chen Peng, Chen Dong, Deming Chen (Univ. of Illinois, Urbana-Champaign, U.S.A.) *"SETmap: A Soft Error Tolerant Mapping Algorithm for FPGA Designs with Low Power"*	**4D-4:** Chul-Hong Park (Samsung Electronics, Republic of Korea), David Z. Pan (Univ. of Texas, Austin, U.S.A.), Kevin Lucas (Synopsys, U.S.A.) *"Exploration of VLSI CAD Researches for Early Design Rule Evaluation"*

Lunch Break / **Student Forum** (12:20 - 13:40)

13:40

5A: System-Level Simulation

Chairs: Nagisa Ishiura (Kwansei Gakuin Univ., Japan), Bo-Cheng Charles Lai (National Chiao Tung Univ., Taiwan)

5A-1: Marius Gligor, Frédéric Pétrot (TIMA Laboratory, CNRS/INP Grenoble/UJF, France) *"Handling Dynamic Frequency Changes in Statically Scheduled Cycle-Accurate Simulation"*

5A-2: Ryo Kawahara, Kenta Nakamura, Kouichi Ono, Takeo Nakada (IBM Research, Japan), Yoshifumi Sakamoto (Global Business Services, IBM Japan, Japan) *"Coarse-grained Simulation Method for Performance Evaluation a of Shared Memory System"*

5A-3: Wei Zang, Ann Gordon-Ross (Univ. of Florida, U.S.A.) *"T-SPaCS – A Two-Level Single-Pass Cache Simulation Methodology"*

5A-4: Héctor Posadas, Luis Diaz, Eugenio Villar (Univ. of Cantabria, Spain) *"Fast Data-Cache Modeling for Native Co-Simulation"*

15:40

5B: Resilient and Thermal-Aware NoC Design

Chairs: Michihiro Koibuchi (NII, Japan), Pao-Ann Hsiung (National Chung Cheng Univ., Taiwan)

5B-1: Yung-Chang Chang (ITRI, Taiwan), Ching-Te Chiu (National Tsing Hua Univ., Taiwan), Shih-Yin Lin, Chung-Kai Liu (ITRI, Taiwan) *"On the Design and Analysis of Fault Tolerant NoC Architecture Using Spare Routers"*

5B-2: Cheng Liu, Lei Zhang, Yinhe Han, Xiaowei Li (Chinese Academy of Sciences, China) *"A Resilient On-chip Router Design Through Data Path Salvaging"*

5B-3: Sudeep Pasricha, Yong Zou (Colorado State Univ., U.S.A.) *"NS-FTR: A Fault Tolerant Routing Scheme for Networks on Chip with Permanent and Runtime Intermittent Faults"*

5B-4: Zhiliang Qian, Chi-Ying Tsui (Hong Kong Univ. of Science and Tech., Hong Kong) *"A Thermal-aware Application Specific Routing Algorithm for Network-on-Chip Design"*

5C: High-Level and Logic Synthesis

Chair: Kiyoung Choi (Seoul National Univ., Republic of Korea)

5C-1: Yu Pang (Chongqing Univ. of Posts and Telecommunications, China), Katarzyna Radecka, Zeljko Zilic (McGill Univ., Canada) *"An Efficient Hybrid Engine to Perform Range Analysis and Allocate Integer Bit-widths for Arithmetic Circuits"*

5C-2: Rami Beidas, Wai Sum Mong, Jianwen Zhu (Univ. of Toronto, Canada) *"Register Pressure Aware Scheduling for High Level Synthesis"*

5C-3: James Williamson (Univ. of Colorado, Boulder, U.S.A.), Yinghai Lu (Northwestern Univ., U.S.A.), Li Shang (Univ. of Colorado, Boulder, U.S.A.), Hai Zhou (Northwestern Univ., U.S.A.), Xuan Zeng (Fudan Univ., China) *"Parallel Cross-Layer Optimization of High-Level Synthesis and Physical Design"*

5C-4: Bei Yu, Sheqin Dong, Yuchun Ma, Tao Lin, Yu Wang (Tsinghua Univ., China), Song Chen, Satoshi GOTO (Waseda Univ., Japan) *"Network Flow-based Simultaneous Retiming and Slack Budgeting for Low Power Design"*

5D: Designers' Forum: (Panel Discussion) C-P-B Co-design/Co-verification Technology for DDR3 1.6G in Consumer Products

Organizer: Koji Kato (Sony, Japan)

Moderator:
Makoto Nagata (Kobe Univ., Japan)

Panelists:
Keisuke Matsunami (Sony, Japan)
Yoshinori Fukuba (Toshiba, Japan)
Ji Zheng (Apache Design Solutions, U.S.A.)
Jen-Tai Hsu (Global Unichip Corp., U.S.A.)
CP Hung (ASE, Taiwan)

Coffee break (15:40 - 16:00)

16:00

6A: Design Validation Techniques

Chairs: Miroslav Velev (Aries Design Automation, U.S.A.), Kiyoharu Hamaguchi (Osaka Univ., Japan)

6A-1: Brian Keng, Andreas Veneris (Univ. of Toronto, Canada) *"Managing Complexity in Design Debugging with Sequential Abstraction and Refinement"*

6A-2: Hong-Zu Chou (National Taiwan Univ., Taiwan), Kai-Hui Chang (Avery Design Systems, Inc., U.S.A.), Sy-Yen Kuo (National Taiwan Univ., Taiwan) *"Facilitating Unreachable Code Diagnosis and Debugging"*

6A-3: Hongxia Fang (Duke Univ., U.S.A.), Zhiyuan Wang, Xinli Gu (Cisco Systems Inc., U.S.A.), Krishnendu Chakrabarty (Duke Univ., U.S.A.) *"Deterministic Test for the Reproduction and Detection of Board-Level Functional Failures"*

6A-4: Chi-Hui Lee, Che-Hua Shih, Juinn-Dar Huang, Jing-Yang Jou (National Chiao Tung Univ., Taiwan) *"Equivalence Checking of Scheduling with Speculative Code Transformations in High-Level Synthesis"*

18:00

6B: Clock Network Design

Chairs: Yuchun Ma (Tsinghua Univ., China), Youngsoo Shin (KAIST, Republic of Korea)

6B-1: Kyoung-Hwan Lim, Taewhan Kim (Seoul National Univ., Republic of Korea) *"An Optimal Algorithm for Allocation, Placement, and Delay Assignment of Adjustable Delay Buffers for Clock Skew Minimization in Multi-Voltage Mode Designs"*

6B-2: Tak-Kei Lam, Xiaoqing Yang, Wai-Chung Tang, Yu-Liang Wu (Chinese Univ. of Hong Kong, Hong Kong) *"On Applying Erroneous Clock Gating Conditions to Further Cut Down Power"*

6B-3: Li Li (Northwestern Univ., U.S.A.), Jian Sun (Fudan Univ., China), Yinghai Lu, Hai Zhou (Northwestern Univ., U.S.A.), Xuan Zeng (Fudan Univ., China) *"Low Power Discrete Voltage Assignment Under Clock Skew Scheduling"*

6B-4: Yanling Zhi (Fudan Univ., China), Hai Zhou (Northwestern Univ., U.S.A.), Xuan Zeng (Fudan Univ., China) *"A Practical Method for Multi-domain Clock Skew Optimization"*

6C: Advances in Routing

Chair: David Z. Pan (Univ. of Texas, Austin, U.S.A.)

6C-1: Jia-Ru Chuang, Jai-Ming Lin (National Cheng Kung Univ., Taiwan) *"Efficient Multi-Layer Obstacle-Avoiding Preferred Direction Rectilinear Steiner Tree Construction"*

6C-2: Fong-Yuan Chang (National Tsing Hua Univ., Taiwan), Sheng-Hsiung Chen (SpringSoft, Taiwan), Ren-Song Tsay, Wai-Kei Mak (National Tsing Hua Univ., Taiwan) *"Cut-Demand Based Routing Resource Allocation and Consolidation for Routability Enhancement"*

6C-3: Wen-Hao Liu, Yih-Lang Li (National Chiao Tung Univ., Taiwan) *"Negotiation-Based Layer Assignment for Via Count and Via Overflow Minimization"*

6C-4: Michael Moffitt (IBM Corp., U.S.A.), C. N. Sze (IBM Research, U.S.A.) *"Wire Synthesizable Global Routing for Timing Closure"*

6D: Designers' Forum: Emerging Technologies for Wellness Applications

Chair: Hideki Yoshizawa (Fujitsu Labs., Japan)

6D-1: Masaharu Imai, Yoshinori Takeuchi, Keishi Sakanushi, Hirofumi Iwato (Osaka Univ., Japan) *"Biological Information Sensing Technologies for Medical, Health Care, and Wellness Applications"*

6D-2: Srinivasa R. Sridhara (Texas Instruments, Inc., U.S.A.) *"Ultra-Low Power Microcontrollers for Portable, Wearable, and Implantable Medical Electronics"*

6D-3: Valer Pop, Ruben de Francisco, Hans Pflug, Juan Santana, Huib Visser, Ruud Vullers, Harmke de Groot, Bert Gyselinckx (IMEC, Netherlands) *"Human++: Wireless Autonomous Sensor Technology for Body Area Networks"*

6D-4: Koji Ara, Tomoaki Akitomi, Nobuo Sato, Satomi Tsuji, Miki Hayakawa, Yoshihiro Wakisaka, Norio Ohkubo, Rieko Otsuka, Fumiko Beniyama, Norihiko Moriwaki, Kazuo Yano (Hitachi, Ltd., Japan) *"Healthcare of an Organization: Using Wearable Sensors and Feedback System for Energizing Workers"*

Banquet (19:00 - 21:00)

Friday, January 28, 2011

Registration (7:30 -)

9:00 — 10:00

3K: Keynote Session III

Chair: Kunihiro Asada (Univ. of Tokyo, Japan)

Subhasish Mitra (Stanford Univ., U.S.A.) *"Robust Systems: From Clouds to Nanotubes"*

Coffee break (10:00 - 10:20)

10:20 — 12:20

7A: System Level Analysis and Optimization	**7B: NBTI and Power Gating**	**7C: Physical Design for Yield**	**7D: Special Session: Virtualization, Programming, and Energy-Efficiency Design Issues of Embedded Systems**
Chairs: Hiroshi Saito (Aizu Univ., Japan), Lovic Ganchier (Kyushu Univ., Japan)	Chairs: Kimiyoshi Usami (Shibaura Inst. of Tech., Japan), Toshio Sudo (Shibaura Inst. of Tech., Japan)	Chair: Cliff Sze (IBM, U.S.A.)	Organizer & Moderator: Tei-Wei Kuo (National Taiwan Univ., Taiwan)
7A-1: Junwhan Ahn, Imyong Lee, Kiyoung Choi (Seoul National Univ., Republic of Korea) *"A Polynomial-Time Custom Instruction Identification Algorithm Based on Dynamic Programming"*	**7B-1:** Ashutosh Chakraborty, David Z. Pan (Univ. of Texas, Austin, U.S.A.) *"Controlling NBTI Degradation during Static Burn-in Testing"*	**7C-1:** Jae-Seok Yang, Jiwoo Pak (Univ. of Texas, Austin, U.S.A.), Xin Zhao, Sung Kyu Lim (Georgia Tech, U.S.A.), David Z. Pan (Univ. of Texas, Austin, U.S.A.) *"Robust Clock Tree Synthesis with Timing Yield Optimization for 3D-ICs"*	**7D-1:** Tatsuo Nakajima, Yuki Kinebuchi, Hiromasa Shimada, Alexandre Courbot, Tsung-Han Lin (Waseda Univ., Japan) *"Temporal and Spatial Isolation in a Virtualization Layer for Multi-core Processor based Information Appliances"*
7A-2: Jiawei Huang, John Lach (Univ. of Virginia, U.S.A.) *"Exploring the Fidelity-Efficiency Design Space using Imprecise Arithmetic"*	**7B-2:** Yongho Lee (Samsung Electronics, Republic of Korea), Taewhan Kim (Seoul National Univ., Republic of Korea) *"A Fine-Grained Technique of NBTI-Aware Voltage Scaling and Body Biasing for Standard Cell Based Designs"*	**7C-2:** Xin Gao, Luca Macchiarulo (Univ. of Hawaii, Manoa, U.S.A.) *"Track Routing Optimizing Timing and Yield"*	**7D-2:** Jason Loew, Jesse Elwell, Dmitry Ponomarev, Patrick H. Madden (SUNY Binghamton Computer Science Department, U.S.A.) *"Mathematical Limits of Parallel Computation for Embedded Systems"*
7A-3: Juinn-Dar Huang, Yi-Hang Chen, Ya-Chien Ho (National Chiao Tung Univ., Taiwan) *"Throughput Optimization for Latency-Insensitive System with Minimal Queue Insertion"*	**7B-3:** Ming-Chao Lee, Yu-Guang Chen, Ding-Kai Huang, Shih-Chieh Chang (National Tsing Hua Univ., Taiwan) *"NBTI-Aware Power Gating Design"*	**7C-3:** Shing-Tung Lin (National Tsing Hua Univ., Taiwan), Kuang-Yao Lee (Taiwan Semiconductor Manufacturing Company, Taiwan), Ting-Chi Wang (National Tsing Hua Univ., Taiwan), Cheng-Kok Koh (Purdue Univ., U.S.A.), Kai-Yuan Chao (Intel Corp., U.S.A.) *"Simultaneous Redundant Via Insertion and Line End Extension for Yield Optimization"*	**7D-3:** Jen-Wei Hsieh (National Taiwan Univ. of Science and Tech., Taiwan), Yuan-Hao Chang (National Taipei Univ. of Tech., Taiwan), Wei-Li Lee (National Taiwan Univ. of Science and Tech., Taiwan) *"An Enhanced Leakage-Aware Scheduler for Dynamically Reconfigurable FPGAs"*
7A-4: Yi-Siou Chen, Lih-Yih Chiou, Hsun-Hsiang Chang (National Cheng Kung Univ., Taiwan) *"A Fast and Effective Dynamic Trace-based Method for Analyzing Architectural Performance"*	**7B-4:** Tung-Yeh Wu, Shih-Hsin Hu, Jacob A. Abraham (Univ. of Texas, Austin, U.S.A.) *"Robust Power Gating Reactivation By Dynamic Wakeup Sequence Throttling"*	**7C-4:** Kang Zhao, Jinian Bian (Tsinghua Univ., China) *"Pruning-based Trace Signal Selection Algorithm"*	**7D-4:** Tiefei Zhang (Zhejiang Univ., China), Ying-Jheng Chen, Che-Wei Chang, Chuan-Yue Yang, Tei-Wei Kuo (National Taiwan Univ., Taiwan), Tianzhou Chen (Zhejiang Univ., China) *"Power Management Strategies in Data Transmission"*

Lunch Break (12:20 - 13:40)

13:40

8A: Modeling and Design for Variability

Chairs: Fedor G. Pikus (Mentor Graphics, U.S.A.), Hidetoshi Matsuoka (Fujitsu Laboratories, Japan)

8A-1: Mingzhi Gao, Zuochang Ye, Dajie Zeng, Yan Wang, Zhiping Yu (Tsinghua Univ., China) *"Robust Spatial Correlation Extraction with Limited Sample via L1-Norm Penalty"*

8A-2: Ken-ichi Shinkai, Masanori Hashimoto (Osaka Univ., Japan) *"Device-Parameter Estimation with On-chip Variation Sensors Considering Random Variability"*

8A-3: Jianxin Fang, Sachin S. Sapatnekar (Univ. of Minnesota, U.S.A.) *"Accounting for Inherent Circuit Resilience and Process Variations in Analyzing Gate Oxide Reliability"*

8A-4: Chih-Hsiang Ho, Chao Lu, Debabrata Mohapatra, Kaushik Roy (Purdue Univ., U.S.A.) *"Variation-Tolerant and Self-Repair Design Methodology for Low Temperature Polycrystalline Silicon Liquid Crystal and Organic Light Emitting Diode Displays"*

15:40

8B: Test for Reliability and Yield

Chairs: Yu Huang (Mentor Graphics, U.S.A.), Yoshinobu Higami (Ehime Univ., Japan)

8B-1: Fu-Wei Chen, Shih-Liang Chen, Yung-Sheng Lin, TingTing Hwang (National Tsing Hua Univ., Taiwan) *"A Physical-Location-Aware Fault Redistribution for Maximum IR-Drop Reduction"*

8B-2: Vikas Chandra, Robert Aitken (ARM, U.S.A.) *"On the Impact of Gate Oxide Degradation on SRAM Dynamic and Static Write-ability"*

8B-3: Xuan-Lun Huang, Ping-Ying Kang (National Taiwan Univ., Taiwan), Hsiu-Ming Chang (Univ. of California, Santa Barbara, U.S.A.), Jiun-Lang Huang (National Taiwan Univ., Taiwan), Yung-Fa Chou, Yung-Pin Lee, Ding-Ming Kwai, Cheng-Wen Wu (ITRI, Taiwan) *"A Self-Testing and Calibration Method for Embedded Successive Approximation Register ADC"*

8B-4: Yeonbok Lee, Takeshi Matsumoto, Masahiro Fujita (Univ. of Tokyo, Japan) *"On-chip Dynamic Signal Sequence Slicing for Efficient Post-Silicon Debugging"*

8C: System-Level Power Optimization

Chairs: Masanori Muroyama (Tohoku Univ., Japan), Lih-Yih Chiou (National Cheng Kung Univ., Taiwan)

8C-1: Abhishek Sinkar, Nam Sung Kim (Univ. of Wisconsin-Madison, U.S.A.) *"AVS-Aware Power-Gate Sizing for Maximum Performance and Power Efficiency of Power-Constrained Processors"*

8C-2: Junhe Gan (Tech. Univ. of Denmark, Denmark), Flavius Gruian (Lund Univ., Sweden), Paul Pop, Jan Madsen (Tech. Univ. of Denmark, Denmark) *"Energy/Reliability Trade-offs in Fault-Tolerant Event-Triggered Distributed Embedded Systems"*

8C-3: Jingqing Mu, Roman Lysecky (Univ. of Arizona, U.S.A.) *"Profile Assisted Online System-Level Performance and Power Estimation for Dynamic Reconfigurable Embedded Systems"*

8C-4: Jiayin Li, Meikang Qiu (Univ. of Kentucky, U.S.A.), Jian-wei Niu (Beihang Univ., China), Tianzhou Chen (Zhejiang Univ., China) *"Battery-Aware Task Scheduling in Distributed Mobile Systems with Lifetime Constraint"*

8D: Designers' Forum: State-of-The-Art SoCs and Design Methodologies

Chair: Masaitsu Nakajima (Panasonic, Japan)

8D-1: Takao Suzuki (Panasonic Corp., Japan) *"Advanced System LSIs for Home 3D System"*

8D-2: Yoshiyuki Kitasho, Yu Kikuchi, Takayoshi Shimazawa, Yasuo Ohara, Masafumi Takahashi, Yoshio Masubuchi, Yukihito Oowaki (Toshiba Corp. Semiconductor Company, Japan) *"Development of Low Power and High Performance Application Processor (T6G) for Multimedia Mobile Applications"*

8D-3: Atsuki Inoue (Platform Technologies Laboratories, Japan) *"Design Constraint of Fine Grain Supply Voltage Control LSI"*

8D-4: Masaru Takahashi (Renesas Electronics Corp., Japan) *"FPGA Prototyping using Behavioral Synthesis for Improving Video Processing Algorithm and FHD TV SoC Design"*

8D-5: Nobuyuki Nishiguchi (STARC, Japan) *"An RTL-to-GDS2 Design Methodology for Advanced System LSI"*

Coffee break (15:40 - 16:00)

16:00

9A: Printability and Mask Optimization

Chairs: Murakata Masami (STARC, Japan), Zheng Shi (Zhejiang Univ., China)

9A-1: Duo Ding (Univ. of Texas, Austin, U.S.A.), Andres Torres, Fedor Pikus (Mentor Graphics Corp., U.S.A.), David Pan (Univ. of Texas, Austin, U.S.A.) *"High Performance Lithographic Hotspot Detection using Hierarchically Refined Machine Learning"*

9A-2: Jen-Yi Wuu (Univ. of California, Santa Barbara, U.S.A.), Fedor G. Pikus, Andres Torres (Mentor Graphics Corp., U.S.A.), Malgorzata Marek-Sadowska (Univ. of California, Santa Barbara, U.S.A.) *"Rapid Layout Pattern Classification"*

9A-3: Hongbo Zhang, Yuelin Du, Martin D. F. Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.), Kai-Yuan Chao (Intel Corp., U.S.A.) *"Mask Cost Reduction with Circuit Performance Consideration for Self-Aligned Double Patterning"*

9A-4: Jian Sun (Fudan Univ., China), Yinghai Lu, Hai Zhou (Northwestern Univ., U.S.A.), Xuan Zeng (Fudan Univ., China) *"Post-Routing Layer Assignment for Double Patterning"*

18:00

9B: Emerging Solutions in Scan Testing

Chairs: Seiji Kajihara (Kyusyu Inst. of Tech., Japan), Ting Ting Hwang (National Tsing Hua Univ., Taiwan)

9B-1: Yoshinobu Higami, Hiroshi Takahashi, Shinya Kobayashi (Ehime Univ., Japan), Kewal K. Saluja (Univ. of Wisconsin-Madison, U.S.A.) *"Fault Simulation and Test Generation for Clock Delay Faults"*

9B-2: Jia Li (Tsinghua Univ., China), Qiang Xu (Chinese Univ. of Hong Kong, Hong Kong), Dong Xiang (Tsinghua Univ., China) *"Compression-Aware Capture Power Reduction for At-Speed Testing"*

9B-3: Joseph Howard, Sudhakar M Reddy (Univ. of Iowa, U.S.A.), Irith Pomeranz (Purdue Univ., U.S.A.), Bernd Becker (Univ. of Freiburg, Germany) *"Fault Diagnosis Aware ATE Assisted Test Response Compaction"*

9B-4: Hideo Fujiwara (NAIST, Japan), Katsuya Fujiwara, Hideo Tamamoto (Akita Univ., Japan) *"Secure Scan Design Using Shift Register Equivalents against Differential Behavior Attack"*

9C: Clock and Package

Chair: Yasuhiro Takashima (Univ. of Kitakyushu, Japan)

9C-1: Kuan-Yu Lin, Hong-Ting Lin, Tsung-Yi Ho (National Cheng Kung Univ., Taiwan) *"An Efficient Algorithm of Adjustable Delay Buffer Insertion for Clock Skew Minimization in Multiple Dynamic Supply Voltage Designs"*

9C-2: Alireza Rakhshanfar, Jason Anderson (Univ. of Toronto, Canada) *"An Integer Programming Placement Approach to FPGA Clock Power Reduction"*

9C-3: Ren-Jie Lee, Hung-Ming Chen (National Chiao Tung Univ., Taiwan) *"Row-Based Area-Array I/O Design Planning in Concurrent Chip-Package Design Flow"*

9C-4: Qiang Ma, Hui Kong, Martin D. F. Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.), Evangeline F. Y. Young (Chinese Univ. of Hong Kong, Hong Kong) *"A Provably Good Approximation Algorithm for Rectangle Escape Problem with Application to PCB Routing"*

9D: Designers' Forum: (Panel Discussion) Advanced Packaging and 3D Technologies

Organizer: Yoshio Masubuchi (Toshiba, Japan)

Moderator:
Yaoko Nakagawa (Hitachi, Japan)

Panelists:
Geert Van der Plas (IMEC, Belgium)
Hirokazu Ezawa (Toshiba, Japan)
Yasumitsu Orii (IBM, Japan)
Yoichi Hiruta (J-Devices, Japan)
Chris Cheung (Cadence Design Systems, U.S.A.)

Registration

Conference pre-registration through Web is strongly advised. Please visit the Online Registration page:

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FEES

Category	By Dec. 17 '10	After Dec. 18 '10	On site
[Conference]			
∗Member	53,000 yen	58,000 yen	60,000 yen
Non-member	63,000 yen	68,000 yen	70,000 yen
Full-time Student	33,000 yen	38,000 yen	40,000 yen
[Keynotes + Designers' Forum]			
	23,000 yen	28,000 yen	30,000 yen

∗ **Member of IEEE, ACM SIGDA, IEICE, IPSJ**

Category	By Dec. 17 '10	After Dec. 18 '10 / On site
[Tutorial] (Full-Day or two Half-Days)		
∗Member	32,000 yen	37,000 yen
Non-member	38,000 yen	42,000 yen
Full-time Student	22,000 yen	25,000 yen
∗∗Student Group	15,400 yen	17,500 yen
[Tutorial] (Half-Day)		
∗Member	22,000 yen	26,000 yen
Non-member	26,000 yen	30,000 yen
Full-time Student	14,000 yen	16,000 yen
∗∗Student Group	9,800 yen	11,200 yen

∗ **Member of IEEE, ACM SIGDA, IEICE, IPSJ**

∗∗ "Student Group" discount is applied to a group of four or more students from the same affiliation (faculty or graduate school). A list of the group members must be submitted. Please check the details in the following registration form.

The conference fee includes:

- Admission to all sessions (including keynote speeches and Designers' Forum) without tutorial
- Banquet (excluding Full-time Students)
- One refreshment per break
- Conference kit (with a final program and one CD-ROM of conference proceedings)

The Designers' Forum fee includes:

- Admission to Keynote Speech and Designers' Forum
- One CD-ROM of conference proceedings
- One refreshment per break

The tutorial fee includes:

- Admission to full-day or half-day tutorial(s)
- One copy of all tutorial texts
- One lunch coupon
- One refreshment per break

PAYMENT

All registration fees must be paid in Japanese yen by bank remittance or credit card. Please note that personal checks and bank drafts will not be accepted.

Bank Remittance

Please remit the appropriate amount to the following bank account.

Bank Name: **SUMITOMO MITSUI BANKING CORPORATION**
(The Mitsui Sumitomo Bank)
Marunouchi Branch
SWIFT Code: **SMBCJPJT**
Account Title: **ASP-DAC 2011 Kunihiro Asada**
Account No.: **6583544** (Ordinary)

Credit Card

The following credit cards will be accepted:

VISA, MasterCard

CANCELLATION AND REFUND

When written notification of cancellation is received by the conference secretariat by December 17, 2010, 5,000 yen will be deducted from the fees paid to cover administrative costs. No refunds will be made for cancellation requests received after this date. Speakers are not allowed to cancel registrations.

REGISTRATION HOURS

Tuesday,	January 25:	8:00 – 18:00
Wednesday,	January 26:	7:00 – 17:00
Thursday,	January 27:	7:30 – 17:00
Friday,	January 28:	7:30 – 17:00

Advance Registration Deadline: Dec. 17th, 2010

ASP-DAC 2011 SECRETARIAT
Japan Electronics Show Association
12F Ote Center Bldg.,
1-1-3 Otemachi, Chiyoda-ku, Tokyo 100-0004 Japan
Phone: +81-3-6212-5231 Fax: +81-3-6212-5225
E-mail: aspdac2011@aspdac.com

ASP-DAC 2011 Registration Form

Registrant: ( )Prof. ( )Dr. ( )Mr. ( )Ms. (Please choose one.)

Family name:_____ First name:_____

Other name:_____

Affiliation:_____

Mailstop: _____

Dept./Div.: _____

Mailing address:_____ City:_____

State:_____ Zip:_____ Country:_____

Phone:_____ Fax:_____

E-mail:_____

Membership: ( )IEICE ( )IPSJ ( )ACM SIGDA ( )IEEE ( )Non-member

Member code:_____

Tutorial:
(Please choose one Full-Day topic or one/two Half-Day topics. If you choose two Half-Day topics, please choose Morning Tutorial (Tutorial 1 or 3) and Afternoon Tutorial (Tutorial 2 or 4)).

( ) Tutorial 1 (Half-Day): Advanced CMOS Device Technologies (1)

( ) Tutorial 2 (Half-Day): Advanced CMOS Device Technologies (2)

( ) Tutorial 3 (Half-Day): 3D Integration (1)

( ) Tutorial 4 (Half-Day): 3D Integration (2)

( ) Tutorial 5 (Full-Day): Post Silicon Debug

( ) Tutorial 6 (Full-Day): MPSoC: Multiprocessor System on Chip

"Student Group" discount is applied to a group of four or more students from the same affiliation (faculty or graduate school). One person should be chosen as a leader of the group. Please identify if you are the leader of the group or a member in the below.

☐ **leader** ☐ **member**

If you are the leader for your group (checked leader in Student Group), ASP-DAC 2011Secretariat will ask you to submit a member list to confirm your members' registration later. After you receive an excel format file for the member list, please fill it out and send it back to **aspdac2011@aspdac.com**.

Registration Fee & Payment Method

Category	By Dec.17 '10	After Dec.18 '10	Total
[Conference]			
Member	53,000 yen	58,000 yen	¥_____
Non-member	63,000 yen	68,000 yen	¥_____
Full-time Student	33,000 yen	38,000 yen	¥_____
[Keynotes + Designers' Forum]			
	23,000 yen	28,000 yen	¥_____
[Tutorial] (Full-Day or two Half-Days)			
Member	32,000 yen	37,000 yen	¥_____
Non-member	38,000 yen	42,000 yen	¥_____
Full-time Student	22,000 yen	25,000 yen	¥_____
Student Group	15,400 yen	17,500 yen	¥_____
[Tutorial] (Half-Day)			
Member	22,000 yen	26,000 yen	¥_____
Non-member	26,000 yen	30,000 yen	¥_____
Full-time Student	14,000 yen	16,000 yen	¥_____
Student Group	9,800 yen	11,200 yen	¥_____
		Grand Total	¥_____

( ) BANK TRANSFER:

I remitted or will remit a grand total of _____ yen on _____ (date/month/year)

through my bank named _____ to the following account:

Name of Bank: **SUMITOMO MITSUI BANKING CORPORATION**
(The Mitsui Sumitomo Bank)
Marunouchi Branch
SWIFT Code: **SMBCJPJT**
Account Title: **ASP-DAC 2011 Kunihiro Asada**
Account No.: **6583544** (Ordinary)

( ) CREDIT CARD:

( )VISA ( )MasterCard

Amount to be paid: _____ yen

Card No.:_____- _____- _____- _____

Exp. Date: ____/_____(month/year)

Cardholder's name: _____

Authorized Signature:

Date: _____**Signature:**_____

Invoices and Receipts

Invoice Required? ( )Yes ( ) No

If you replied "Yes," and you would like the invoice to be sent to a different address from that of your registration, please input the address below.

Invoice to (name): _____

Address: _____

Receipt Required? ( )Yes ( ) No

If you replied "Yes," and you would like the receipt to be sent to a different address from that of your registration, please input the address below.

Receipt to (name): _____

Address: _____

Note:

1. All payments must be in Japanese yen.
2. Bank drafts and personal checks will not be accepted.
3. If paying by credit card, please visit the Online Registration page (http://www.aspdac.com/) or send this form by post mail.
4. The remitter's name should be the same as the registrant's name.
5. If paying by bank transfer using your company's name, please advise us of the ID#, registrant's name, and transfer date (the day you transfer the fees) by e-mail to

   aspdac2011@aspdac.com or by Fax at **+81-3-6212-5225**. If you don't advise us above information within a week after you transfer the fee, we can't confirm your payment.
6. Handling fees and other bank transfer fees are to be borne by the registrant.
7. If payment of the registration fee is unremitted, or the credit card charge cannot be authorized, please go to the accounting desk.
8. If registered contents are changed or added, please notify the ASP-DAC 2011 Secretariat by e-mail at

   aspdac2011@aspdac.com or by Fax at **+81-3-6212-5225**. (Please be sure to specify your ID#.)
9. Cancellation and Refund.
   When you cancel this registration by December 17, regardless of reason, in refund, 5,000 yen will be deducted from the fees paid to cover administrate cost. No refund will be made for cancellation request received after this date.
10. Speakers are not allowed to cancel registrations.

Attendee Survey

1. Which category best describes your work? (choose one only)

   ( ) System or LSI Design
   ( ) Research and Development of EDA Tools
   ( ) Design Methodology
   ( ) Marketing/Sales
   ( ) Management
   ( ) Research/Education in an Academic Institution
   ( ) Student
   ( ) Other

2. Which area do you primarily work in? (pick all that apply)

   ( ) System Level ( ) Logic/Behavioral Level ( ) Circuit Level
   ( ) Layout Level ( ) Process Technology Level

   ( ) Design ( ) Design Methodology/Tool environment
   ( ) Synthesis/Optimization ( ) Verification
   ( ) Test

   ( ) Embedded System ( ) Low Power
   ( ) Timing and Signal Integrity ( ) Power Supply and Heat
   ( ) Analog, RF, Mixed Signal ( ) System-level Integration, SIP
   ( ) Other

3. What is your primary motivation/interest for attending ASP-DAC? (pick all that apply)

   ( ) I am a speaker at the conference
   ( ) I want to learn about EDA in general
   ( ) I want to learn more about the basics of EDA
   ( ) I want to learn more about advances in theory
   ( ) I want to learn more about practical application of EDA
   ( ) I have interest in Keynote speakers
   ( ) I have interest in specific technical presentation(s)
   ( ) I have interest in Special Sessions and Designers' Forum
   ( ) I have interest in the technical program as a whole
   ( ) I have interest in networking and social interaction opportunities
   ( ) Other

4. How did you learn about ASP-DAC? (choose the two most significant factors)

   ( ) ASP-DAC Web Site
   ( ) E-mail
   ( ) Previous Attendance
   ( ) Colleague/Advisor
   ( ) I have paper presentation at the conference
   ( ) Other

Information

Proceedings:

ASP-DAC 2011 will be producing a CD-ROM version of the ASP-DAC 2011 Proceedings. Conference registration in any of the categories will include it. Additional Proceedings will be available for purchase at the Conference. Price is as follows:
CD-ROM: 2,000 yen;

Banquet:

Conference registrants are invited to attend a banquet to be held on January 27, 2011. The banquet will be held from 19:00 to 21:00 at the fifth floor of conference center. Regular Member and Non-member Conference registrants receive a ticket to the banquet when they register at the conference. Full-time students, Designers' Forum-only registrants, and Tutorial-only registrants wishing to attend the banquet will be required to pay 5,000 yen for a ticket when they register on site.

Visa Application:

Without a legal visa, foreign participants may be denied entry into Japan. Please contact your nearest Japanese embassy in order to ensure entry. Notice that the ASP-DAC 2011 Organizing Committee issues the invitation letters and supports the VISA applications only for presenters of the conference papers. All the other attendees have to apply for VISA through their travel agents or by yourself. In some cases it may take two months to obtain a legal visa. The following Web page of Japanese embassy may be helpful.
http://www.mofa.go.jp/j_info/visit/visa/

Insurance:

The organizer cannot accept responsibility for accidents which might occur. Delegates are encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home country prior to departure.

Climate:

The temperature in Yokohama during the period of the Conference ranges between 5°C and 12°C.

Currency Exchange:

Only Japanese Yen(¥) is accepted at ordinary stores and restaurants. Certain foreign currencies may be accepted at a limited number of hotels, restaurants and souvenir shops. You can exchange your currency for Japanese Yen at foreign exchange banks and other authorized money exchange offices with your passport.

Electrical Appliances:

Electrical appliances are supplied on 100 volts in Japan. The frequency is 50 Hz in eastern Japan including Tokyo, Yokohama and 60 Hz in western Japan including Kyoto and Osaka.

Shopping:

The business hours of most department stores are from 10:00 to 20:00. They are open on Sundays and national holidays, but may close on some weekday. Business hours of retail shops differ from one another, but most shops operate from 10:00 to 20:00. Shops are open on Sundays and national holidays.

Sightseeing:

http://www.city.yokohama.jp/ne/info/hotspotE.html

Participants can get sightseeing information at the Travel desk in the Conference site during the Conference period.

CHINA TOWN
Being the largest Chinese settlement in Japan, Chinatown is always alive with people who come to enjoy Chinese food. It is also a fun place for shopping or just walking around its many streets and alleys lined with colorful restaurants, shops overflowing with Chinese goods and stores that sell exotic ingredients and Chinese medicines.

LANDMARK TOWER
296 meters high with 70 stories above ground and three levels underground. It is Japan's tallest skyscraper. A 40-second ride on the world's fastest elevator skyrockets you to the 69th floor's Sky Garden, the highest observatory in Japan.
Hours: 10:00-21:00 Admission: ¥1,000
Access: 3 min. walk from Minato-mirai Station

SANKEIEN GARDEN
A purely Japanese-style landscape garden. Accenting the main garden is an impressive three-story pagoda and graceful garden bridges. Inside contains several old houses and farm buildings as well as Important Cultural Properties such as Rinshunkaku Villa and Chosukaku House.
Hours:9:00-16:30 Admission:¥500
Access: From Sakuragicho Sta., take Bus No. 8 or No. 125 to Honmoku-Sankeien-mae.

MARITIME MUSEUM
The site of the previous Nippon Maru, the former training ship for Japan's Maritime Defense Force. The Yokohama Maritime Museum, which specializes in ports and ships, is located next to the Nippon Maru.
Hours: 10:00-17:00 (Closed Monday) Admission: ¥600
Access: 5 min. walk from Minato-mirai Station

Other Information:

JAPAN NATIONAL TOURISM ORGANIZATION
http://www.jnto.go.jp/
YOKOHAMA CONVENTION & VISITORS BUREAU
http://www.welcome.city.yokohama.jp/eng/tourism/
NARITA AIRPORT
http://www.narita-airport.jp/en/
HANEDA AIRPORT
http://www.haneda-airport.jp/en/
YES ! TOKYO
http://tcvb.or.jp/en/

Accommodations

OFFICIAL TRAVEL AGENT

JTB Yokohama Convention Center has been appointed as the official travel agent. Inquiries and applications concerning arrangements should be addressed to:

JTB Tokyo Metropolitan Corp.
JTB Yokohama Convention Center
Address: Dai-6-Yasuda Bldg. 6F, 3-29-1 Tsuruya-cho,
Kanagawa-ku, Yokohama 221-0835, Japan
Phone: +81-45-316-4602 Fax:+81-45-316-5701
e-mail: jtb_convention@met.jtb.jp
Person in charge: Cross (Mr.), Eda (Ms.), Himei (Mr.), and Hara (Ms.)

HOTEL RESERVATION

JTB Yokohama Convention Center has reserved blocks of rooms at hotels in Yokohama during the period. Please fill in the Hotel Reservation Form and submit it to JTB Yokohama Convention Center by 22th December, 2010, Japan time. Reservation will be made on a first-come, first-served basis. Please indicate your order of preference in the application form. If your desired hotel is fully booked, JTB Yokohama Convention Center will reserve your second choice or a hotel in the same grade. Hotel charge should be paid to JTB Yokohama Convention Center. When submitting the application, please indicate credit card number, expiry date and card holder's signature. Confirmation of hotel reservation will be sent by fax in 2 weeks or so. Hotel reservation will not be honored without this confirmation.

Cancellation of Hotel Reservation

In the event of cancellation, written notification should be sent to JTB Yokohama Convention Center. The following cancellation fees will be charged to your credit card.

Up to 9 days before the first night of stay	2,000yen
8 to 2 days before	20% of daily room charge (minimum 2,000yen)
one day before or after	100% of daily room charge
No notice given	100% of daily room charge

Hotels

#	Name/Address/Fee per Room per Night/Access
A	**Yokohama Grand Inter-Continental** 1-1-1 Minatomirai, Nishi-ku, Yokohama Tel: +81-45-223-2222, Fax: +81-45-221-0650 **S**:¥23,100, **SB**:¥24,150, **T**:¥21,800, **TB**:¥25,800 Adjacent to Pacifico
B	**Pan Pacific Hotel Yokohama** 2-3-7 Minatomirai, Nishi-ku, Yokohama Tel: +81-45-682-2222, Fax: +81-45-682-2223 From Jan. 23 to Jan. 27 **S**:¥16,800, **SB**:¥17,850, **T**:¥21,800, **TB**:¥25,800 Jan. 28 **S**:¥17,850, **SB**:¥18,900, **T**:¥21,800, **TB**:¥25,800 2 min. walk to Pacifico
C	**Yokohama Royal Park Hotel** 2-2-1-3 Minatomirai, Nishi-ku, Yokohama Tel: +81-45-221-1111, Fax: +81-45-224-5153 **SB**:¥21,500, **TB**:¥25,800 5 min. walk to Pacifico
D	**Nabios Yokohama** 2-1-1, Shinko, Naka-ku, Yokohama Tel: +81-45-633-6000, Fax: +81-45-633-6001 Sun–Thu: **S**:¥8,400, **SB**:¥9,450, **T**:¥15,750, **TB**:¥17,850 Fri : **S**:¥9,450, **SB**:¥10,500, **T**:¥17,850, **TB**:¥19,950 7 min. walk to Pacifico
E	**Yokohama Sakuragicho Washington Hotel** 1-1-67, Sakuragi-cho, Naka-ku, Yokohama Tel: +81-45-683-3111, Fax: +81-45-683-3112 Jan. 24 **S**:¥10,500, **SB**:¥11,900, **T**:¥15,400, **TB**:¥18,200 From Jan. 25 to Jan. 28 **S**:¥10,500, **SB**:¥11,760, **T**:¥17,000, **TB**:¥19,800 8 min. walk to Pacifico
F	**Hotel Camelot Japan** 1-11-3, Kita-saiwai, Nishi-ku, Yokohama Tel: +81-45-312-2111, Fax: +81-45-312-2143 **S**:¥9,100, **SB**:¥10,300, **T**:¥14,000, **TB**:¥16,400 30 min. walk to Pacifico

∗ S = Single, SB = Single with breakfast, T = Twin, TB = Twin with breakfast.
Note: Room charge includes service charge and 5% tax.

Hotel Reservation Form

ASP-DAC 2011

January 25 - 28, 2011, Yokohama Japan

Please complete and return this form to:
JTB Tokyo Metropolitan Corp.
JTB Yokohama Convention Center
Address: Dai-6-Yasuda Bldg. 6F, 3-29-1 Tsuruya-cho,
Kanagawa-ku, Yokohama 221-0835, Japan
Phone: +81-45-316-4602 Fax:+81-45-316-5701
e-mail: jtb_convention@met.jtb.jp

Deadline: Dec. 22, 2010, Japan time
Note: You should send this form by postal mail or fax when you apply.

(Please type or write in block letters.)
Full Name: ( )Prof. ( )Dr. ( )Mr. ( )Ms.

Family Name: _____, First Name: _____

Middle Initial: _____

Affiliation: _____

Mail Stop: _____

Dept./Div.: _____

Mailing Address: _____

City: _____ State: _____

Zip: _____ Country: _____

Phone:_____ Fax:_____

E-mail: _____

Please remember to include your country and/or city code for Phone/Fax numbers.

Name of Accompanying Person(s), Family Member(s) if any:
( )Mr. ( )Ms.

Family Name: _____, First Name:_____

Middle Initial: _____

Arrival Schedule:

Arriving at _____(airport) on _____(date)

by _____(flight number)

Hotel Accommodations:

Please select 2 hotels in order of preference and enter the name of the hotel and the hotel number(see hotel list in this program).

1st choice:_____(No.)

2nd choice:_____(No.)

Room Choice: ( )Single ( )Twin

Breakfast: ( )Yes ( )No

Period of Stay: Check-in _____Check-out _____for _____ nights

Guarantee of Booking:

Credit Card: ( )VISA ( )Master Card

Card Number: _____- _____- _____- _____

Card Holder's Name : _____

Expiration Date: ____/_____(month/year)

Authorized Signature: _____

Access to Pacifico Yokohama

●Traffic Information — March, 2005

By Train

- Shibuya Sta. — Tokyu Toyoko Line : Limited Express (Direct link to Minato Mirai Line) → Yokohama Sta. → 30min. → Minato Mirai Sta. → on foot 3min. → PACIFICO YOKOHAMA
- Shinjuku Sta. — JR Shonan Shinjuku Line 29min. → Yokohama Sta. → Minato Mirai Line 3min. (Connecting from Tokyu Toyoko Line) → Minato Mirai Sta. (Take Queen's Square Yokohama Exit and go upto 2nd Floor with Red Escalator) → PACIFICO YOKOHAMA

By Train & Shinkansen

- Tokyo Sta. — JR Tokaido Line 25min. → Yokohama Sta. → by Taxi 7min. (From taxi pool at 2nd basement of Porta shopping mall on the east exit) → PACIFICO YOKOHAMA
- Shinagawa Sta. — Keikyu Express : Limited Express 15min. → Yokohama Sta. → by Taxi 7min. (From taxi pool at 2nd basement of Porta shopping mall on the east exit) → PACIFICO YOKOHAMA
- Shin Yokohama Sta. — JR Yokohama Line 3min. → Kikuna Sta. → Tokyu Toyoko Line 6min (Connecting to Minato Mirai Line 10min. to Minato Mirai Sta.) → Yokohama Sta. → JR Keihin-Tohoku Line 3min. → Sakuragicho Sta. → on foot 12min. → PACIFICO YOKOHAMA
  - JR Yokohama Line 15min. (Change to Keihin-Tohoku Line at Higashikanagawa-Sta.) → Sakuragicho Sta. → by Bus 7min. (From bus stop #1) → PACIFICO YOKOHAMA
  - Yokohama Subway 15min. → Sakuragicho Sta. → by Taxi 5min. → PACIFICO YOKOHAMA

By Air

- Narita Airport — JR Narita Express 90min. → Yokohama Sta. → Minato Mirai Line 3min. (Connecting from Tokyu Toyoko Line) → Minato Mirai Sta. (Take Queen's Square Yokohama Exit and go upto 2nd Floor with Red Escalator) → on foot 3min. → PACIFICO YOKOHAMA
  - Airport Limousine Bus 90min. (120min. for PACIFICO YOKOHAMA) → PACIFICO YOKOHAMA
- Haneda Airport — Keikyu Express 24min. → YCAT Yokohama City Air Terminal Yokohama St. East. → by Taxi 7min. (From taxi pool at 2nd basement of Porta shopping mall on the east exit) → PACIFICO YOKOHAMA
  - Airport Limousine Bus 30min. → YCAT Yokohama City Air Terminal Yokohama St. East. → PACIFICO YOKOHAMA

■Driving To Pacifico

[From Tokyo]

- Metropolitan Expressway — Toward Yokohama Park, Yokohane Route ▸▸▸ Minato Mirai Ramp,3min. ▸▸▸ PACIFICO YOKOHAMA
- Metropolitan Expressway — Toward Yokohama (over Bay bridge), Wangan Route ▸▸▸ Minato Mirai Ramp,3min. ▸▸▸ PACIFICO YOKOHAMA

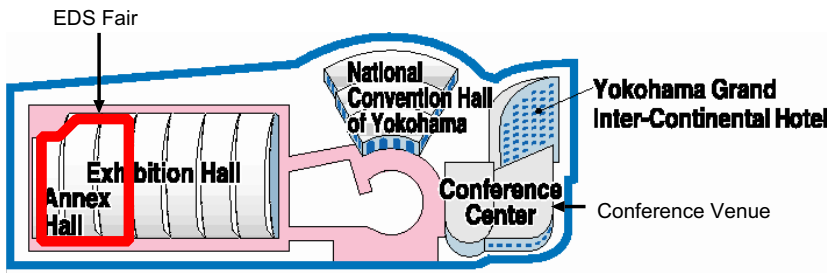
[From Kansai or Chubu]

- Tomei Expressway Yokohama Machida IC — Hodogaya Bypass,20min. ▸ Kariba IC ▸ Toward Yokohama,Metropolitan Expressway,Kariba Route,10min. Minato Mirai Ramp,3min ▸ PACIFICO YOKOHAMA

■Parking Lot

Minato Mirai Public Parking Lot +81-45-221-1301	Capacity:1,200 (Standard-sized cars only)	Open 24 hours	Rates:Standard-sized car 260yen/30min. (1,300yen for max. 15hours between 8 and 23 on weekdays.)
Bus/Large Vehicles Parking Lot +81-45-221-1302	Capacity:40	Open 24 hours	Rates:Large vehicle 500yen/30min.

- ASP-DAC Conference is held at “Conference Center.”
- EDS Fair 2011 is held at “Exhibition Hall/Annex Hall.” (2min. walk from Conference Center.)



Visit our web site
http://www.aspdac.com/

ASP-DAC 2011 SECRETARIAT
Japan Electronics Show Association
12F Ote Center Bldg.,
1-1-3 Otemachi, Chiyoda-ku, Tokyo 100-0004 Japan
Phone: +81-3-6212-5231 Fax: +81-3-6212-5225
E-mail: aspdac2011@aspdac.com