Signal Integrity Modeling and Measurement of TSV in 3D IC

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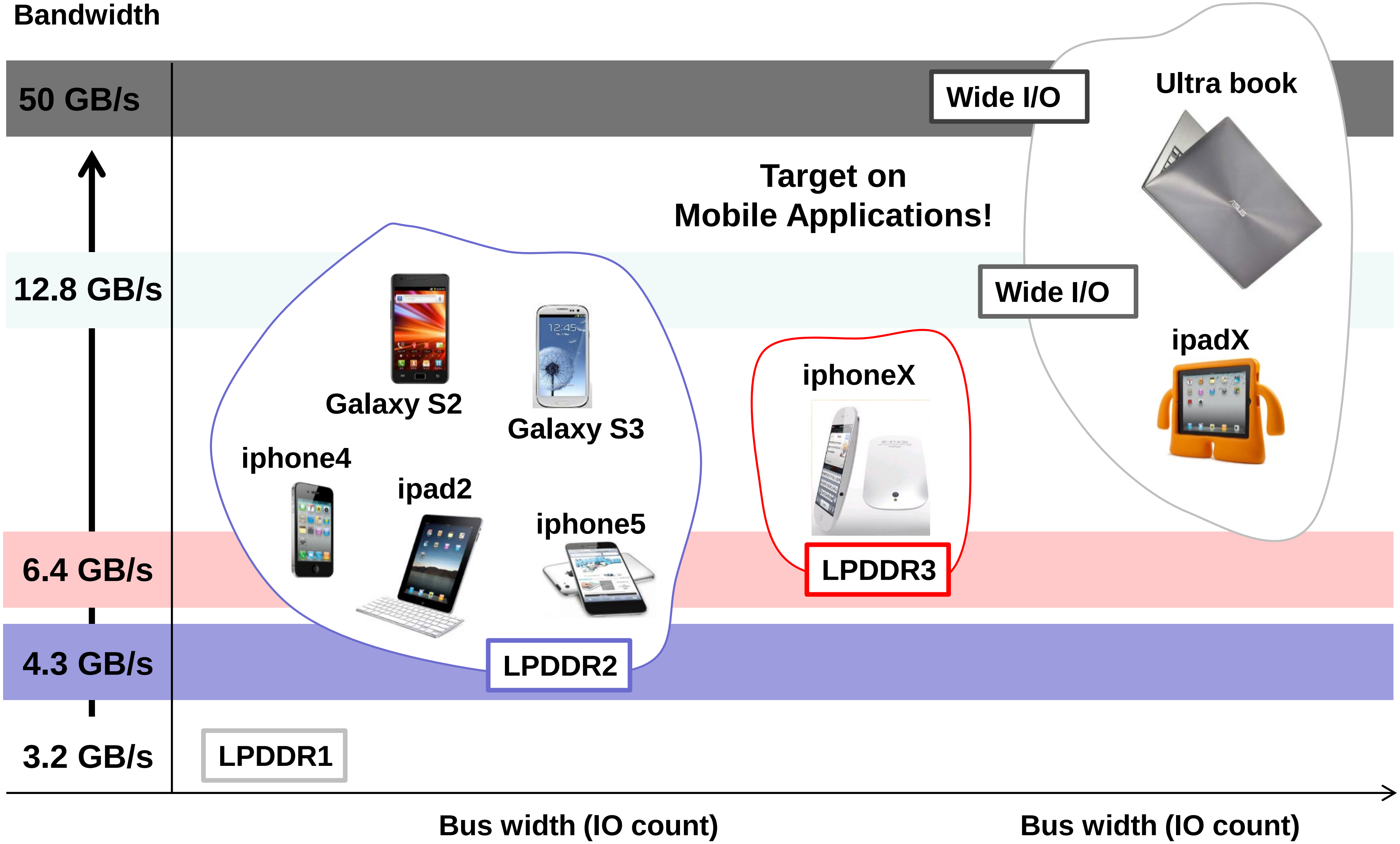
Contents

Semiconductor Requirements for Smart Mobile Applications

- Low power
- High performance
- Multi-function
- Small size
- Low cost

Mobile Application with Increasing I/O count and Bandwidth



Bandwidth

50 GB/s

12.8 GB/s

6.4 GB/s

4.3 GB/s

3.2 GB/s

LPDDR1

LPDDR2

LPDDR3

Wide I/O

Wide I/O

Galaxy S2

Galaxy S3

iphone4

ipad2

iphone5

iphoneX

Ultra book

ipadX

Target on
Mobile Applications!

Bus width (IO count)

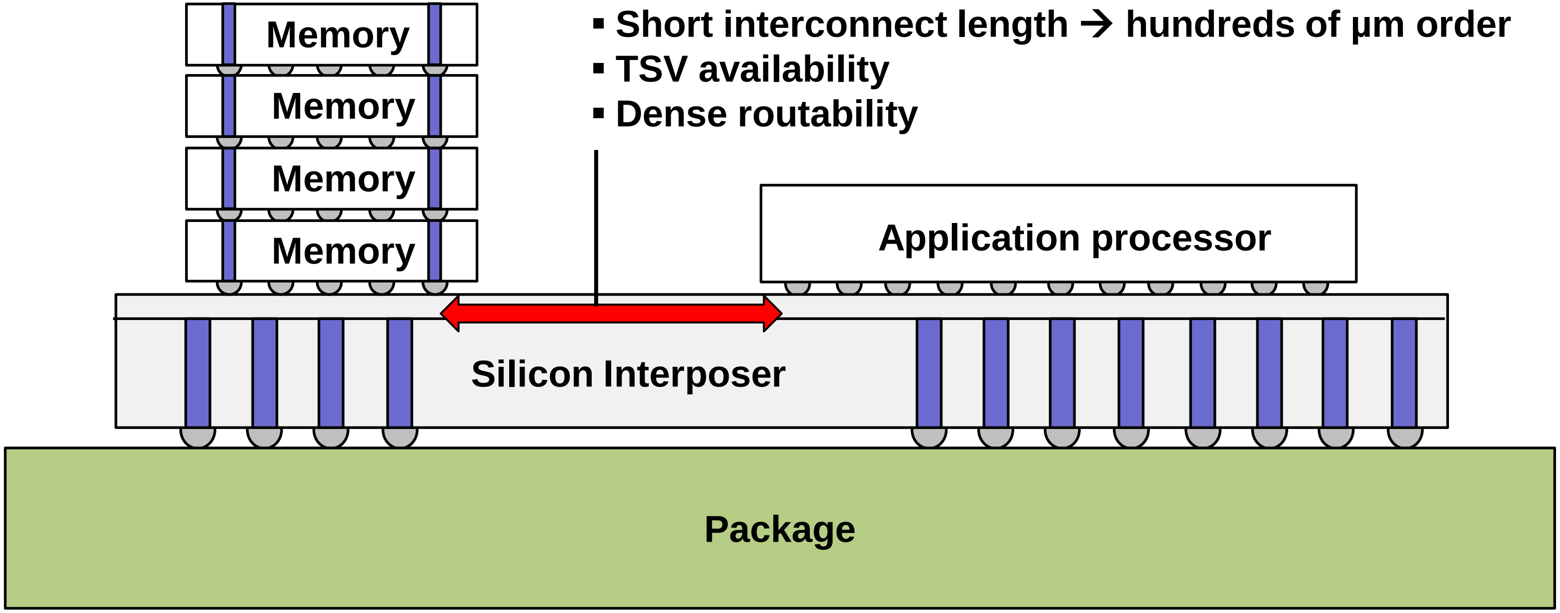
Bus width (IO count)

Why Interposer in Mobile Application?

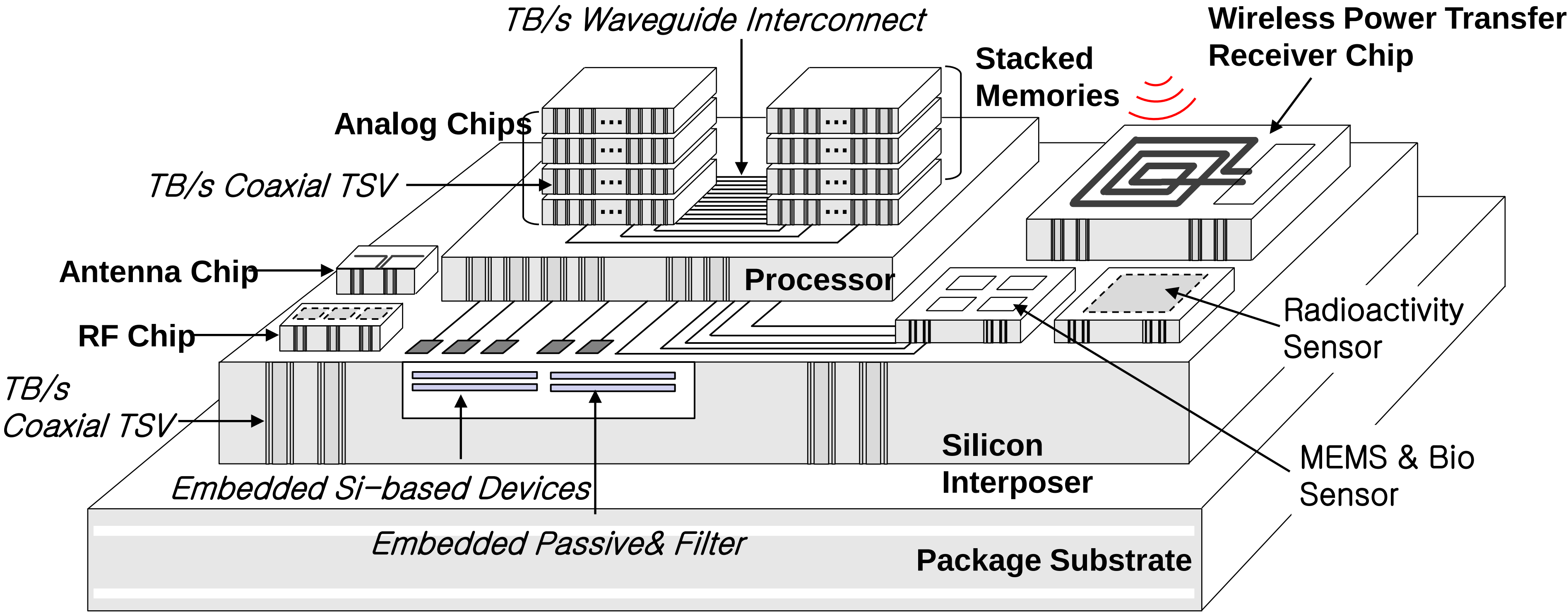
Mobile application requires

- **Faster computing**
- Higher resolution display
- **Longer battery life**
- Compact size

- **Large number of I/O count → 10K**
- **Low power consumption → reduced more than 50 %**
- **Short interconnect length → hundreds of μm order**
- **TSV availability**
- **Dense routability**

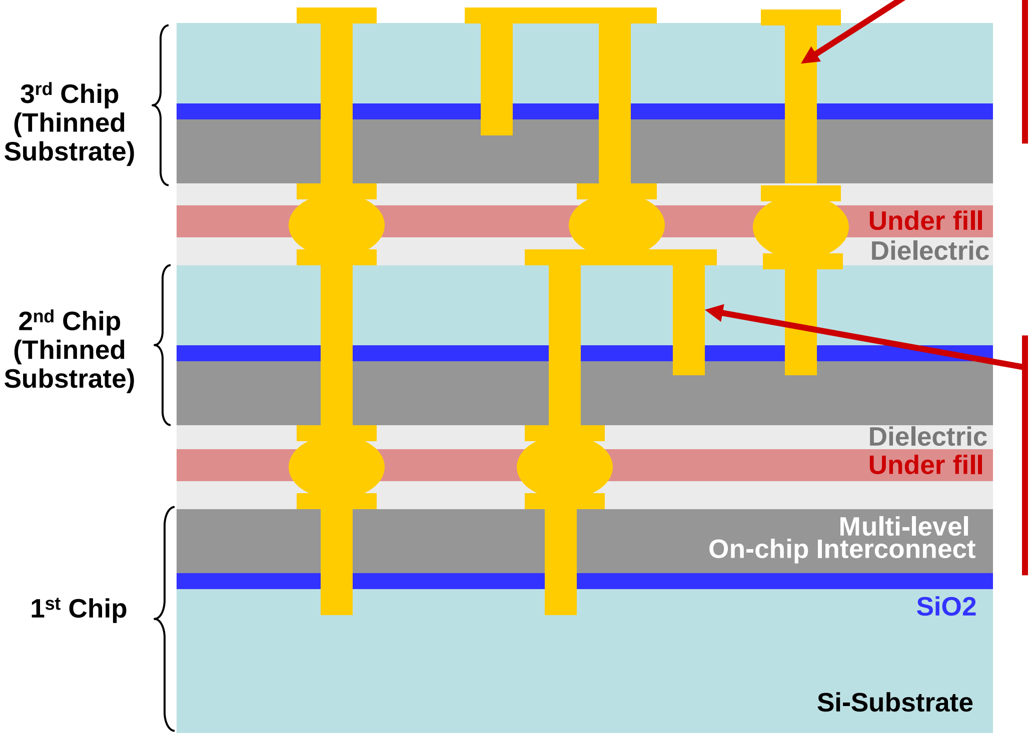


Low Power TB/s Bandwidth 3D IC Structure



- ✓ **Innovative new vertical & horizontal Interconnections for TB/s Bandwidth in 3D IC**
- ✓ **Low Power system using WPT chip**
- ✓ **Silicon Interposer Embedded Passive / Active Devices**

Key Technology : TSV (Through Silicon Via)

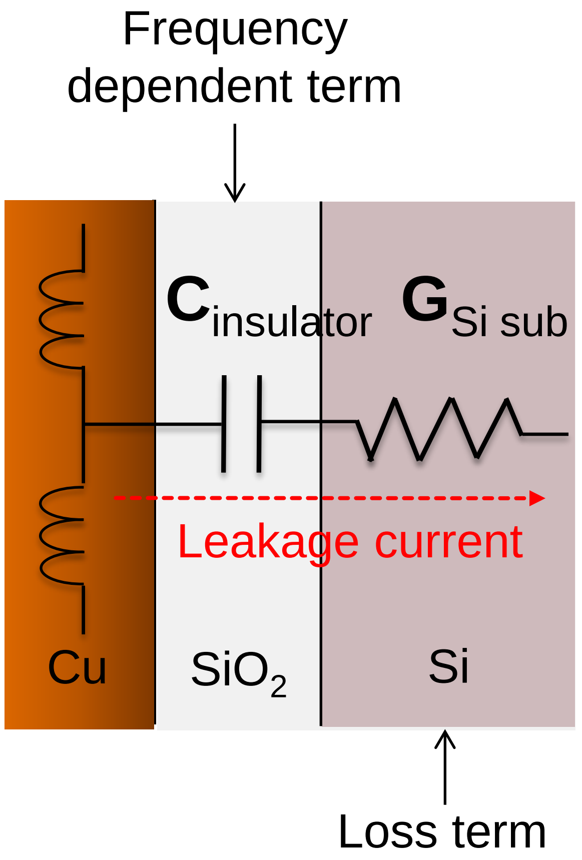


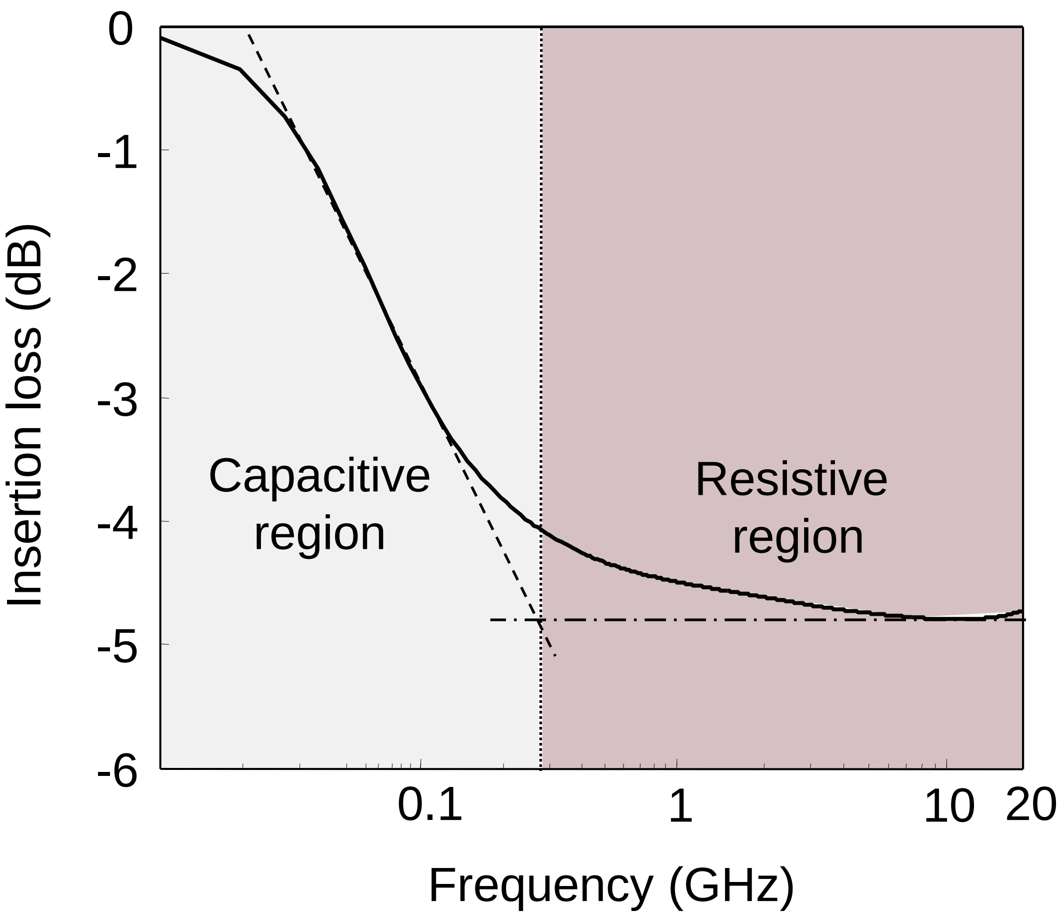
3D TSV Stacked IC

- **Short Interconnection**
  - → **Reduced RC Delays**
  - → **Low Impedance for Power Distribution Network**
  - → **Low Power Consumption**
  - → **Heat Dissipation Through Via**

- **No Space Limitation for Interconnection**
  - → **High Density Chip Wiring**
  - → **No Limitation of I/O Number**
  - → **No Limitation of I/O Pitch**
  - → **Small Area Package**

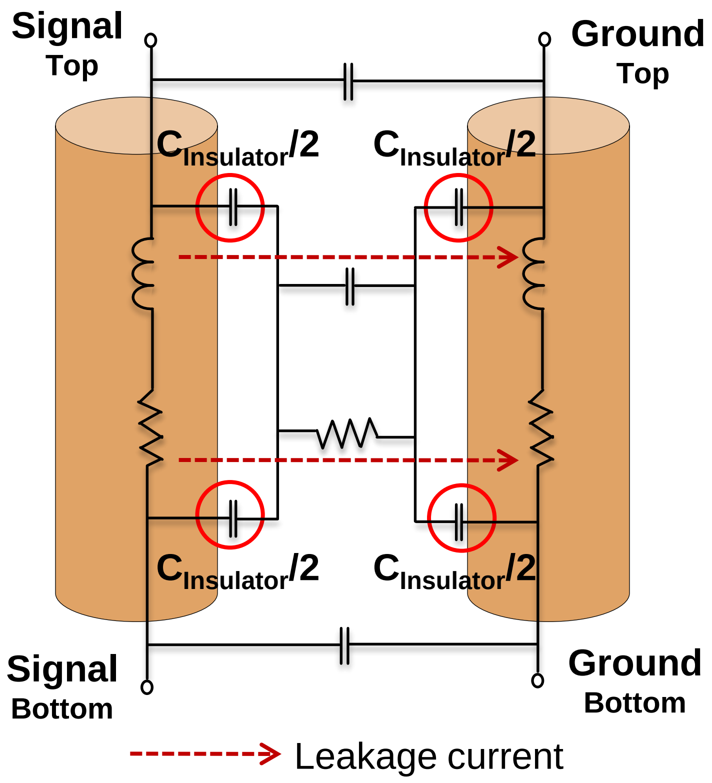
Frequency-dependent Loss of Through Silicon Via

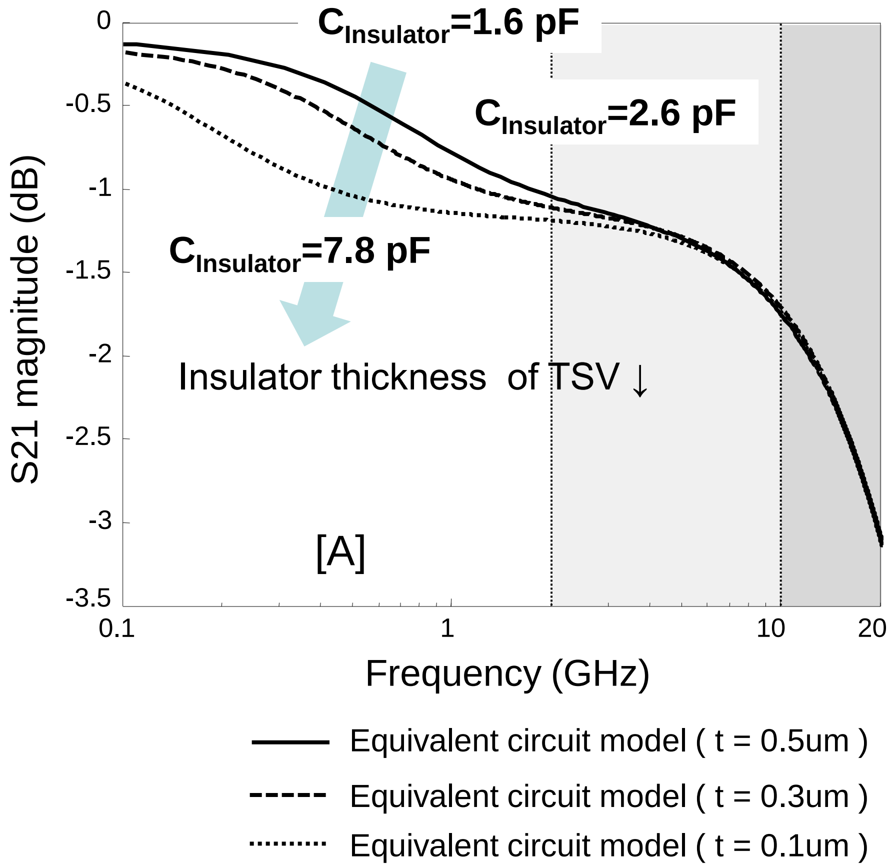




Analysis of a TSV Channel with Insulator Thickness of TSV

- Insulator thickness of TSV (t)

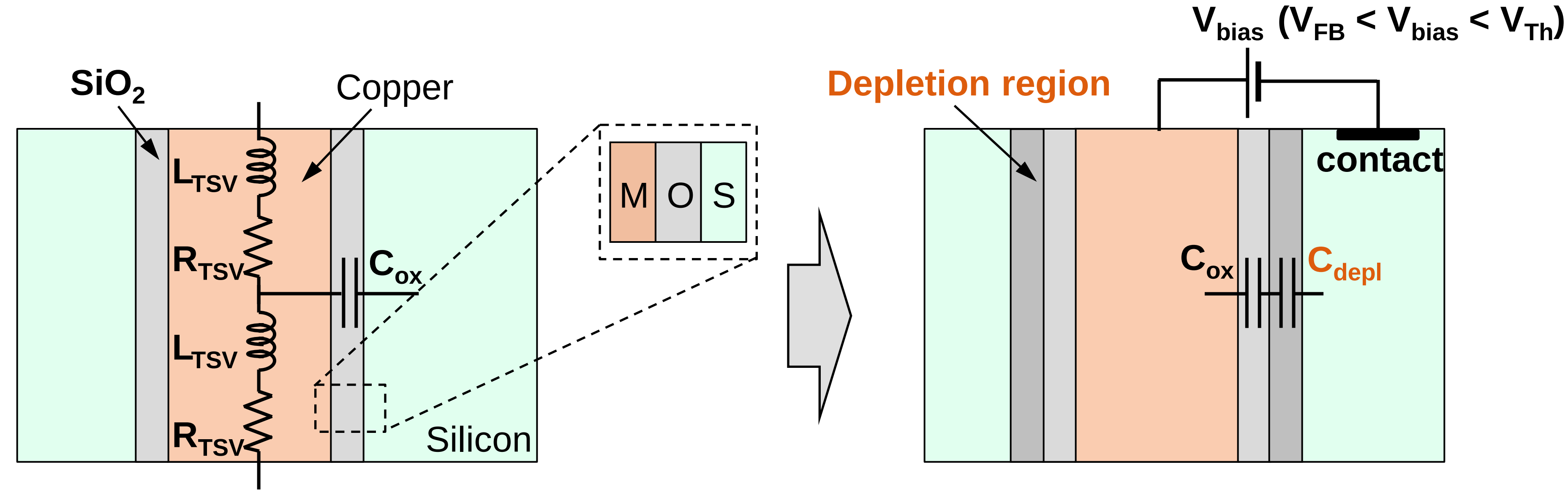




➔ Leakage through silicon substrate dominantly increases due to lowered impedance with increased $C_{insulator}$ in region [A].

➔ Insulator thickness dominantly affects frequency dependent loss of a TSV channel in region [A].

TSV Depletion Phenomenon Depending on DC Bias Voltage

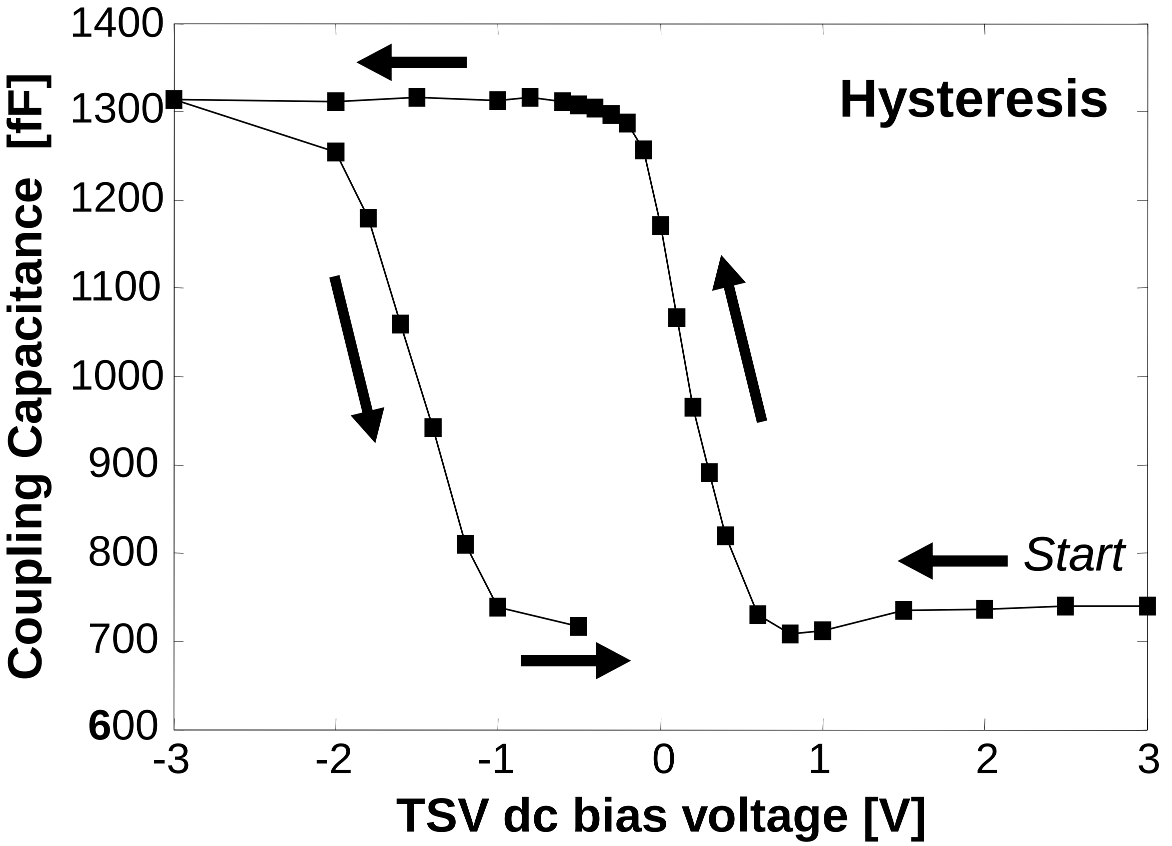


TSV model without considering depletion

$$C_{TSV} = \frac{C_{ox} \cdot C_{depl}}{C_{ox} + C_{depl}}$$

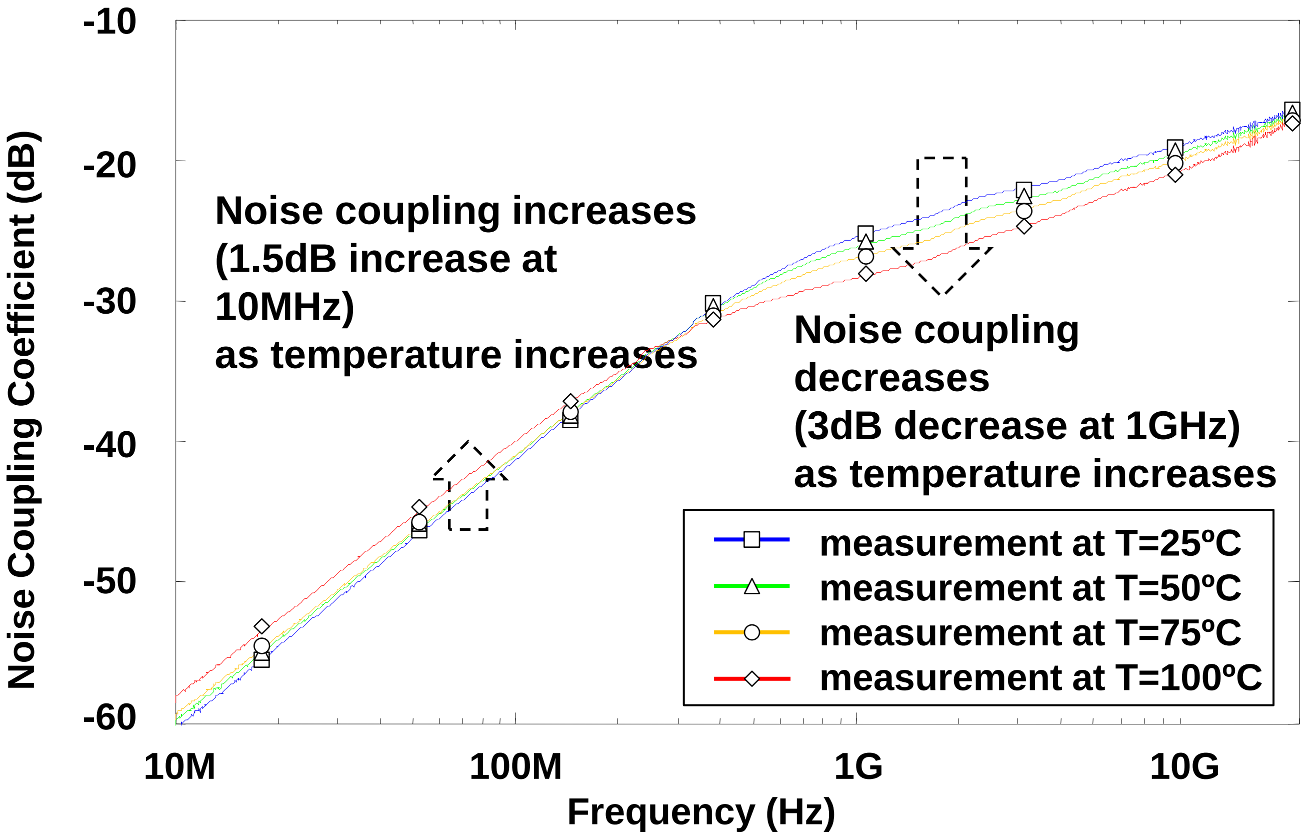
- **TSV has MOS structure → depletion occurs depending on TSV bias voltage**
- **TSV capacitance decreases if depletion region is generated**

Hysteresis of Depletion Capacitance



- **Coupling capacitance increases as TSV dc bias decreases**
- **Coupling capacitance shows hysteresis, which means that capacitance varies depending on the previous TSV dc bias voltage**

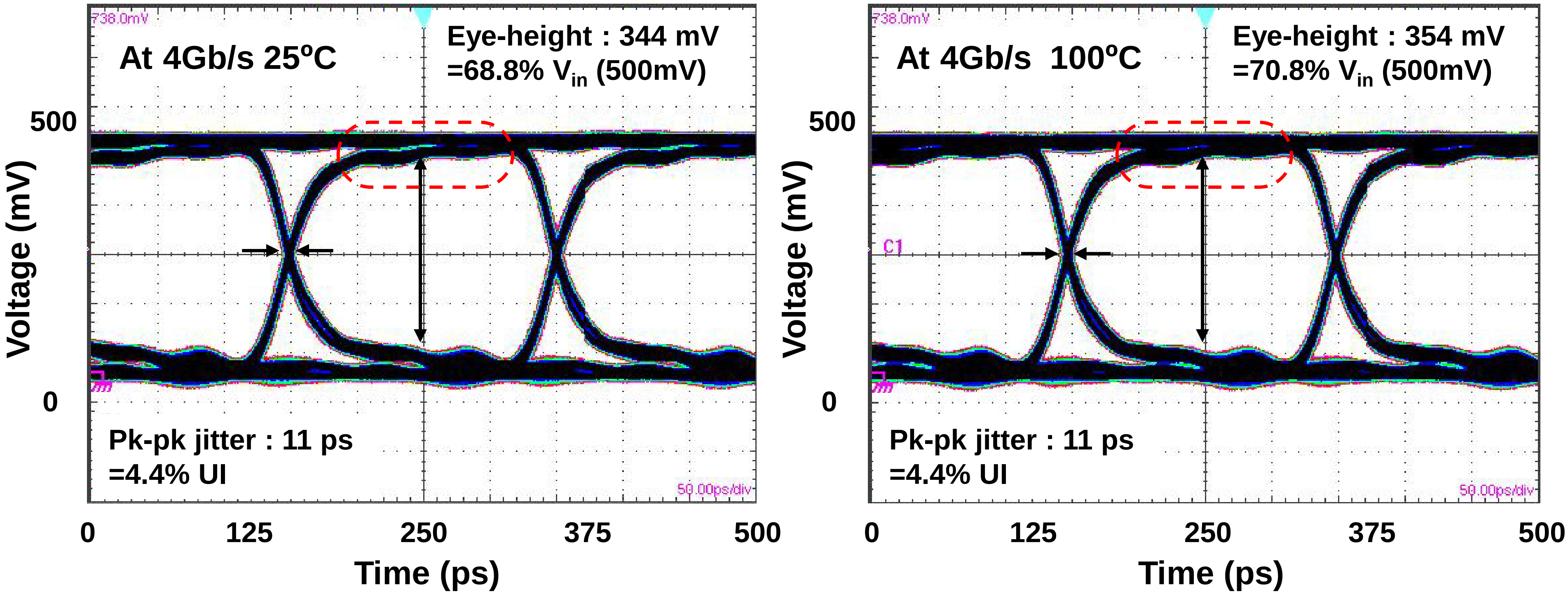
Frequency Domain Measurement Result



- Measurement shows trend reversion between high frequency and low frequency.

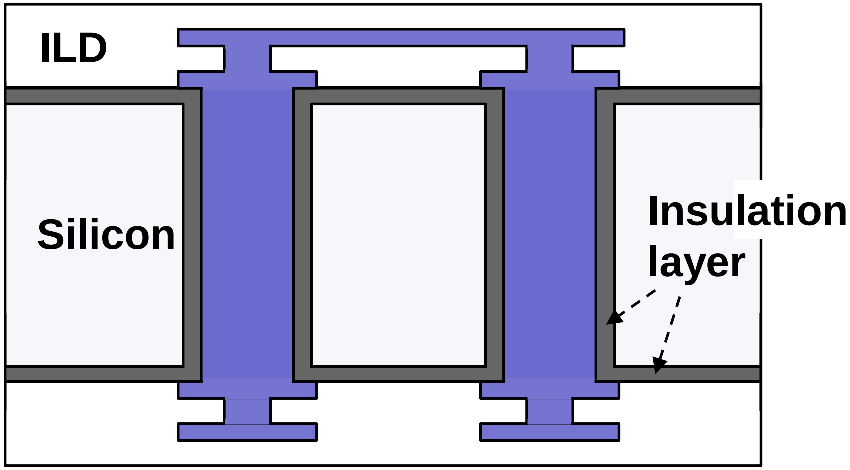
- At very high frequency, noise coupling becomes similar although temperature varies

Eye Diagram of 4Gbps at 25°C and 100°C

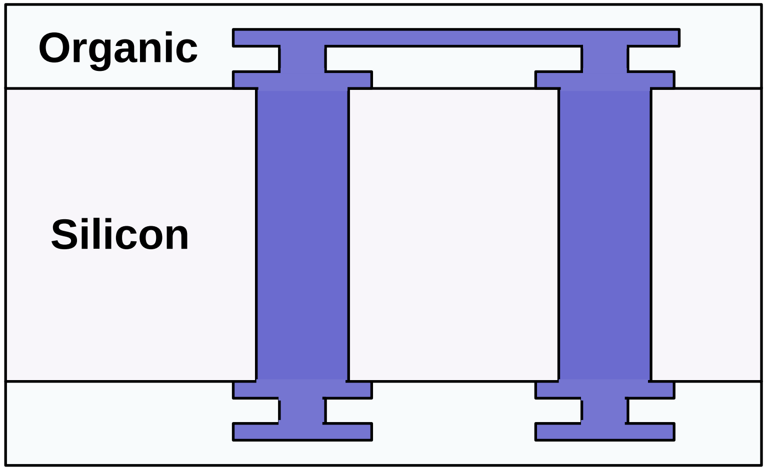


- Eye height increases about 2%
- At 4Gbps, trend is reversed compared with low frequency region
- Jitter is almost same

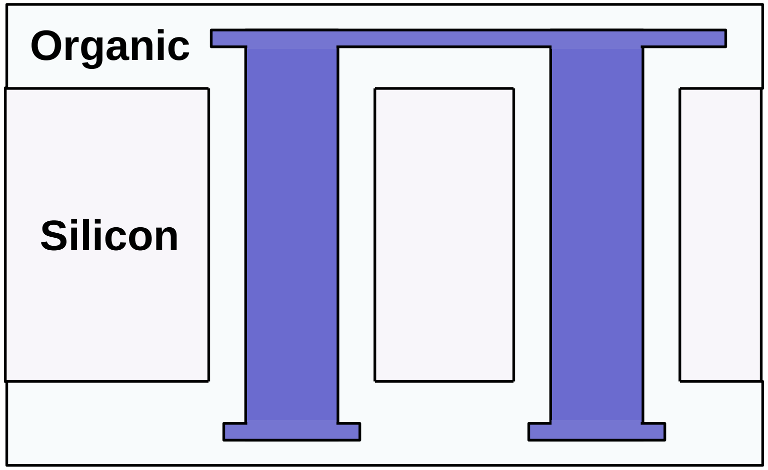
Various Structures of TSV on Interposer



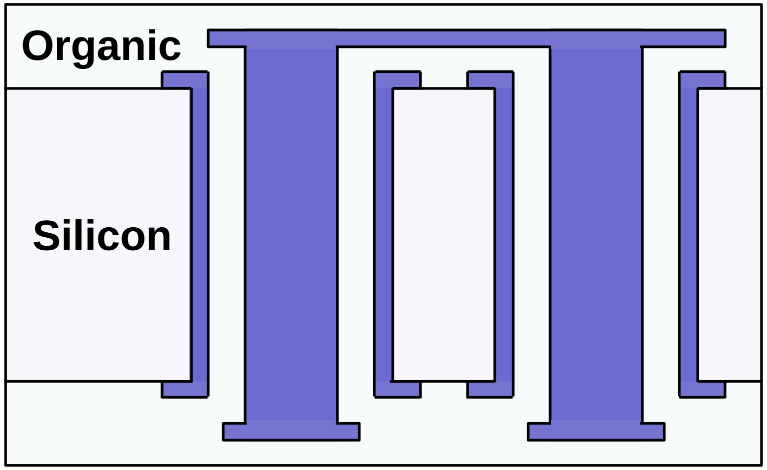
< Normal TSV >



< Through Silicon Line Via (TSLV) >



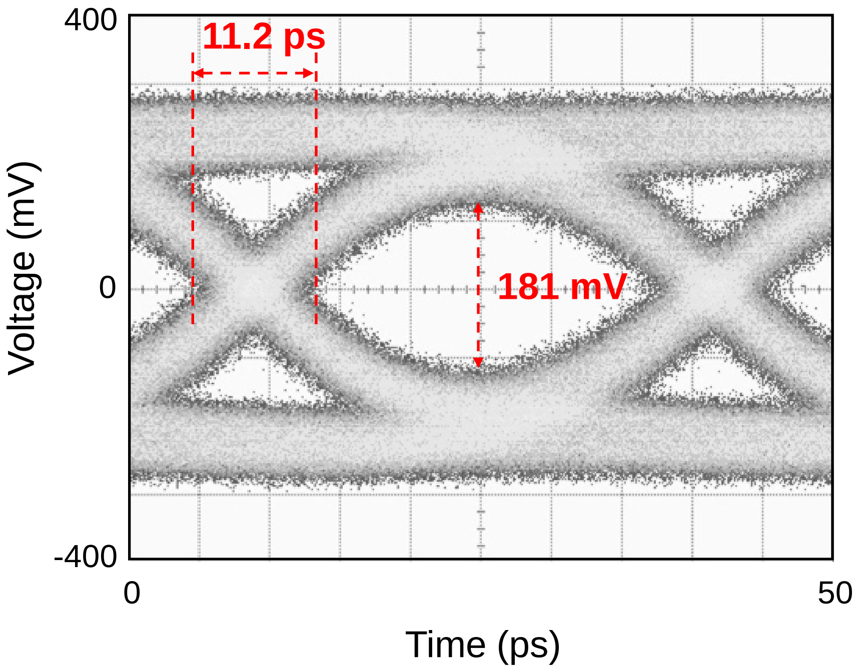
< Through Organic Line Via (TOLV) >



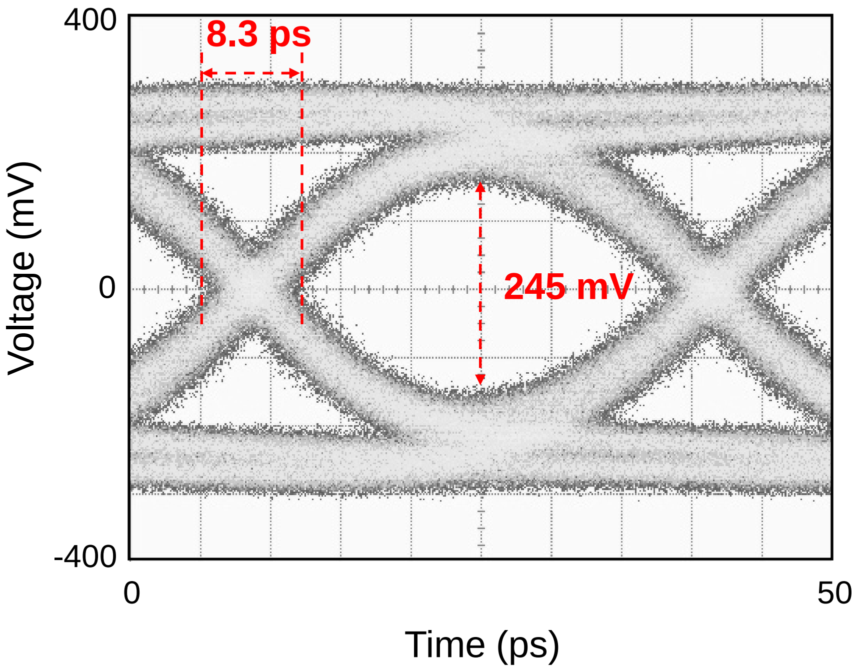
< Coaxial Organic Line Via (COLV) >

Measured Eye-diagrams at 30 Gbps (Coaxial TSV)

Data rate = 30 Gbps



< Eye-diagram of TSV channel >

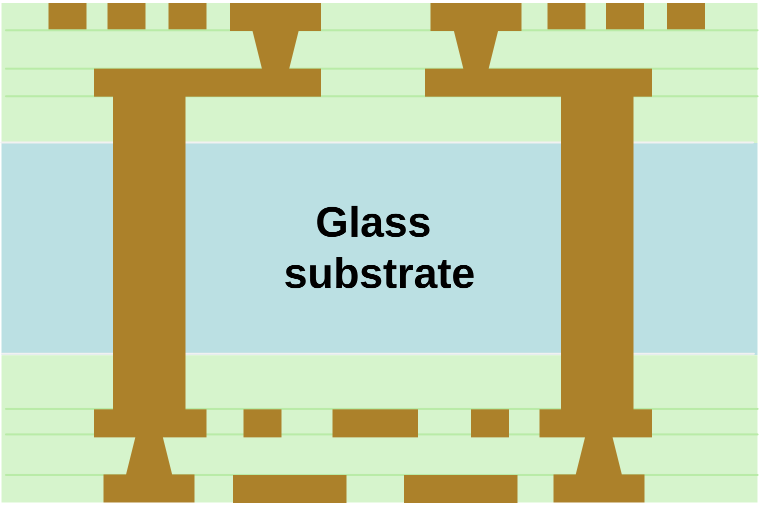


< Eye-diagram of Coaxial TSV channel >

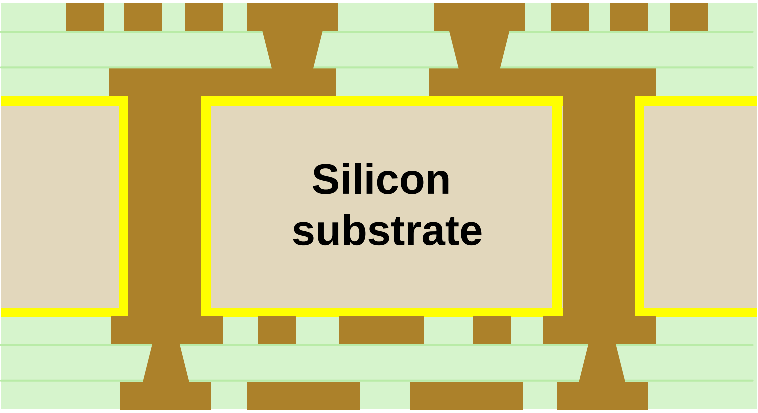
- **Eye-diagram of coaxial TSV channel is better than that of normal TSV channel**

Glass Interposer and TGV

< Double-sided Glass Interposer >



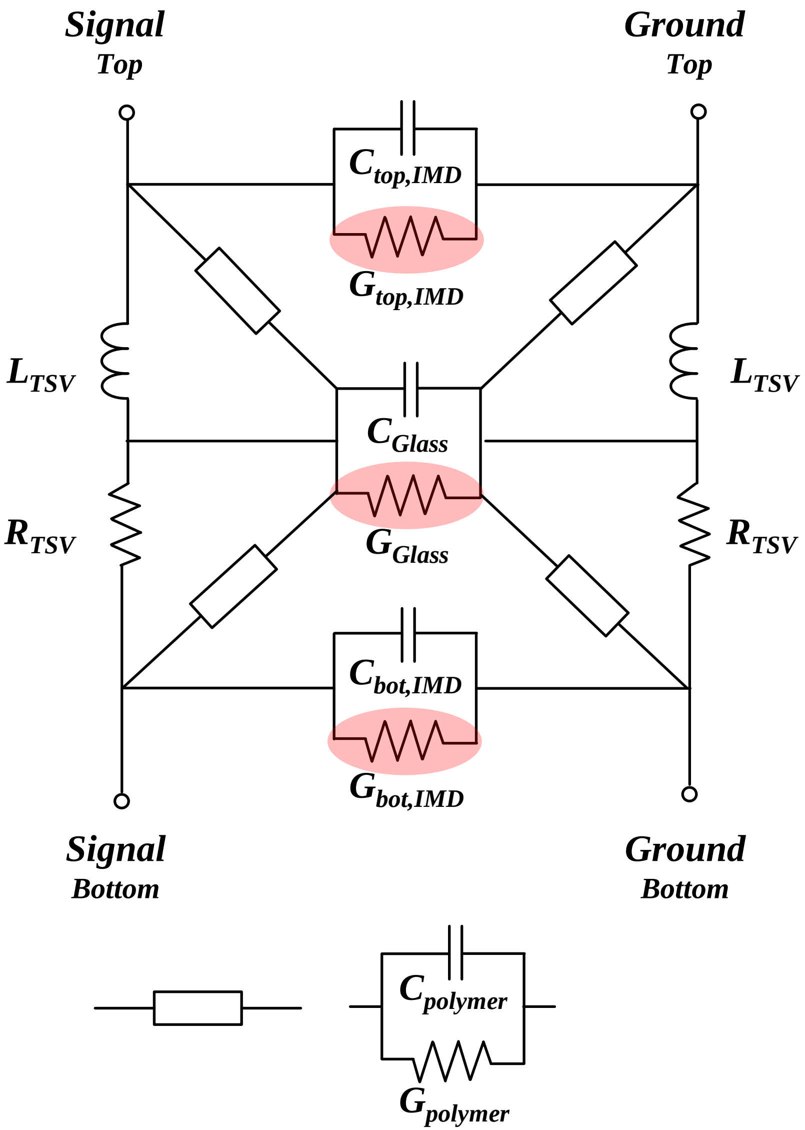
< Double-sided Silicon Interposer >



Physical parameters

- TGV/TSV diameter: 10µm
- TGV/TSV pitch: 40µm, 100µm
- TSV oxide thickness: 0.5µm

Equivalent Circuit Model of a Through Glass Via (TGV)



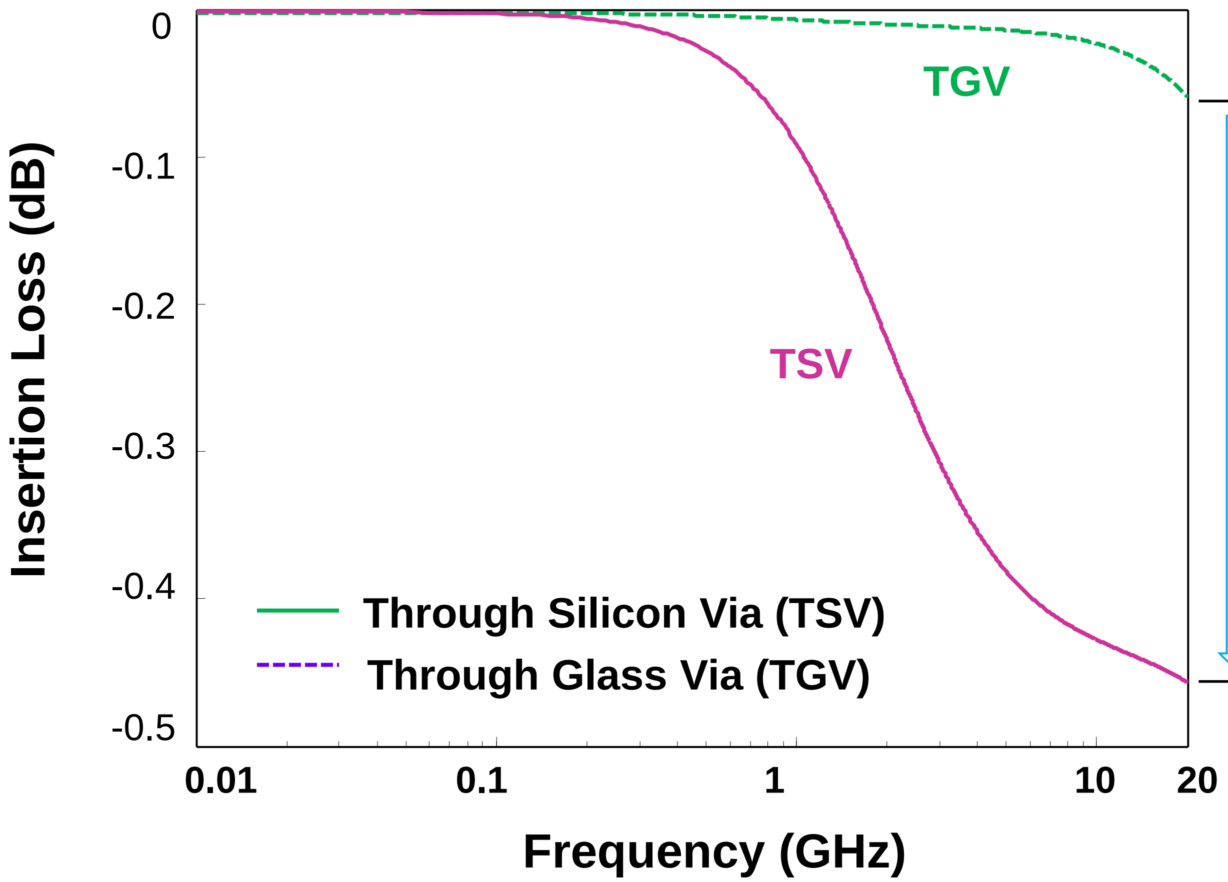
Physical parameters

d_{TSV} = 10 µm
p_{TSV} = 100 µm
h_{TSV} = 100 µm

Extracted RLGC parameters

C_{Glass} = 9 fF
G_{Glass} = 100 kOhm
$C_{polymer}$ = 0.1 fF
$G_{polymer}$ = 10 kOhm
$C_{top,IMD}$ = 7.5 fF
$G_{top.IMD}$ = 10 MOhm
R_{TSV} = 3 mOhm
L_{TSV} = 49 pH

Insertion Loss : TGV vs. TSV



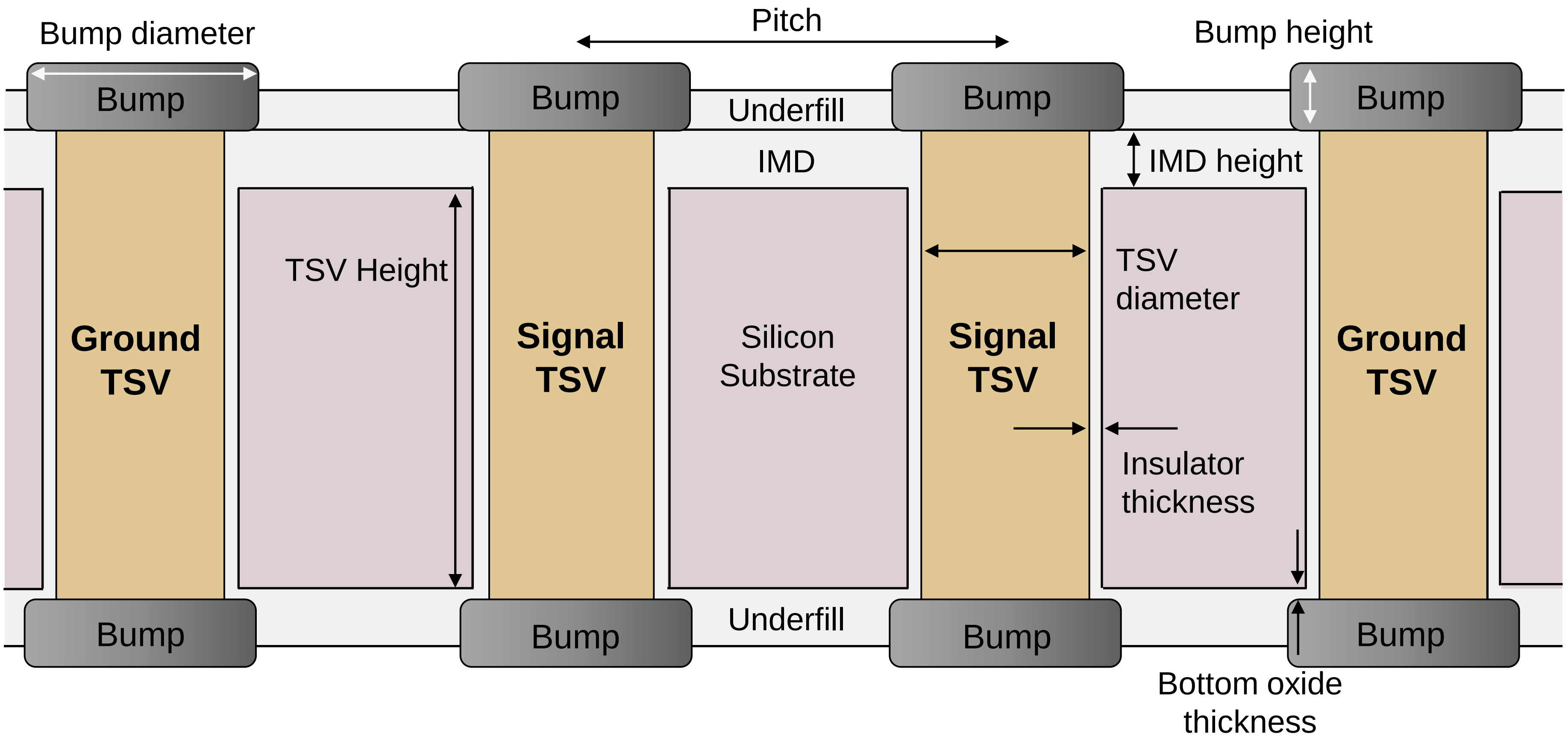
-0.06 dB @ 20GHz

Larger loss due to the lossy silicon substrate and thin SiO_2 liner of TSV

-0.46 dB @ 20GHz

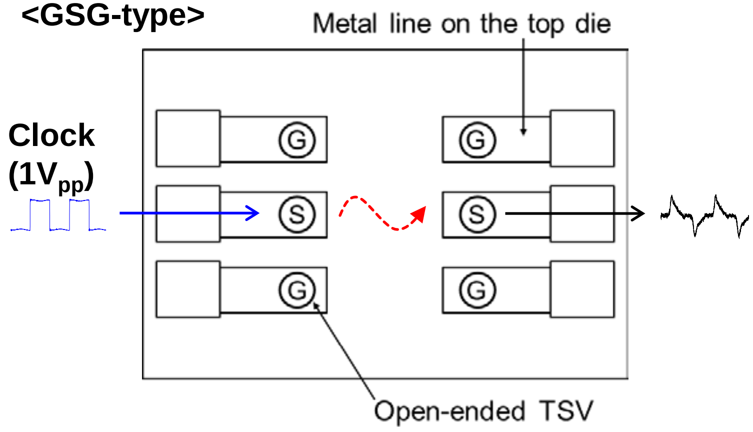
Differential Signal TSV

- Baseline structure of a differential signal TSV (GSSG type) with Bumps

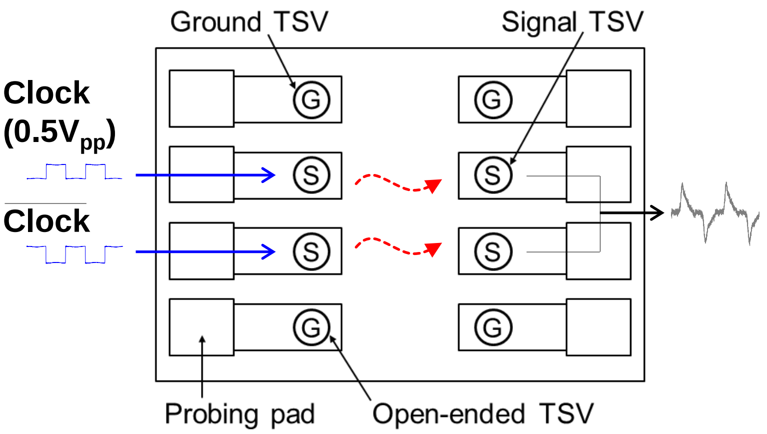


Measured Coupled Voltage of a TSV Channel depending on Signaling

<GSG-type>



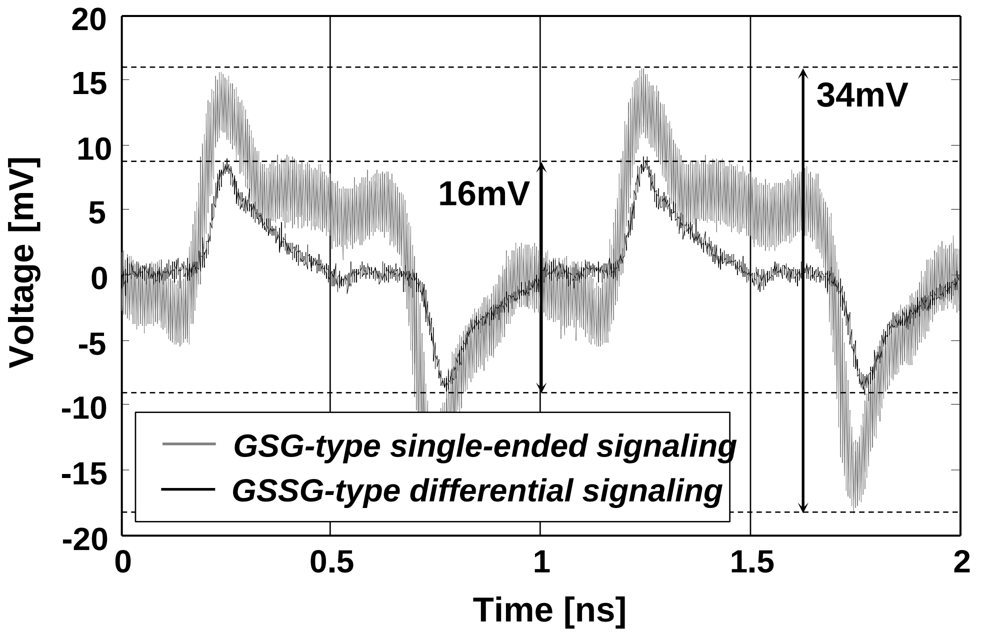
<GSSG-type>



Injected signal : 1GHz clock signal
Using pulse-pattern generator (PPG)
Digital cscilloscope : TDS8000B

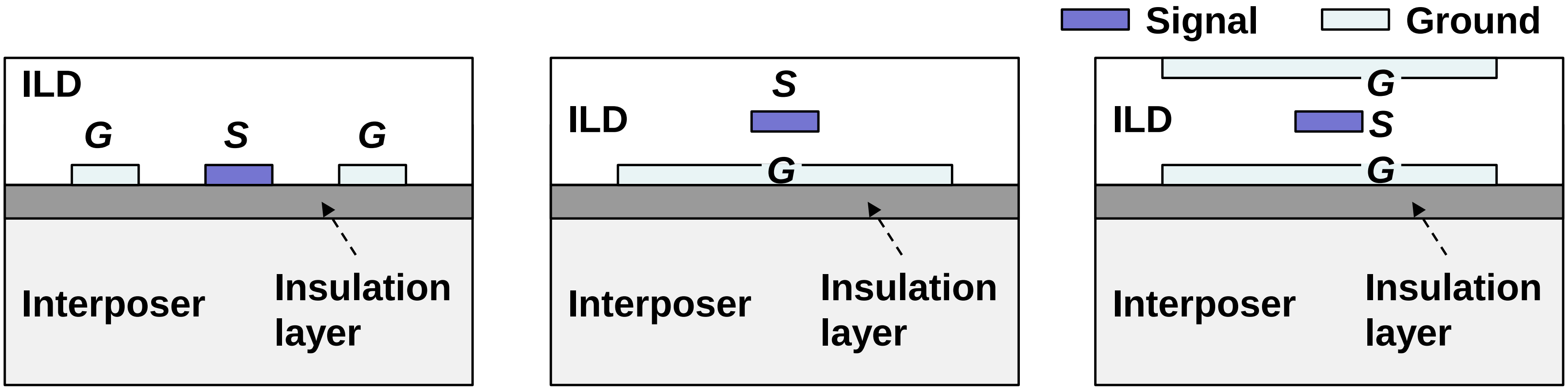
< Coupled Noise voltage >

Single-ended (GSG-type) vs. Differential (GSSG-type)

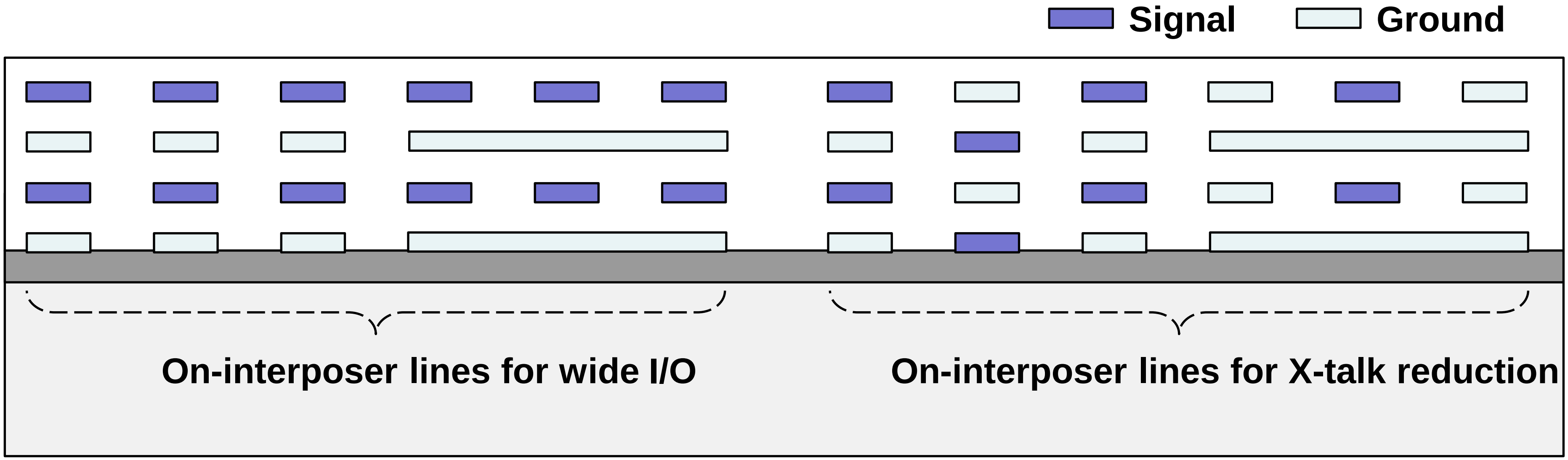


- **Even with the larger insertion loss, GSSG-type differential signal TSV has better noise immunity than GSG-type single-ended signal TSV**

Various Structures of On-interposer Metal Lines

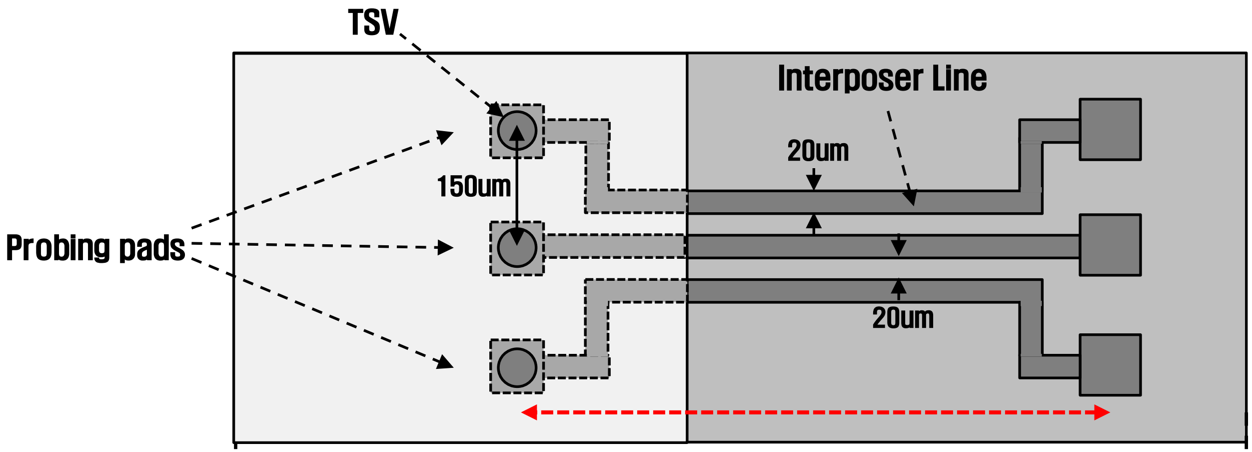


< Baseline structures – Coplanar waveguide (Left), Microstrip (Center), and Strip (Right) line

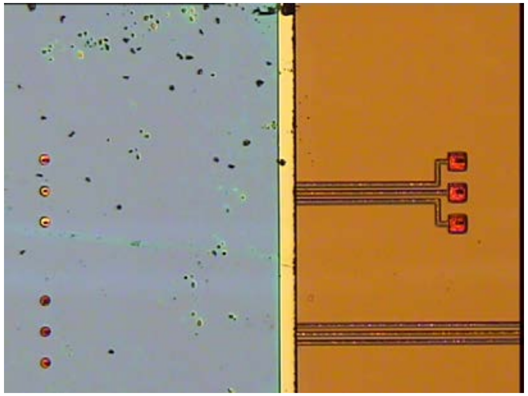


< Examples of on-interposer metal lines >

Fabricated TSV Channel for Modeling and Analysis



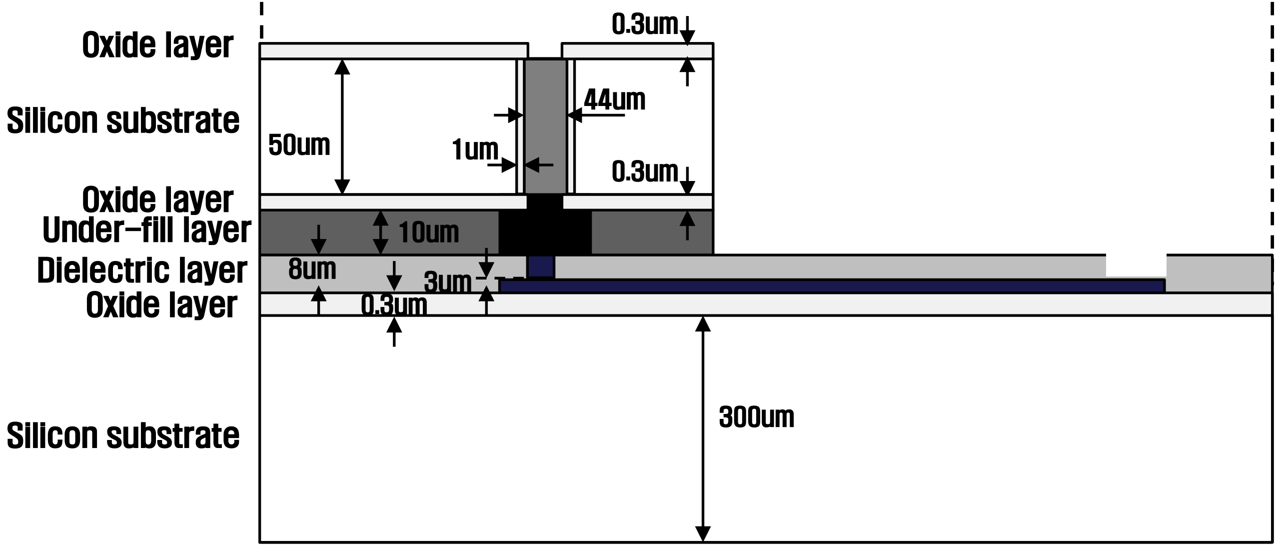
< Top view >



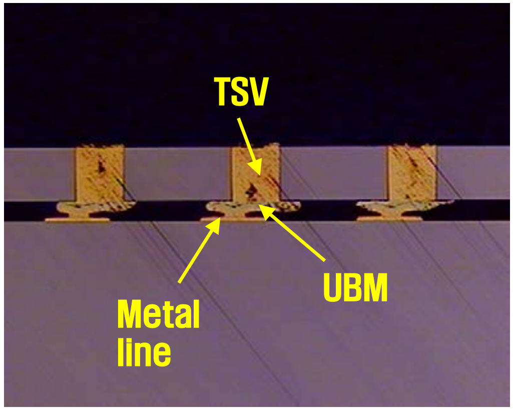
< Top view – SEM picture >

Length variation

→ 2000 / 3000 / 4000 um



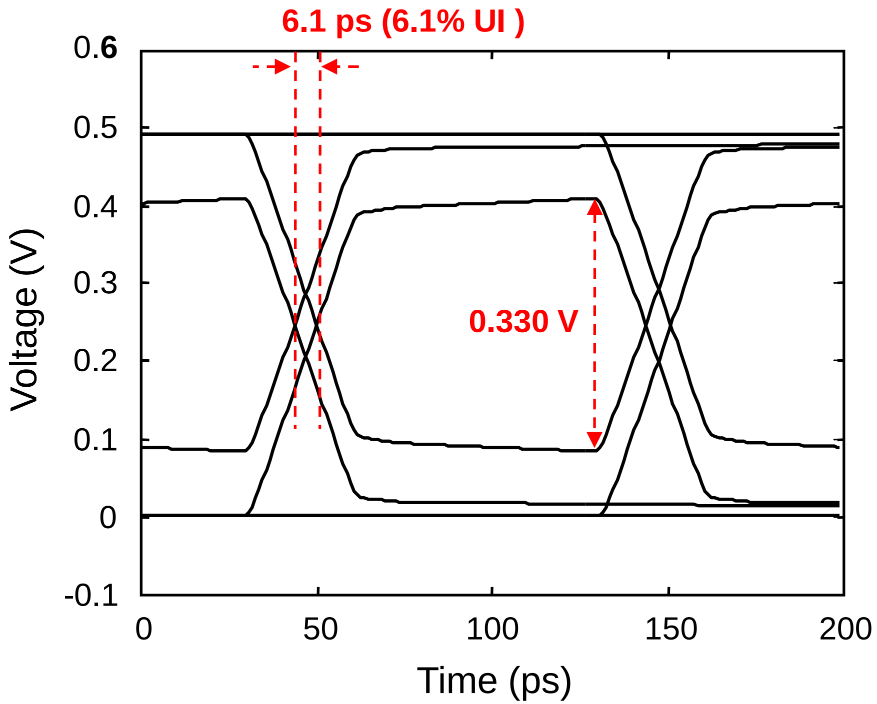
< Side view >



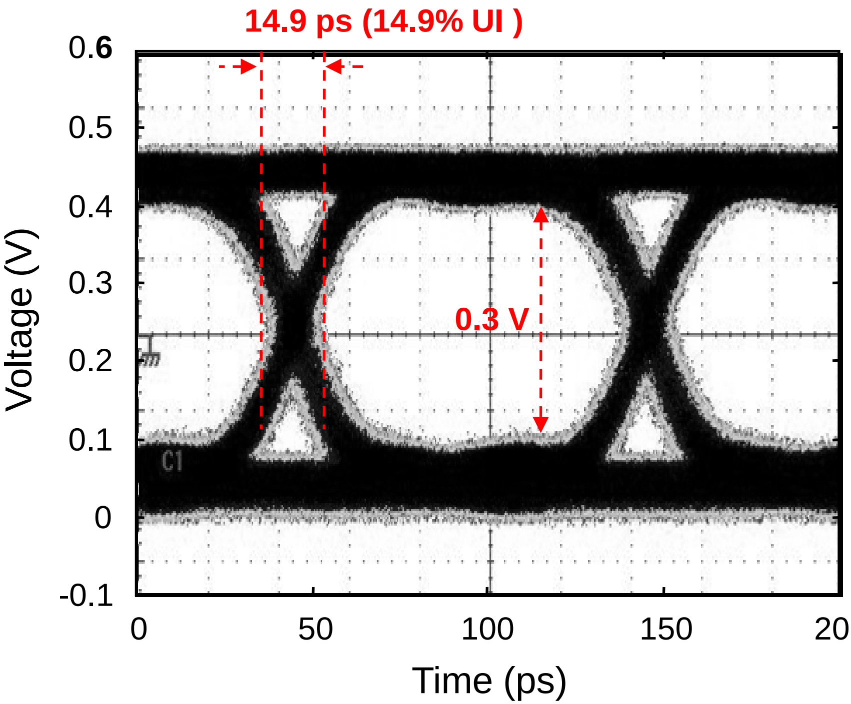
< Cross-sectional view – SEM picture >

Verification of Proposed Method by Time-domain Measurement – Test Vehicle A (Length = 500um) @ 10Gbps

- Input voltage = 1V



<Eye-diagram by using proposed method >

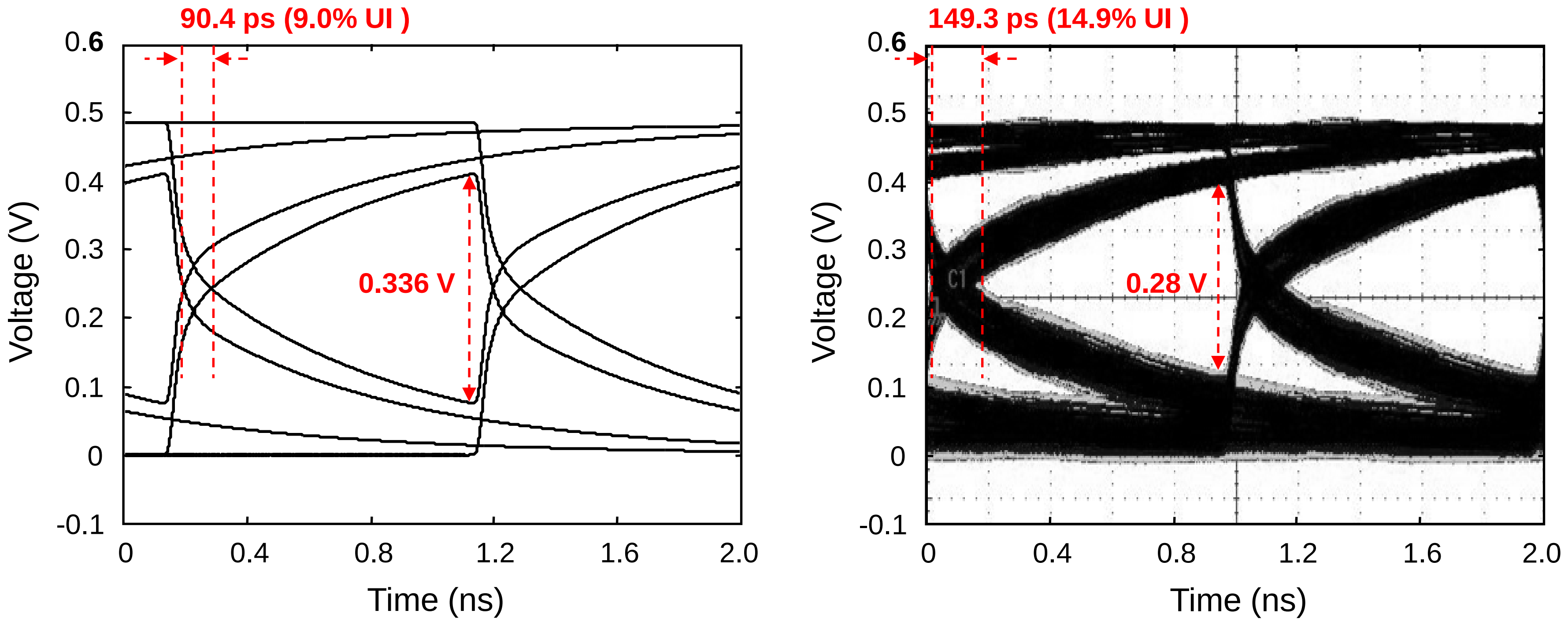


<Eye-diagram by time-domain measurement >

- **Error rate of the estimated eye-diagram using the proposed method**
  - **Eye-opening voltage : 5.2% V_{p-p}**
  - **Timing jitter : 8.8% UI**

Verification of Proposed Method by Time-domain Measurement – Test Vehicle B (Length = 4000um) @ 1Gbps

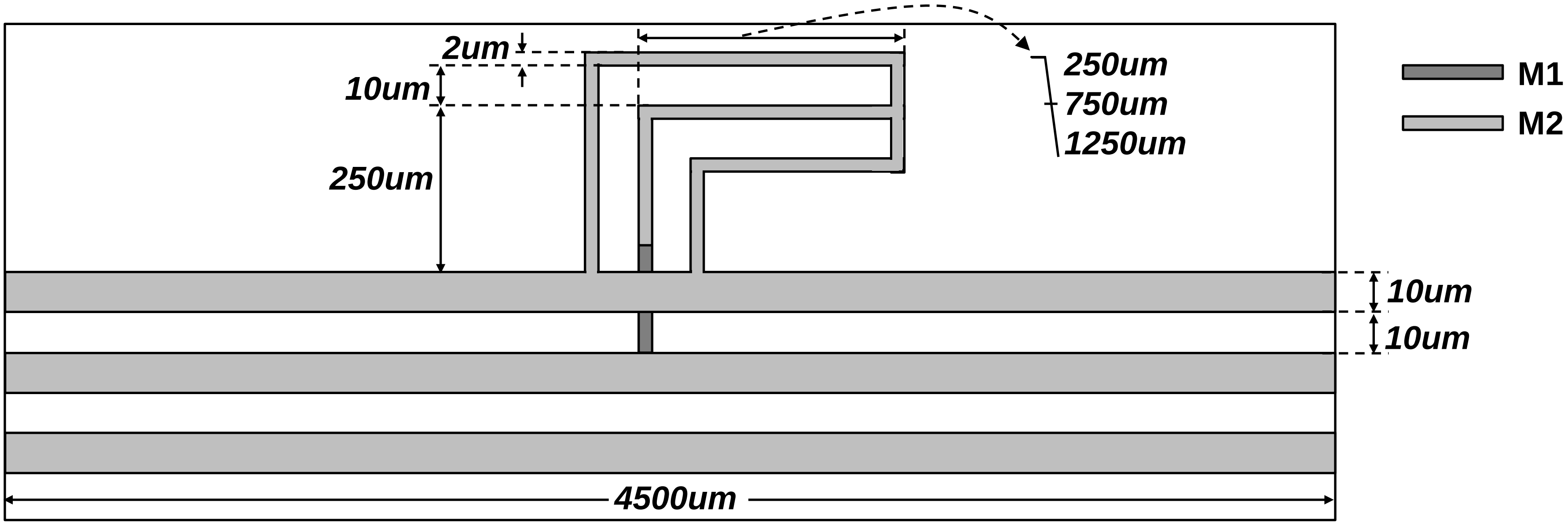
- Input voltage = 1V



<Eye-diagram by using proposed method > **<Eye-diagram by time-domain measurement >**

- **Error rate of the estimated eye-diagram using the proposed method**
  - **Eye-opening voltage : 11.2% $V_{p\text{-}p}$**
  - **Timing jitter : 5.9% UI**

Passive Equalizer at Interposer

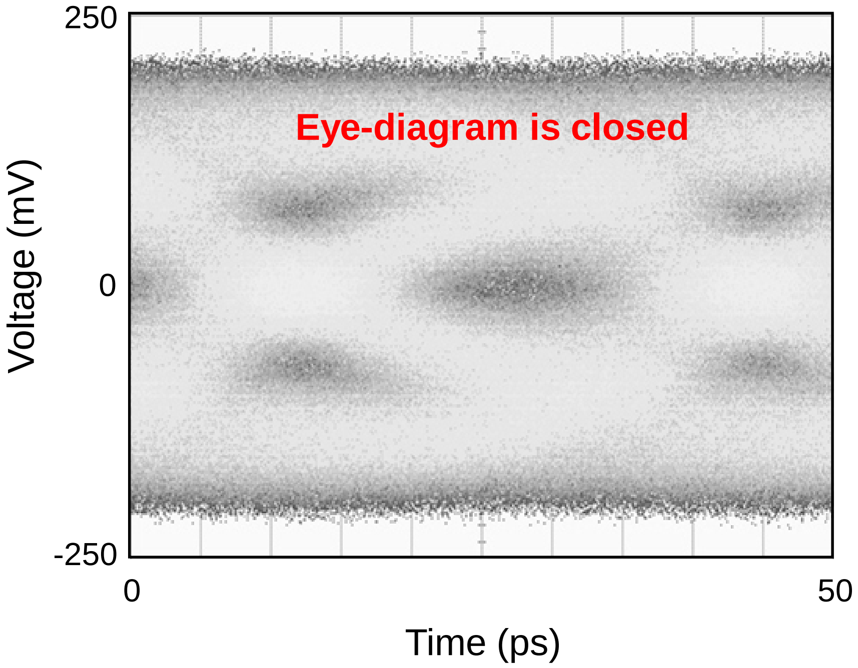


< Top view >

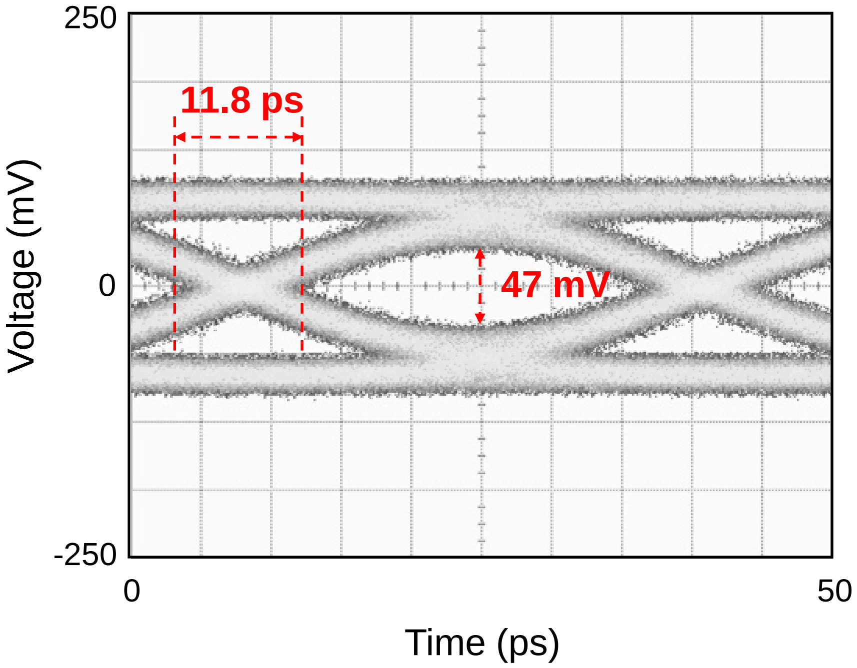
- Thicknesses of M1 / M2 = 0.7um / 0.7um
- Total length of stub = 500um, 1000um, 1500um
- Test pattern will be fabricated by MPW 104th M/H 0.35um
  - Die out : 2011. 12. 20

Measured Eye-diagrams at 30 Gbps (Passive Equalizer)

Data rate = 30 Gbps



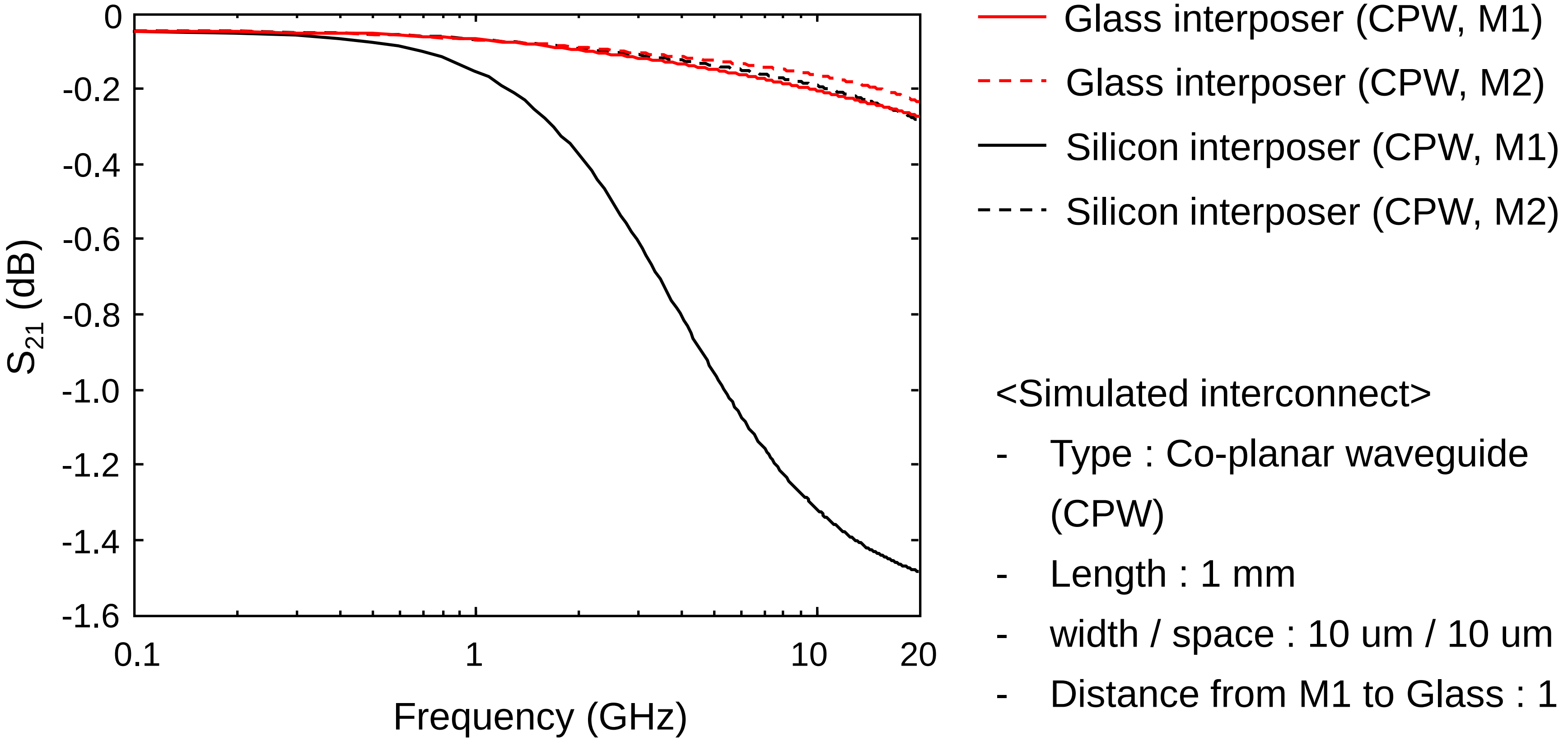
< Eye-diagram without passive EQ. >



< Eye-diagram with passive EQ. >

- **By using the passive equalizer, the eye-diagram at the data rate of 30 Gbps is improved**

S_{21} : Interposer Channel Loss: CPW

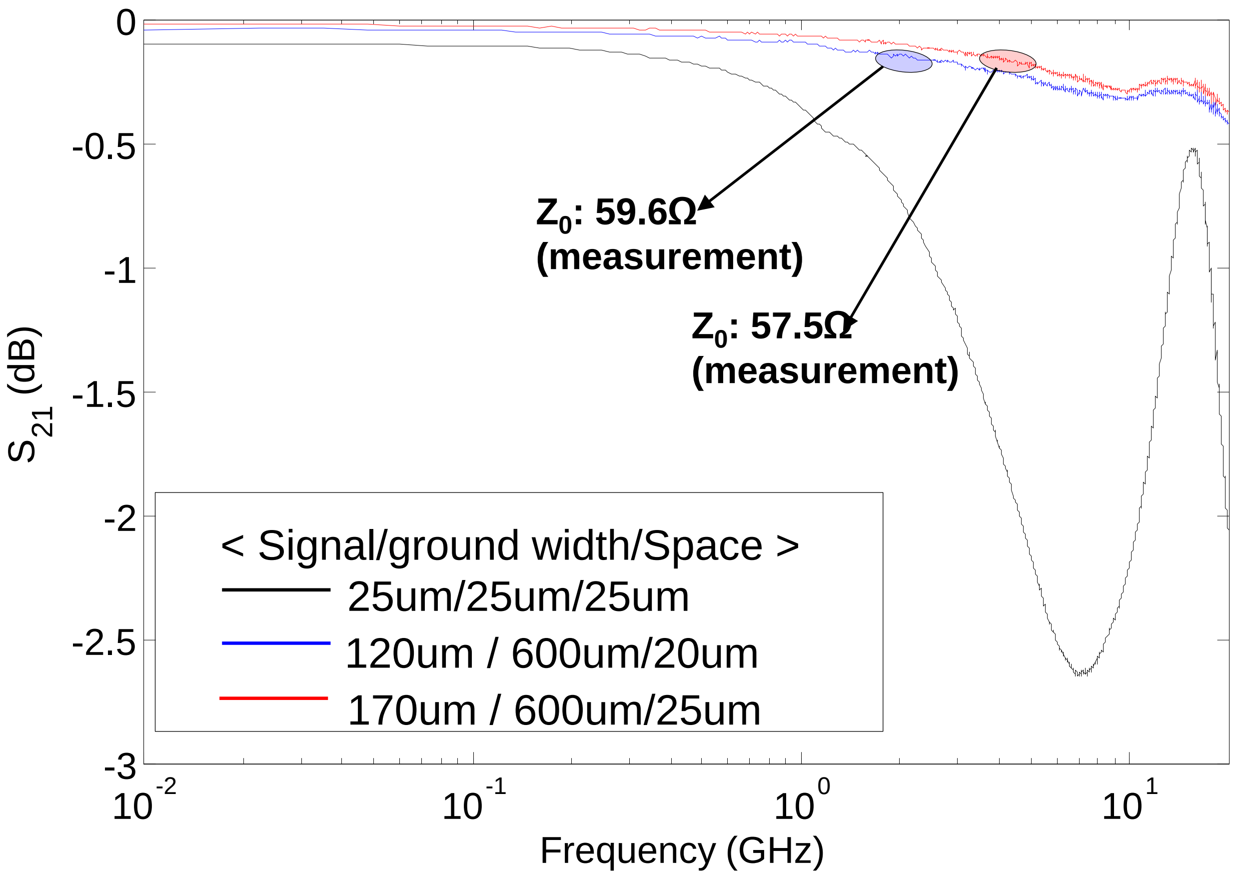


<Simulated interconnect>

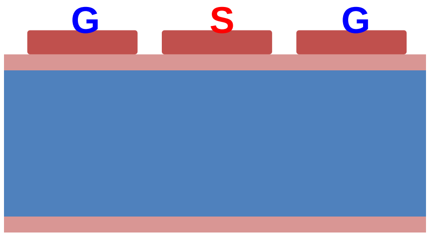
- Type : Co-planar waveguide (CPW)
- Length : 1 mm
- width / space : 10 um / 10 um
- Distance from M1 to Glass : 1 um

Insertion Loss Measurement of Glass Interposer

- 0.5dB loss at 20GHz, 6mm line Length



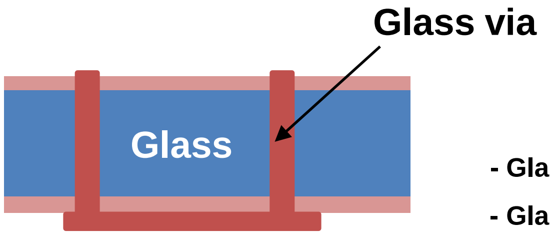
- Type : CPW
- Length : 6000um



< side view >

Eye-diagram of the Glass Channel (Via + Short line + Via)

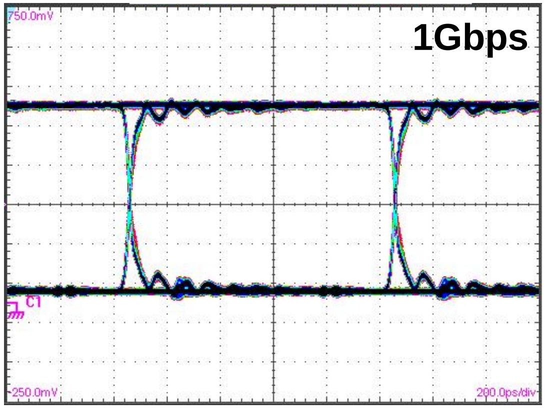
< Top view of glass channel >

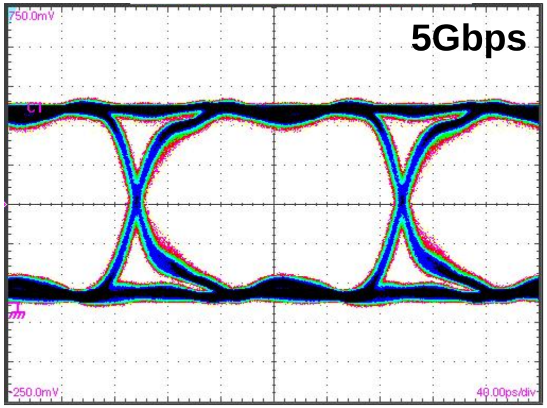


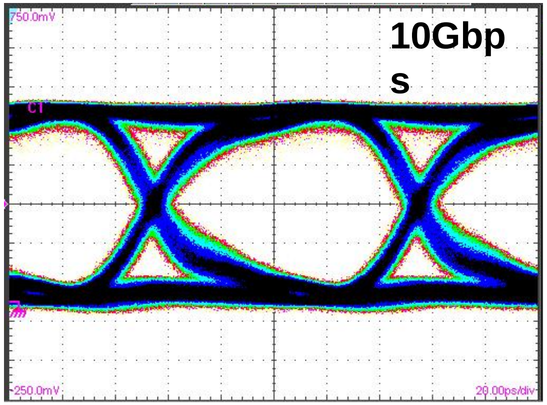
< side view >

- Glass via diameter: 60um

- Glass line: GSG coplanar waveguide (Width: 25um / space: 175um / length : 200um)



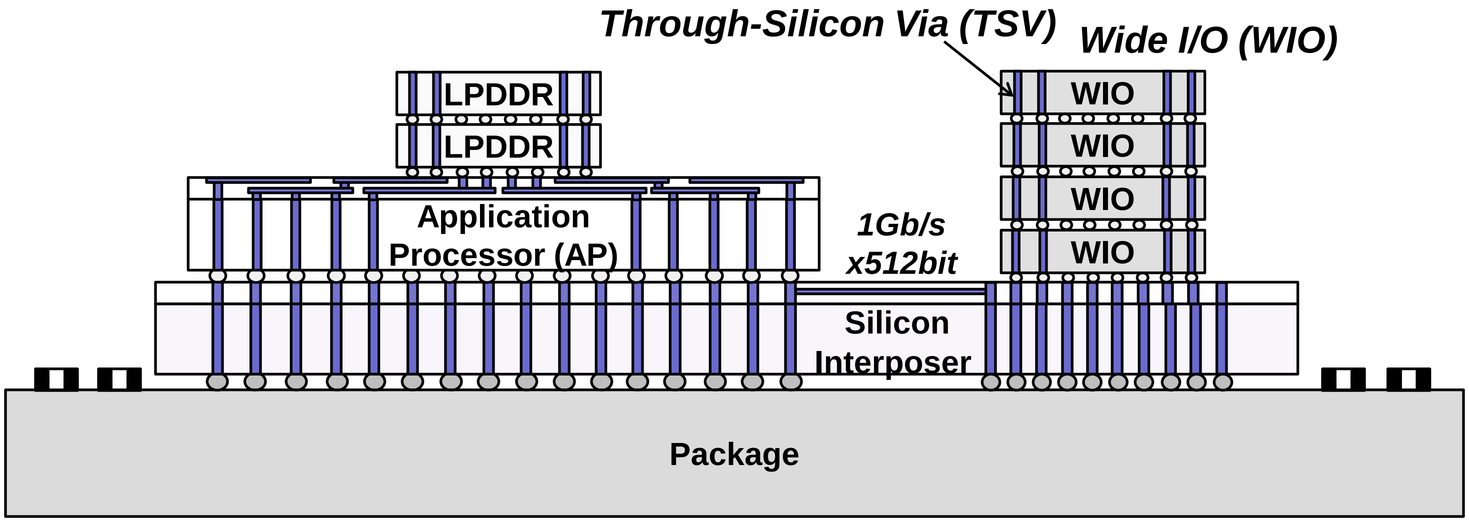




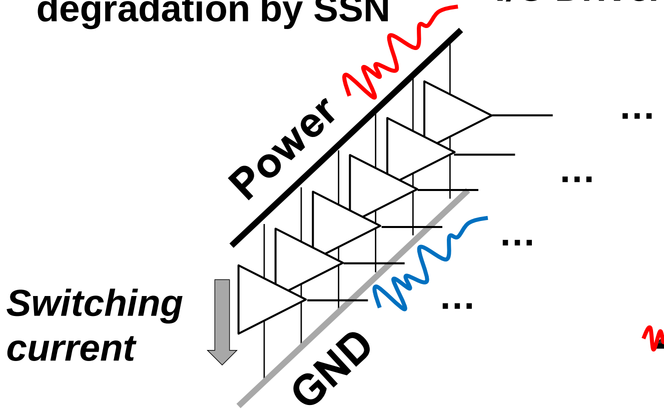
- Eye-diagram of glass channel (glass via + 200um line + glass via) is measured

- Because glass channel has a little loss, eye-diagram shape is almost determined by the cable
(90cm high-frequency cable has -1.3dB insertion loss at 10GHz)

Simultaneous Switching Noise (SSN) on Interposer and Problems caused by SSN

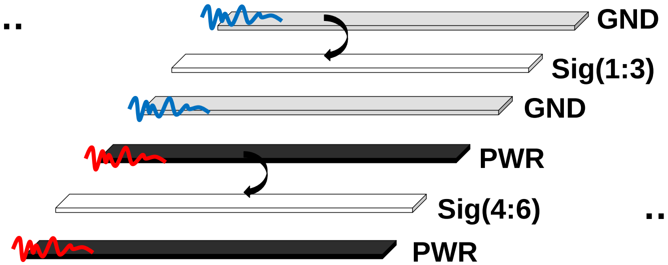


1. Driver performance degradation by SSN



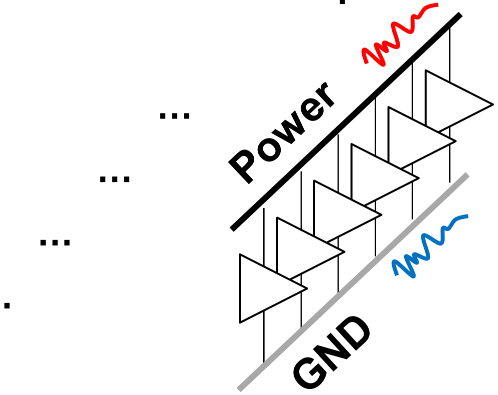
< AP >

2. SSN coupling



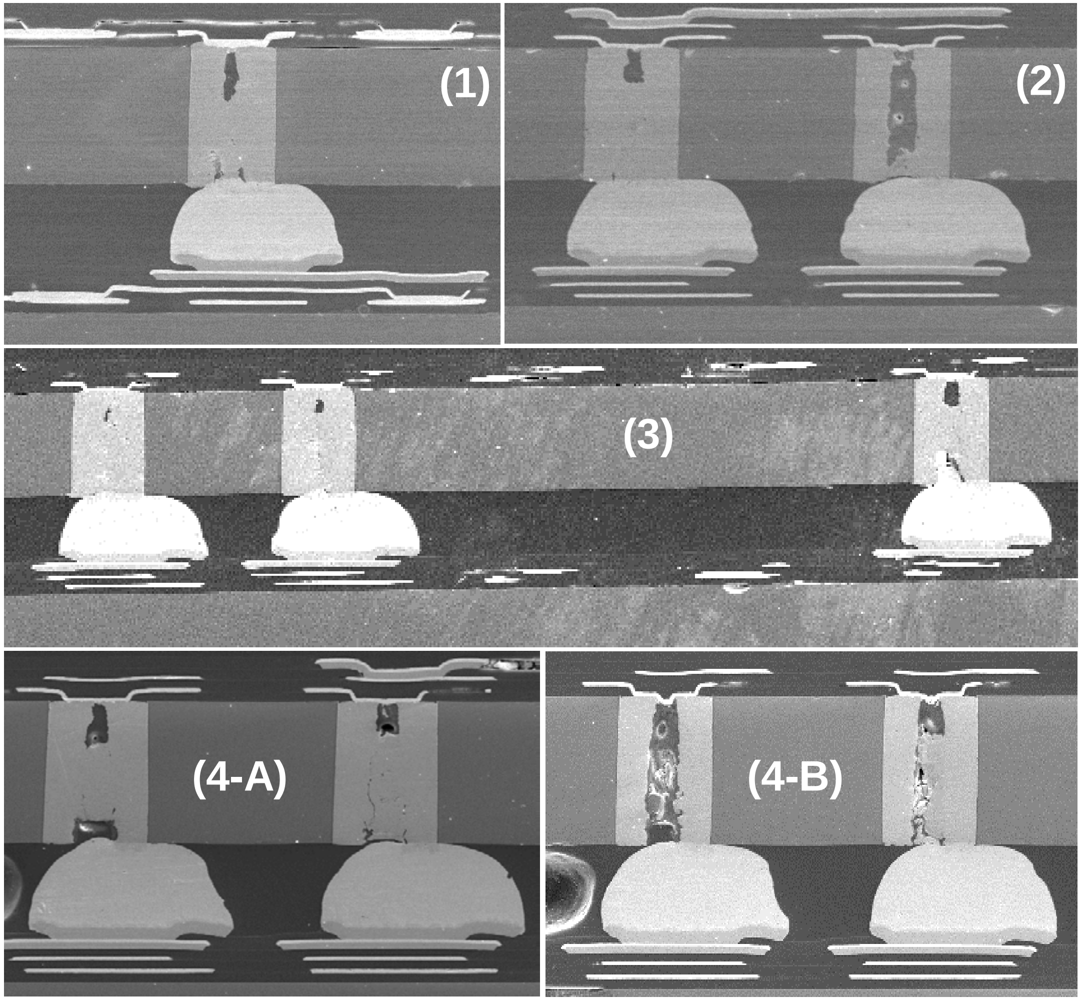
< lines on interposer >

3. SSN transfer through interposer line



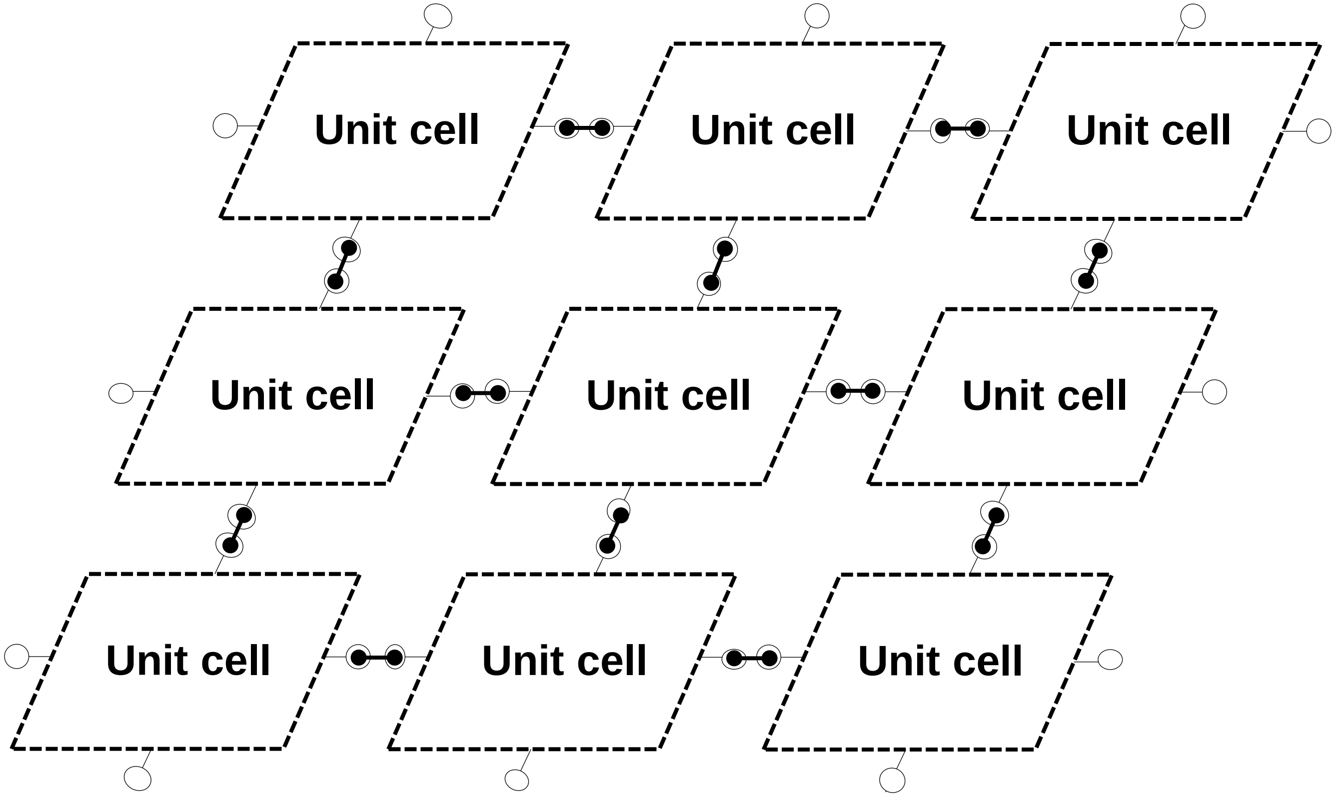
< Wide I/O >

SEM Photos for TSV Connection Test and Physical Dimension Confirmation (2/2)



- **We confirmed all TSV connections and physical dimensions of the fabricated sample by SEM photos.**

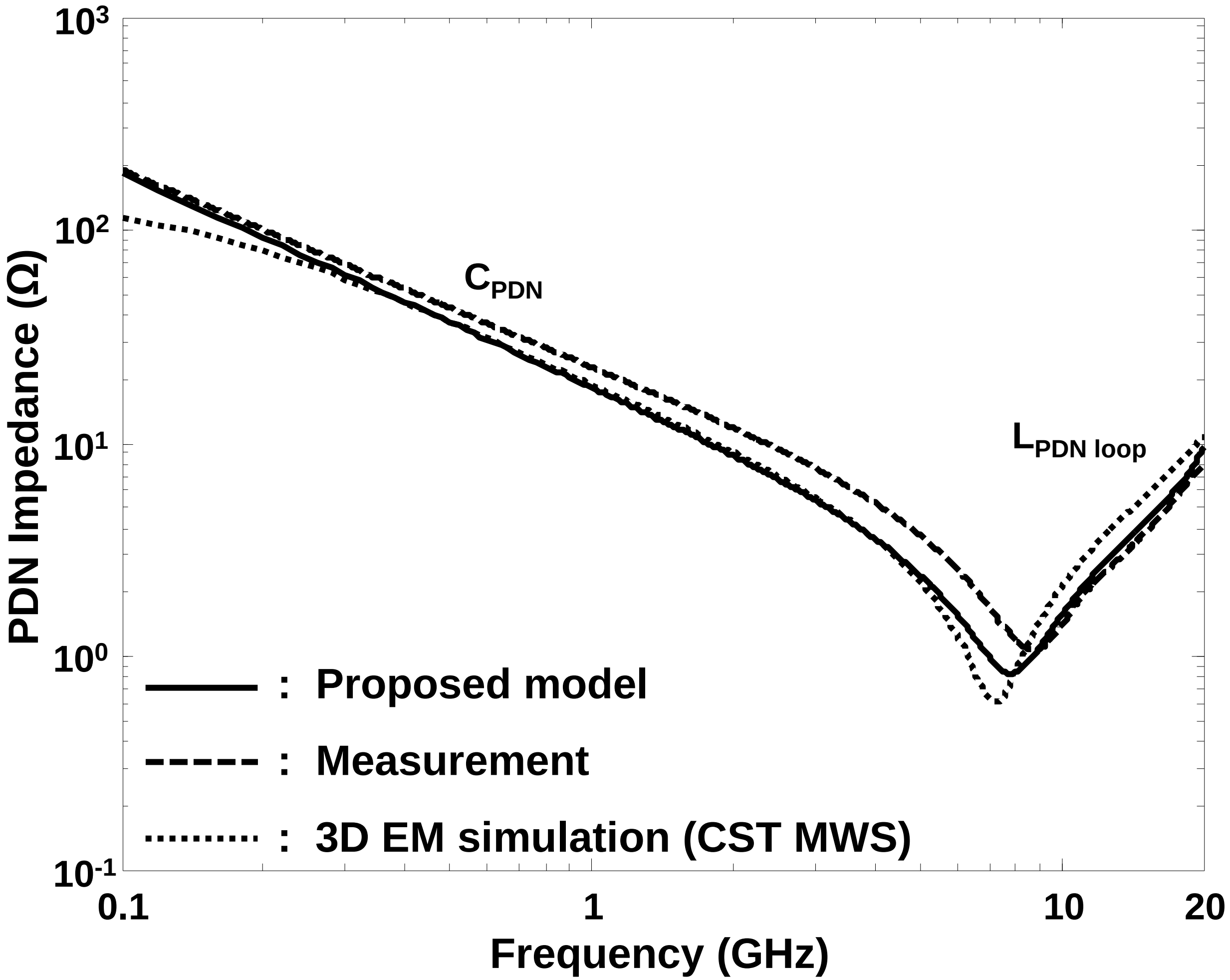
Modeling Method for Grid-type PDN based on a Segmentation Method



●—● : **Segmentation Method**

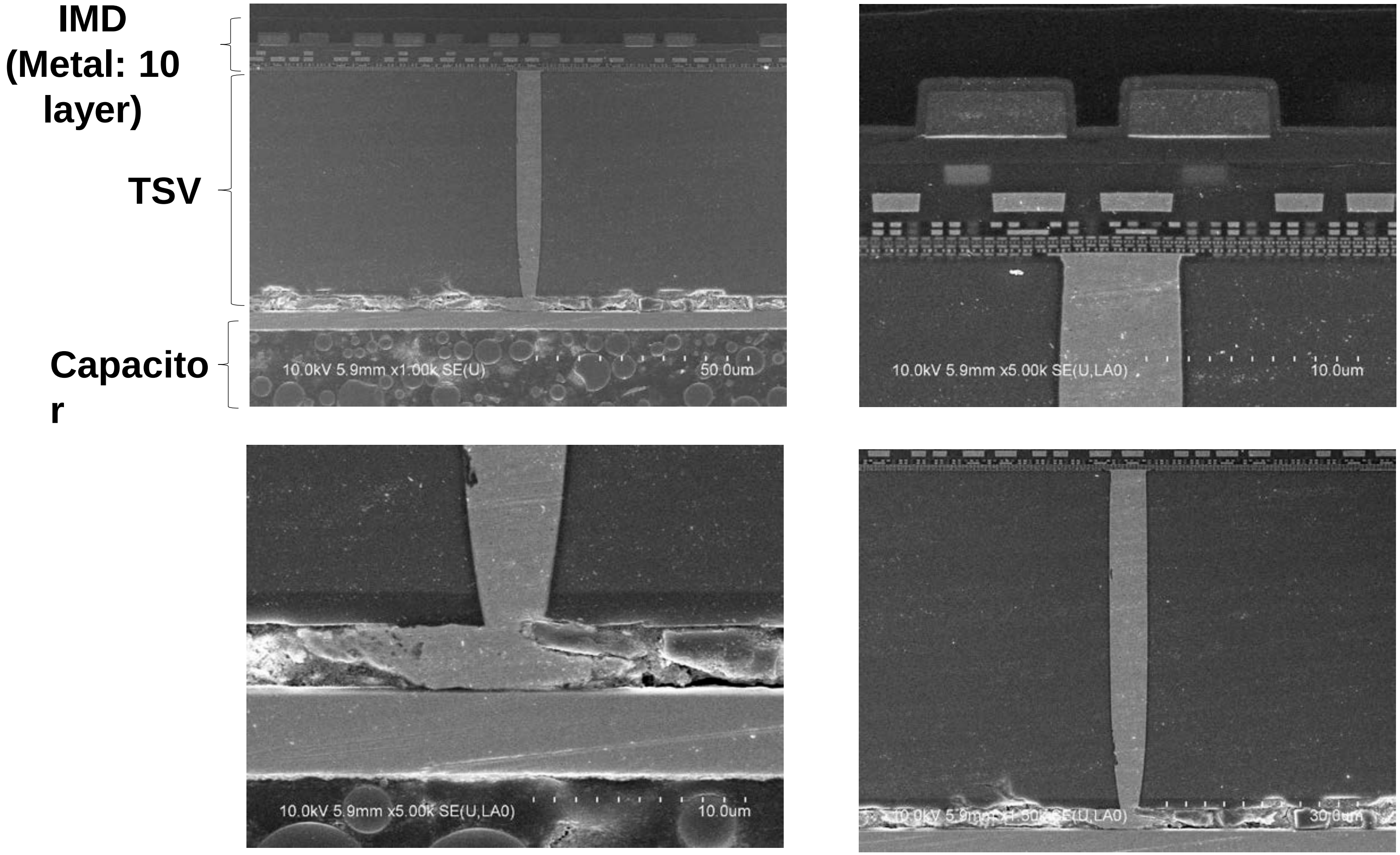
- **Once we have unit-cell models, we model the whole grid-type PDN by connecting all unit-cells that form the grid-type PDN based on a segmentation method.**

Verification of TSV-based Stacked Grid-type PDN Model



- **PDN self impedance estimated from the proposed model is well-matched with the simulation result and measurement in the frequency range of 0.1 GHz to 20 GHz.**

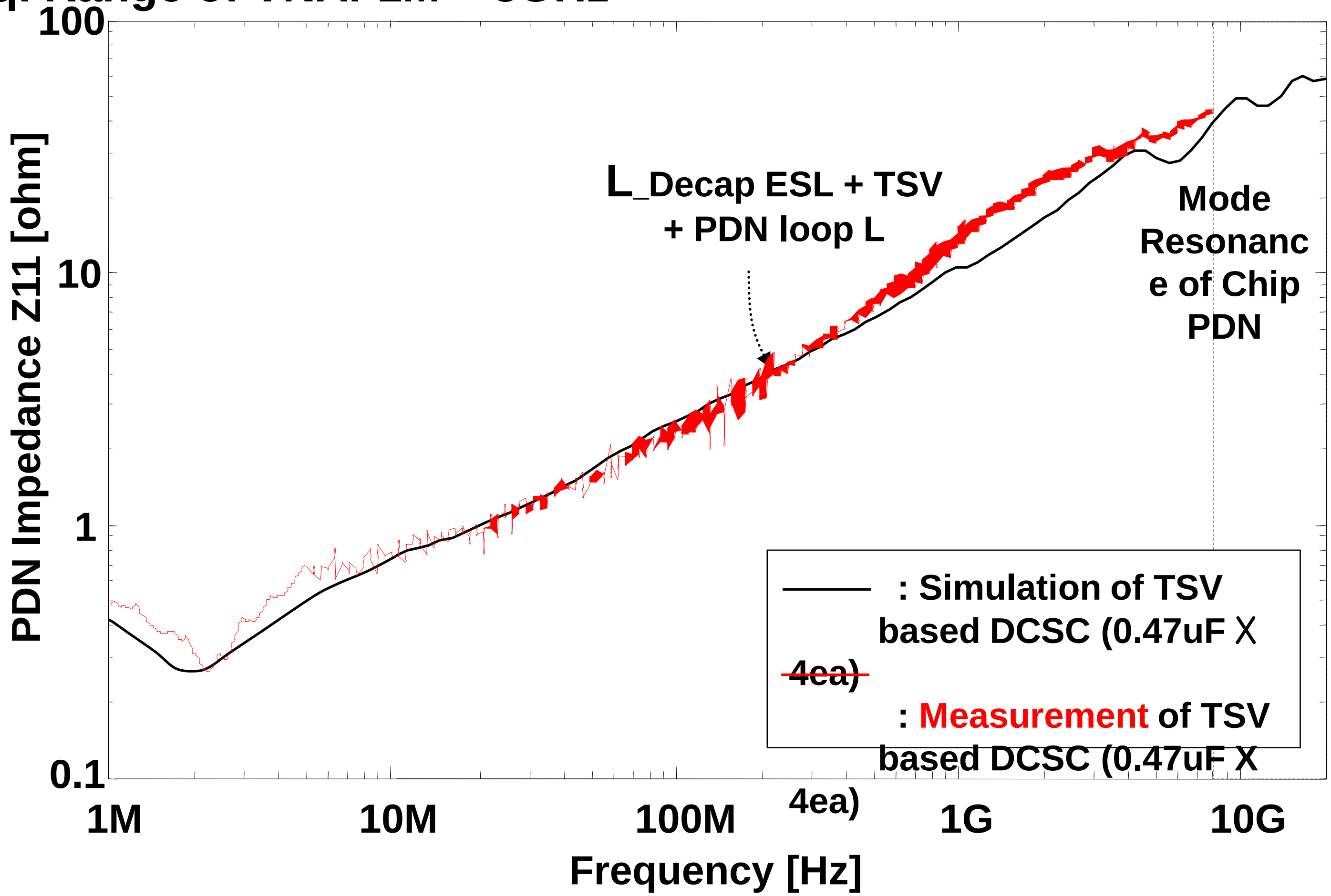
SEM Image of TSV-based DCSC



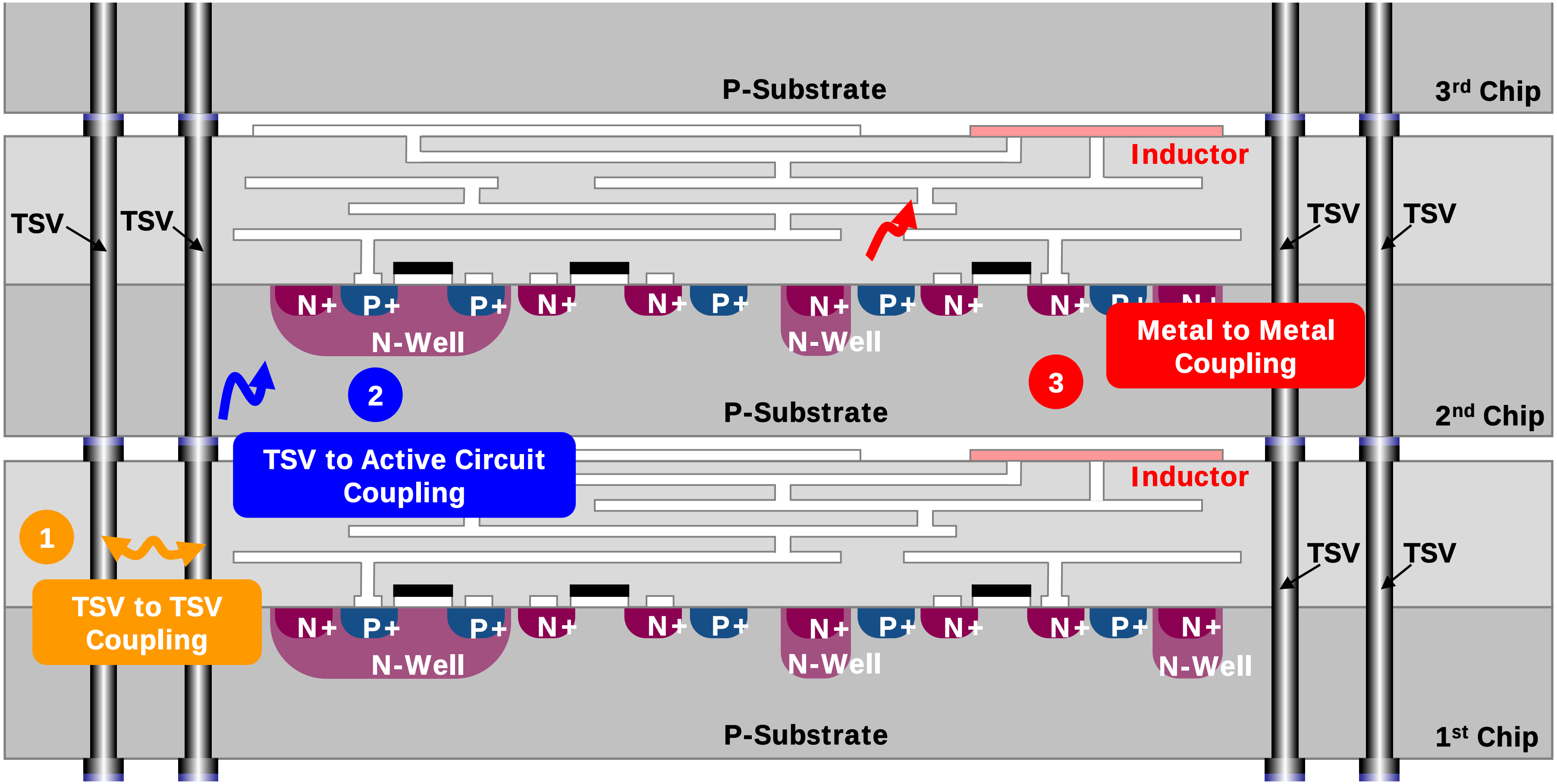
Comparison b/w measurement and simulation for PDN impedance (Z11) of the proposed TSV-based DCSC

- VNA measurement using agilent E5071B

- Freq. Range of VNA: 1M ~ 8GHz



Noise Coupling Paths in Stacked Dies using TSV: Non-ideal RCP

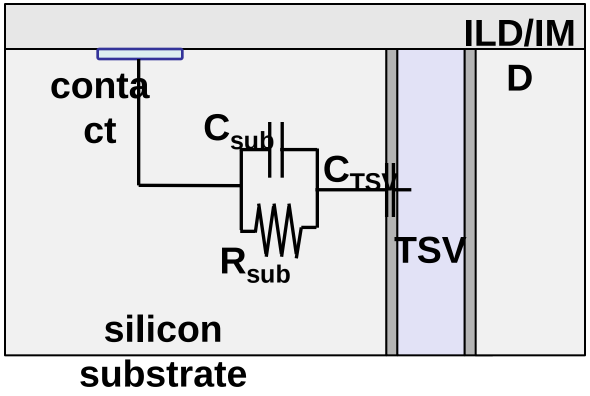


Metal to Metal Coupling

TSV to Active Circuit Coupling

TSV to TSV Coupling

Analysis of Noise Coupling based on the 3D TLM Model

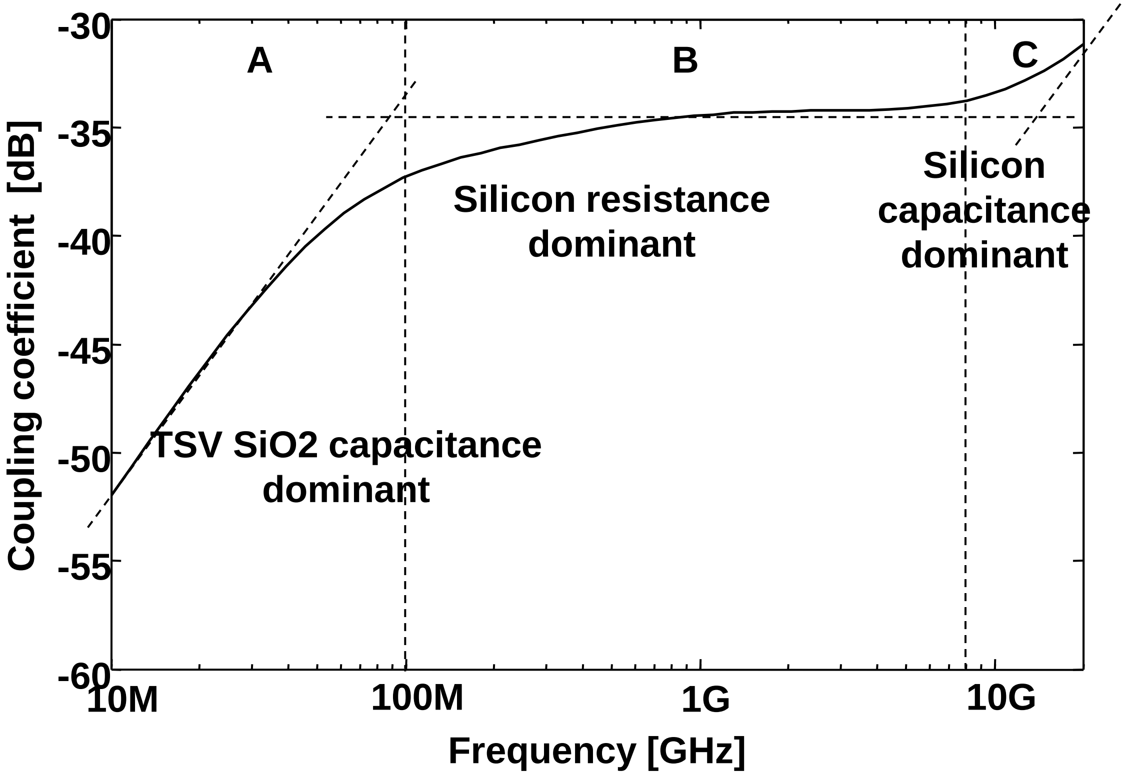


Distance between contact and TSV : 100 µm

Substrate height : 100 µm

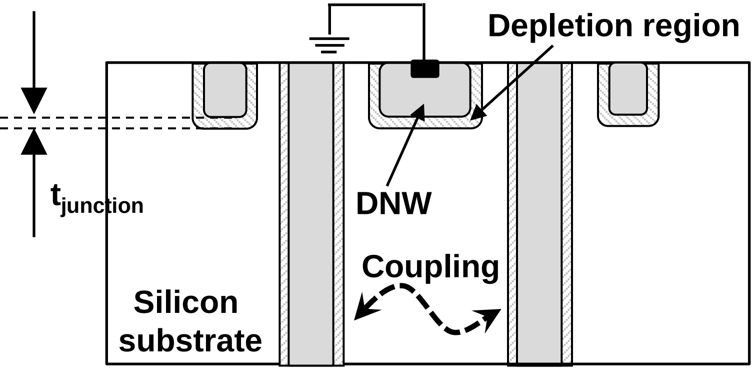
TSV diameter : 30 µm

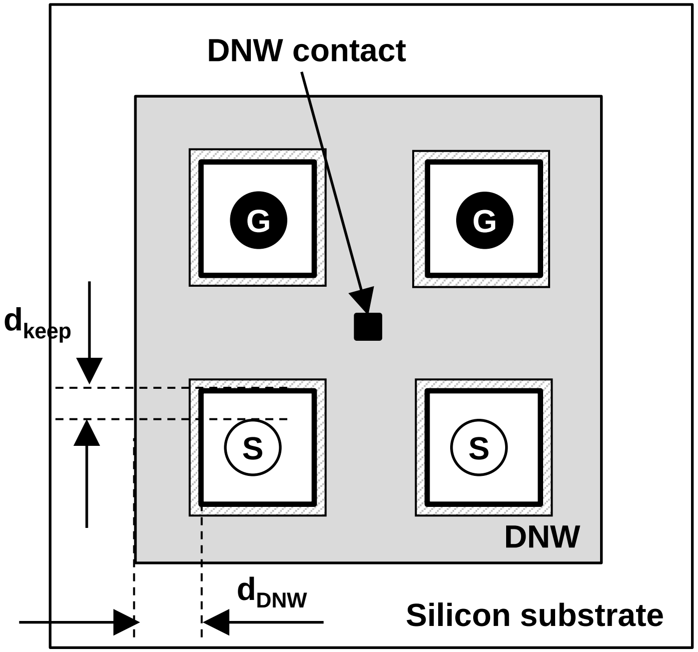
TSV SiO_2 thickness : 0.5 µm

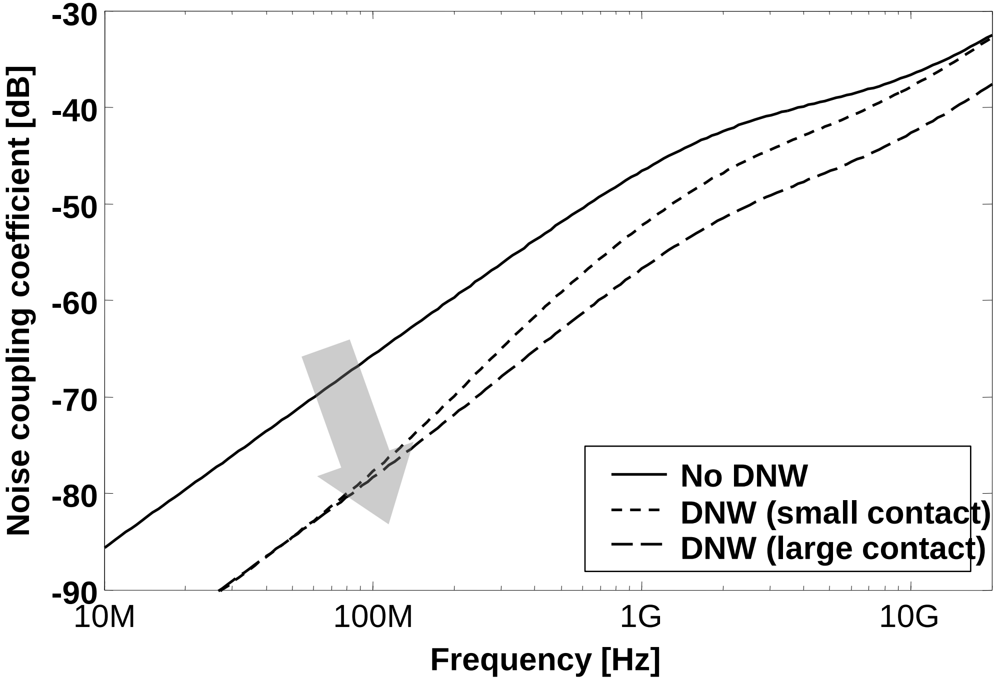


- Coupling can be divided into 3-regions
- In region A, B, and C TSV SiO_2 capacitance , silicon resistance, silicon capacitance is the dominant factor to the coupling

The Shielding Effects of Active Circuit near TSVs



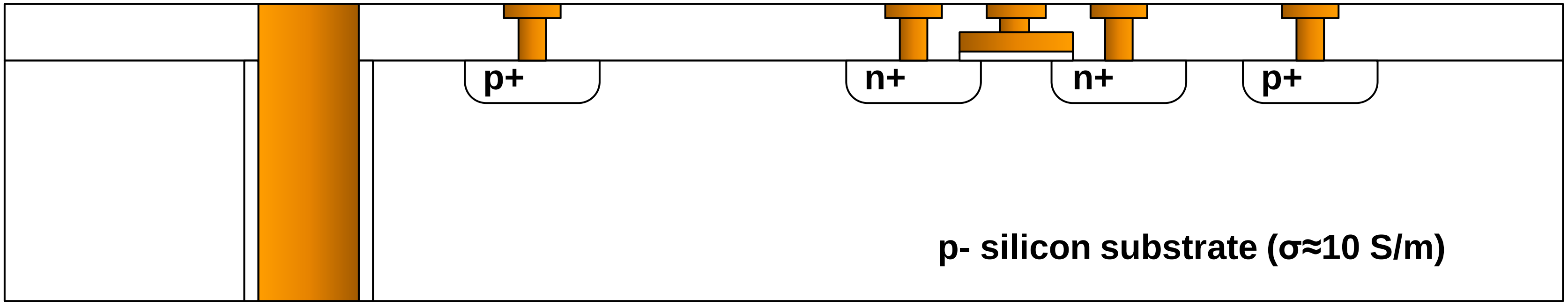




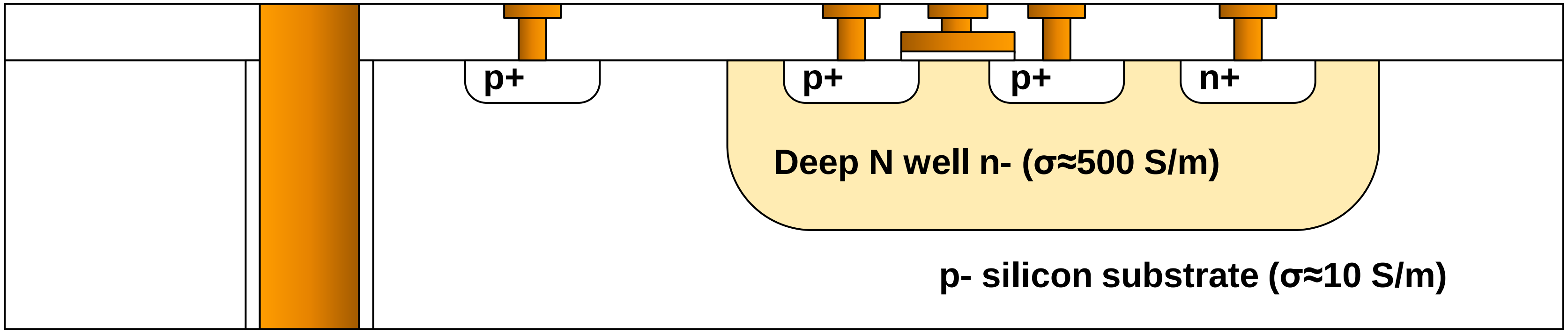
- Active circuit is simply modeled as DNW with keep out area from TSV (d_{keep})
- Shielding effects of DNW is validated by 3D EM-simulation and results are shown

Two cases assumption

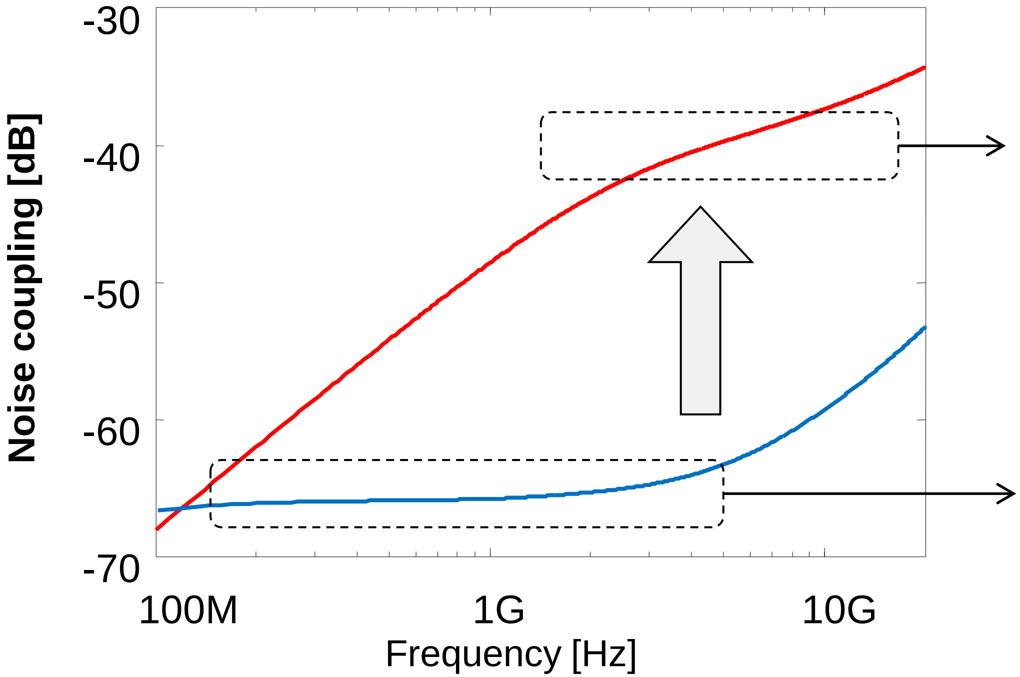
Case 1 (NMOS No DNW)



Case 2 (with σ≈500 S/m DNW)



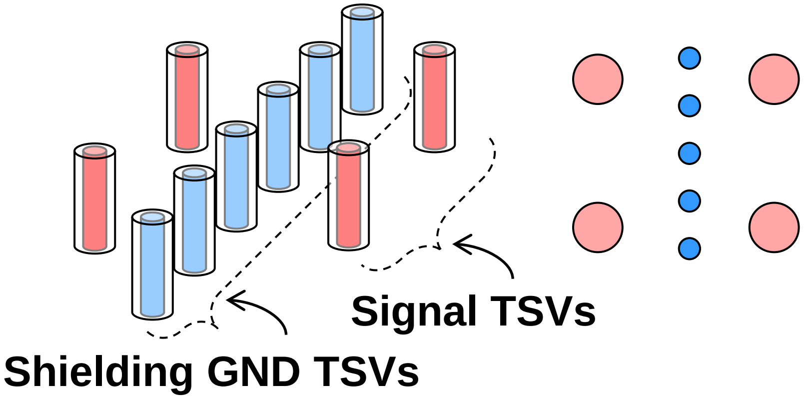
The effect of distance between TSV and ground tie1



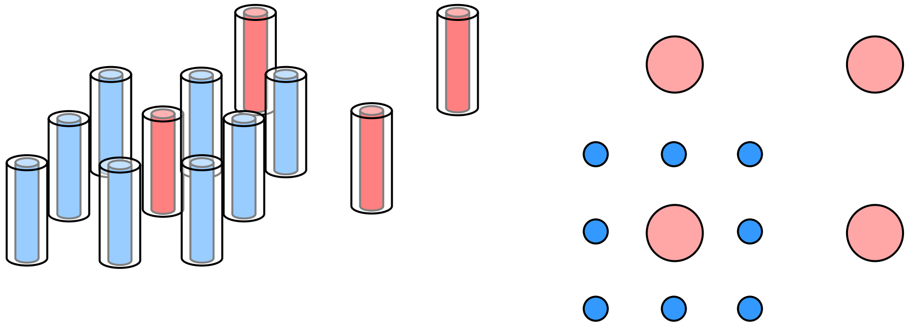
Case 2 : Combination of 10S/m Substrate and 500S/m higher conductivity DNW

Case 1 : Only 10S/m substrate

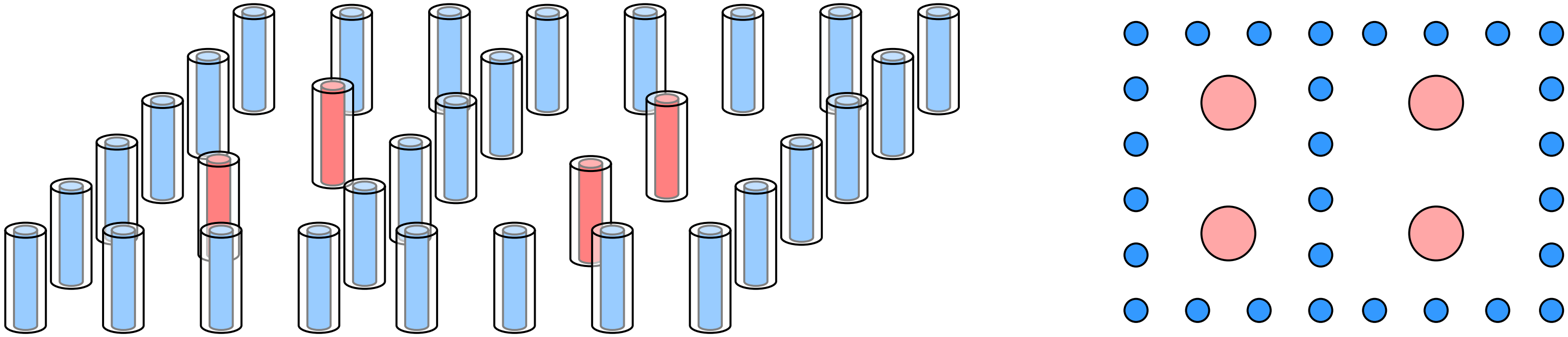
Shielding TSV (bar, ring, fence)



<Bar type>



<Ring type>



<Fence type>

- Shielding TSVs can be formed in various way
- It roles as an blocking structure between Signal and Signal, PWR and PWR TSVs, and even analog and digital block

Conclusions (1)

-2.5D architecture will be the most practical semiconductor integration solution for future low power and high-performance mobile platform

- TSV and interconnections will be the critical interconnection structures in 2.5D IC.

- Significant I/O power reduction and bandwidth increase can be achieved using the 2.5D architecture.

- Special TSV structures, transmission line structures, and equalizers are needed to meet low power and high-speed data transmission requirements.

Conclusions (2)

-I/O power noise suppression and hierarchical decoupling schemes are needed to suppress excessive I/O SSN noise

- Noise coupling is becoming a crucial concern in 2.5D system, and appropriate shielding methods should be applied