A 7.5Gb/s referenceless transceiver for UHDTV with Adaptive Equalization and Bandwidth Scanning Technique in 0.13um CMOS Process

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**Proposed Design**

- **Output driver with Dynamic pre-emphasis**
  - DDJ reduction with Dynamic pre-emphasis
  - Reduce power consumption using double pre-emphasis

- **Clock generator with BW control technique**
  - Minimize jitter using BW control to avoid gain peaking of noise
  - Finding optimum BW with changing of BW in clock generator

- **Equalizer with Pulse-width comparison**
  - Robust with PVT variations
  - Remove the local oscillator
  - Robust operation with self-adjusting reference voltage control
Clock Generator

**PLL**

Proposed bandwidth scanning loop

Skew detection block (SDB)

**CDR**

**Measurement Results**

Summarized results

W/o BW scanning clock Gen.
(10MHz sinusoidal supply noise)

Jitter: 5.27-ps$_{rms}$ 37.5-ps$_{p-p}$

W/ BW scanning clock Gen.
(10MHz sinusoidal supply noise)

Jitter: 3.15-ps$_{rms}$, 21.2-ps$_{p-p}$

RMS jitter comparison

- w/o BW control: 4.9-ps
- w/ BW control: 5.27-ps

38% Reduction

**Advanced Integrated Systems Lab.**
Measurement results – TX & RX

Transmitter measurement results

![Graph showing post-layout simulation results with minimum jitter at 16.9ps_p-p.]

<table>
<thead>
<tr>
<th>Control bit value</th>
<th>Post-layout simulation results</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Minimum jitter: 16.9ps_p-p</td>
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</tbody>
</table>

W/o calibration loop

Eye opening: 0.21UI

W/ calibration loop

Eye opening: 0.53UI

Receiver measurement results

![Before and after equalization of Rx input data and equalized data.]

Before equalization

Rx input data (24dB loss data cable)

Equalized data

Jitter: 23.3ps_p-p.
Conclusions

- Problems in high-speed transceiver are solved using dynamic pre-emphasis and double pre-emphasis control
  → Optimize DDJ problem and reduce power consumption

- Design with considering noisy environment and PVT variations
  → Can be adapted to other transceivers

Performance summary

<table>
<thead>
<tr>
<th></th>
<th>This work</th>
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</thead>
<tbody>
<tr>
<td><strong>Data rate</strong></td>
<td>7.5Gbps</td>
</tr>
<tr>
<td><strong>Acquisition</strong></td>
<td>Referenceless</td>
</tr>
<tr>
<td><strong>BER</strong></td>
<td>$&lt; 10^{-12}$</td>
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<tr>
<td><strong>Supply</strong></td>
<td>1.2V</td>
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<tr>
<td><strong>Power</strong></td>
<td>75.6mW (Tx)</td>
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<tr>
<td></td>
<td>69.6mW (Rx)</td>
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<tr>
<td><strong>Area</strong></td>
<td>0.14mm$^2$ (Tx)</td>
</tr>
<tr>
<td></td>
<td>0.15mm$^2$ (Rx)</td>
</tr>
<tr>
<td><strong>Technology</strong></td>
<td>130nm CMOS</td>
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