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**A 7.5Gb/s referenceless transceiver for UHDTV
with Adaptive Equalization and Bandwidth
Scanning Technique in 0.13um CMOS Process**
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Proposed Design



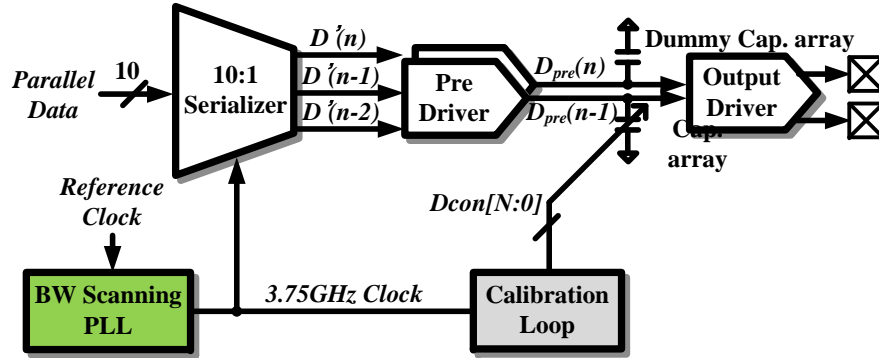
- ✓ **Output driver with Dynamic pre-emphasis**
 - DDJ reduction with Dynamic pre-emphasis
 - Reduce power consumption using double pre-emphasis
- ✓ **Clock generator with BW control technique**
 - Minimize jitter using BW control to avoid gain peaking of noise
 - Finding optimum BW with changing of BW in clock generator
- ✓ **Equalizer with Pulse-width comparison**
 - Robust with PVT variations
 - Remove the local oscillator
 - Robust operation with self-adjusting reference voltage control



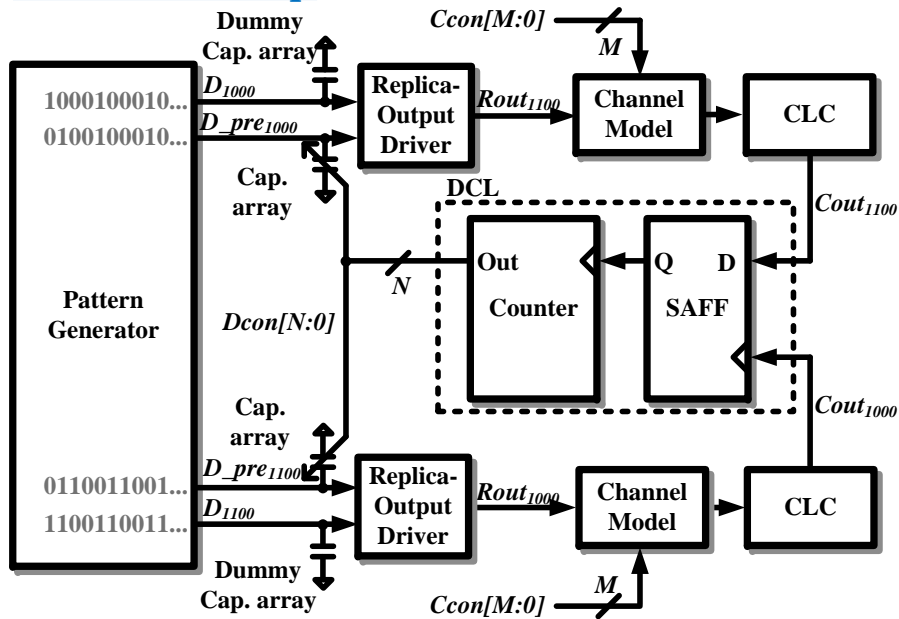
Top Architecture



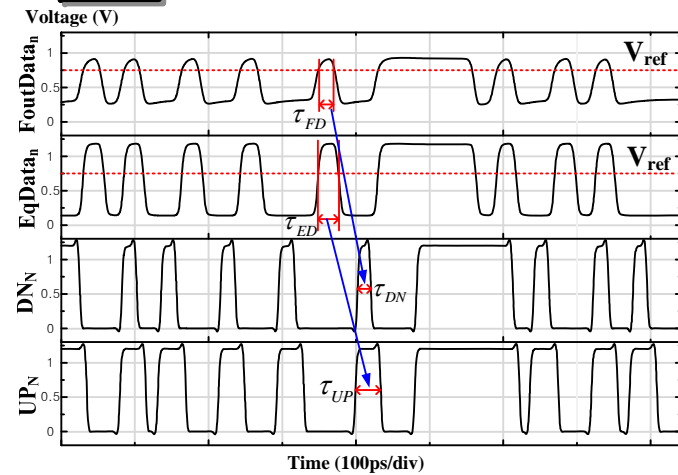
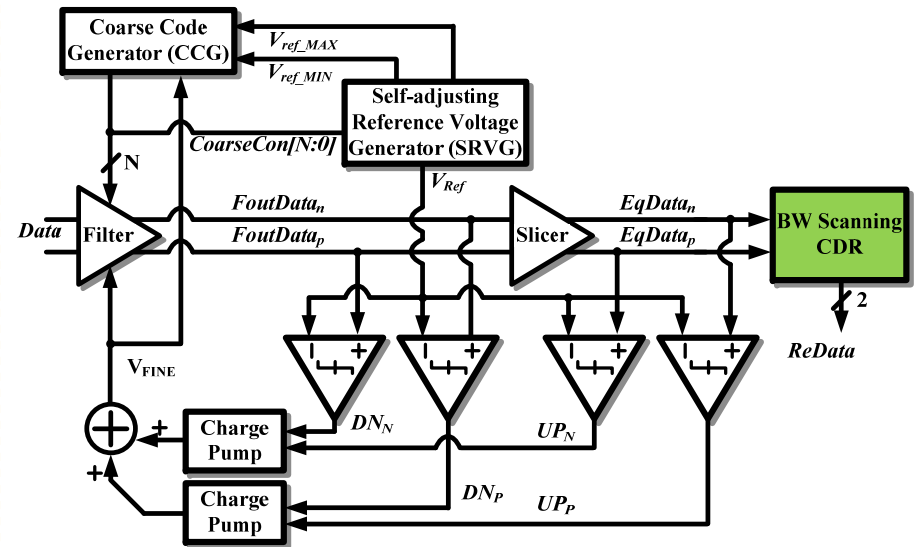
Transmitter



Calibration Loop



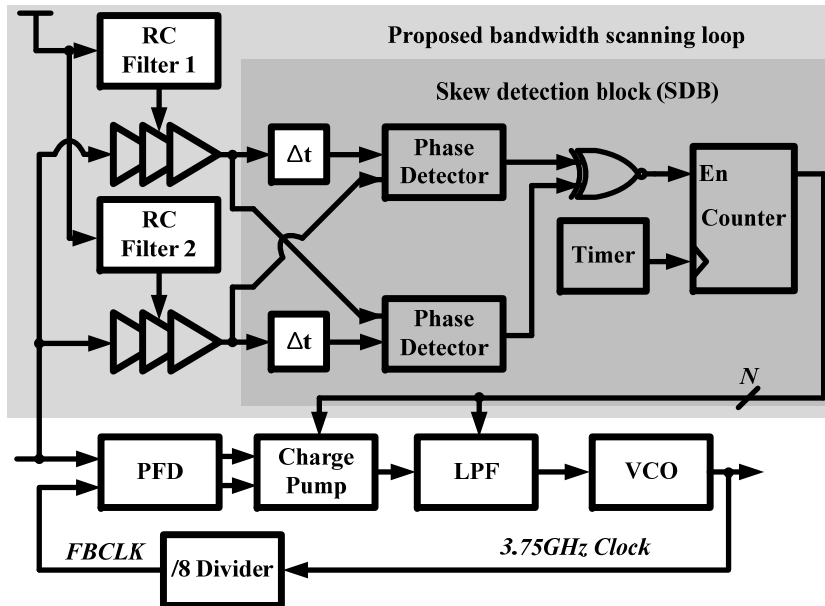
Receiver



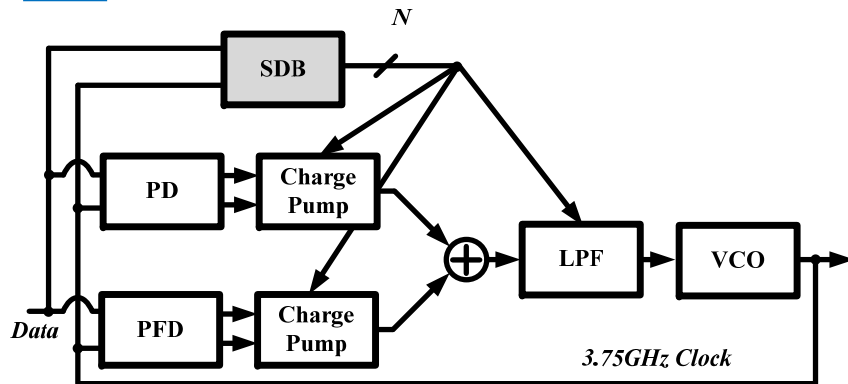
Clock Generator



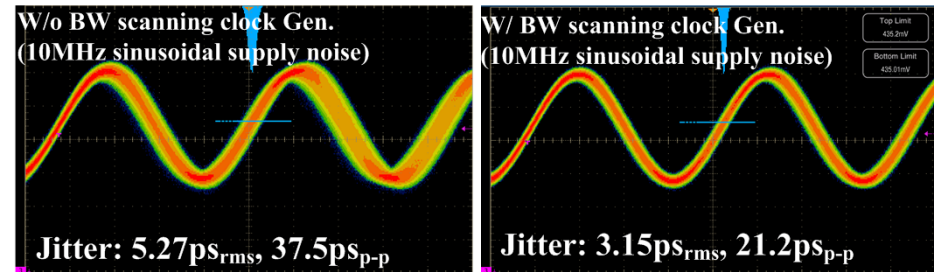
PLL



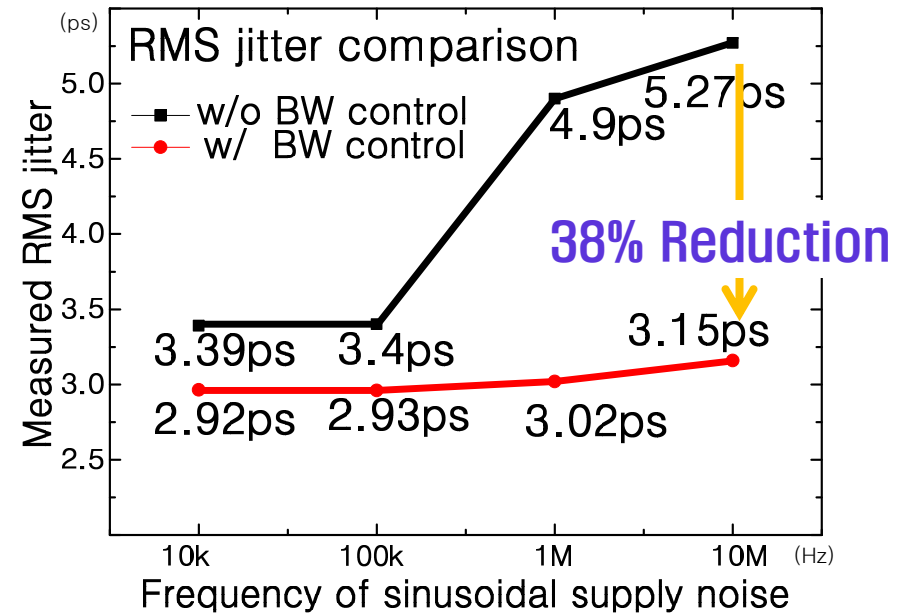
CDR



Measurement Results



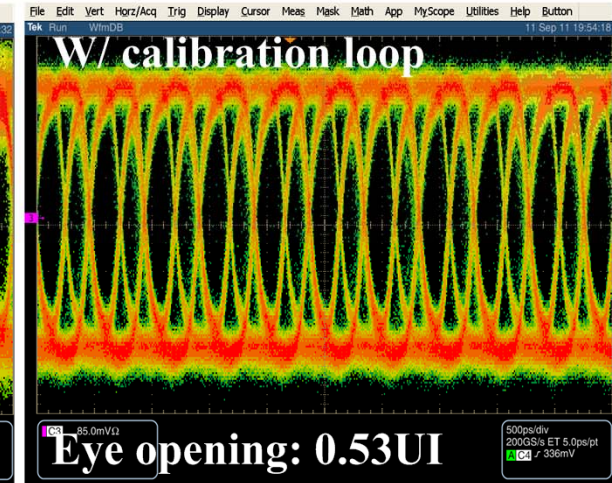
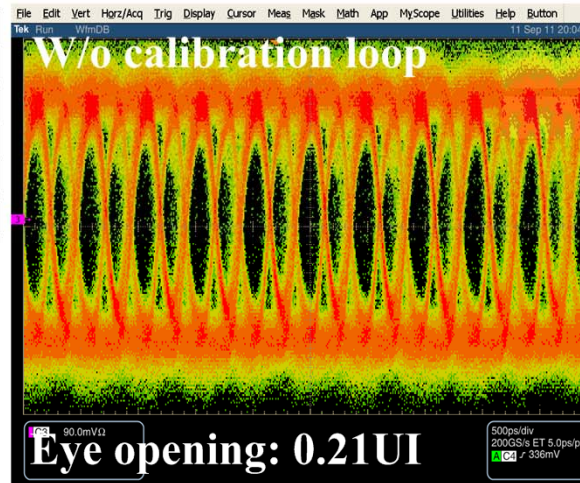
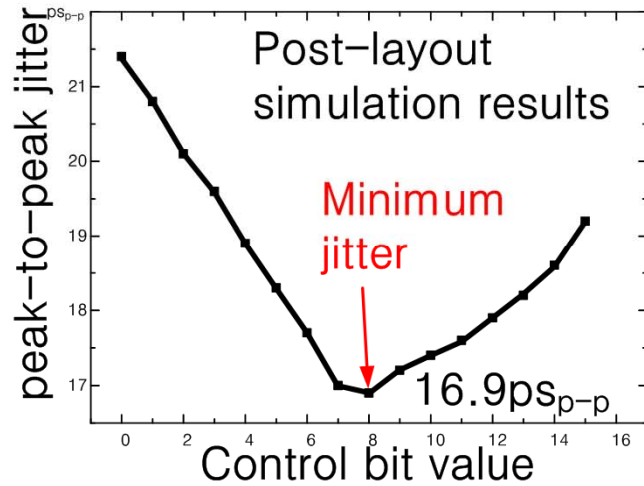
Summarized results



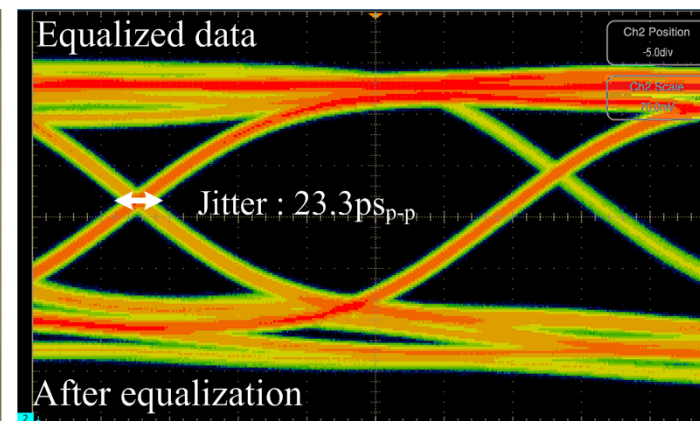
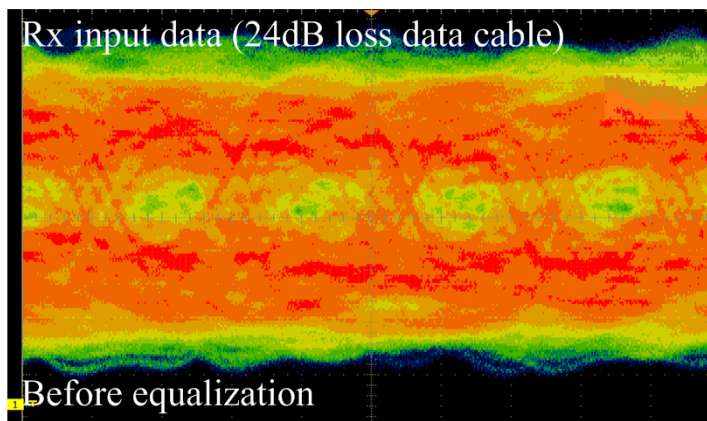
Measurement results – TX & RX



Transmitter measurement results



Receiver measurement results



Conclusions



- ✓ Problems in high-speed transceiver are solved using dynamic pre-emphasis and double pre-emphasis control
 - Optimize DDJ problem and reduce power consumption
- ✓ Design with considering noisy environment and PVT variations
 - Can be adapted to other transceivers

Performance summary

	This work
Data rate	7.5Gbps
Acquisition	Referenceless
BER	$< 10^{-12}$
Supply	1.2V
Power	75.6mW (Tx) 69.6mW (Rx)
Area	0.14mm ² (Tx) 0.15mm ² (Rx)
Technology	130nm CMOS

