315MHz OOK Transceiver with 38-μW Receiver and 36-μW Transmitter in 40-nm CMOS

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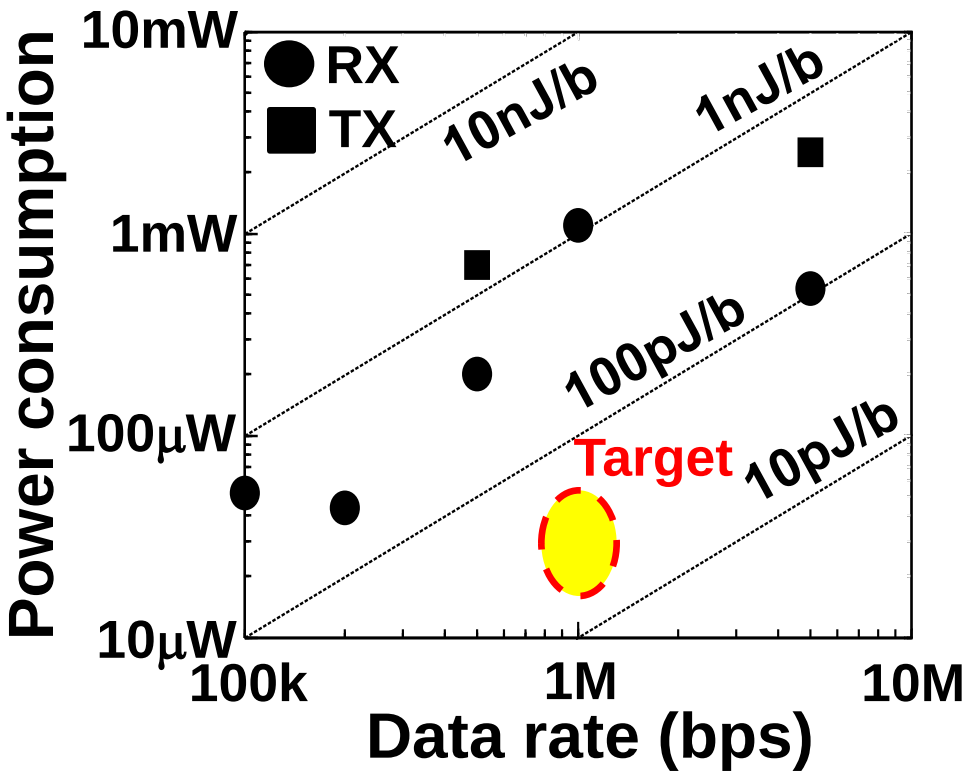
Design target

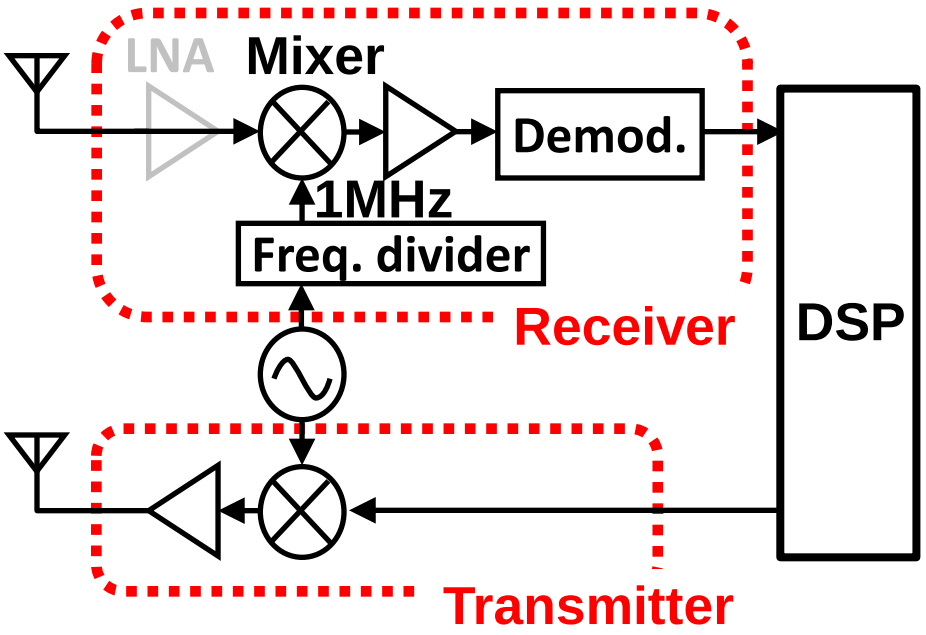
Target wireless communication

Short-range WSN (e.g. BAN)	
Data rate	1Mbps
Power consumption	50μW
Communication distance	1m

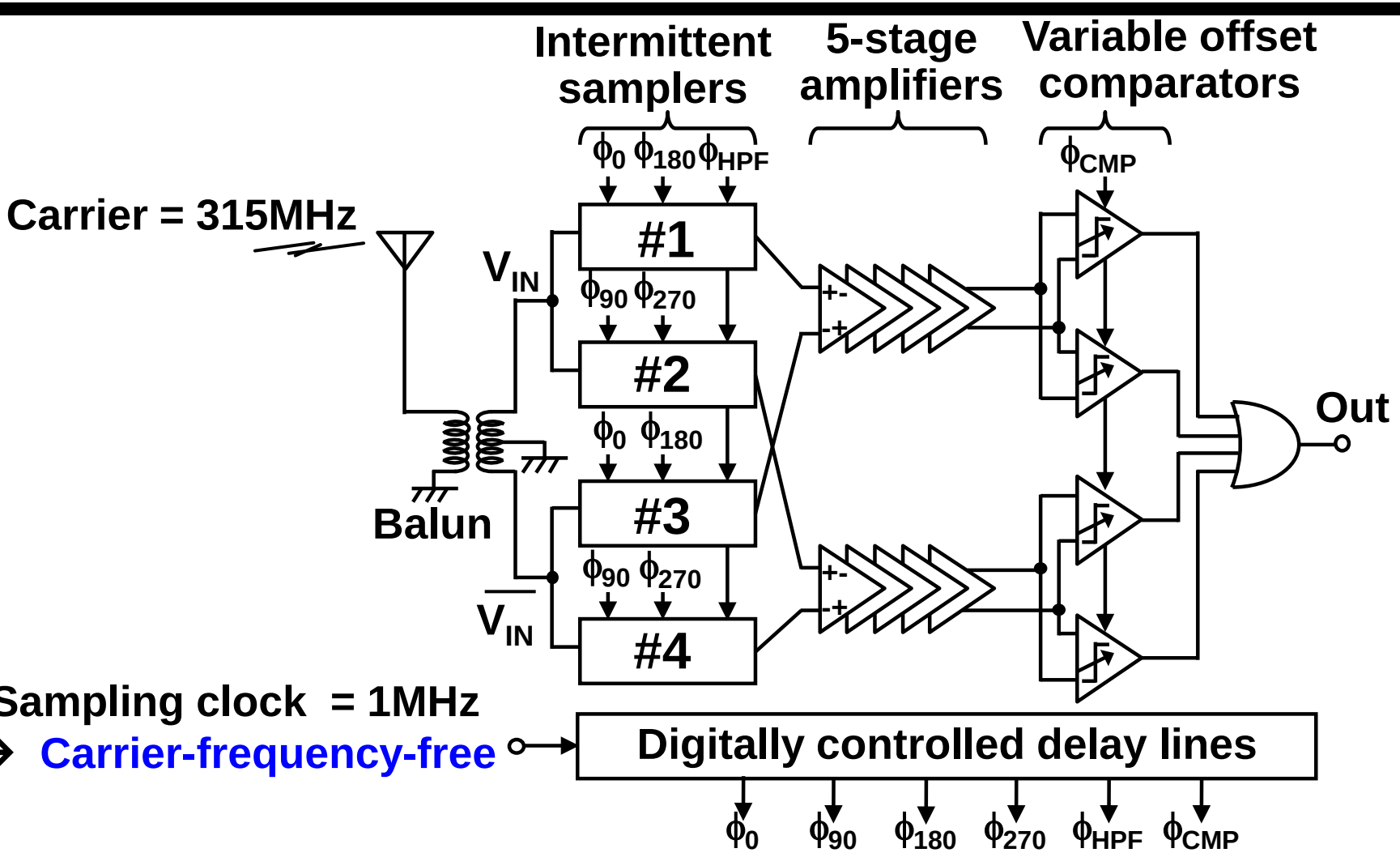


Target transceiver

Frequency	315MHz
Modulation	OOK
TX output power	-20dBm
RX sensitivity	-55dBm
Energy	50pJ/bit

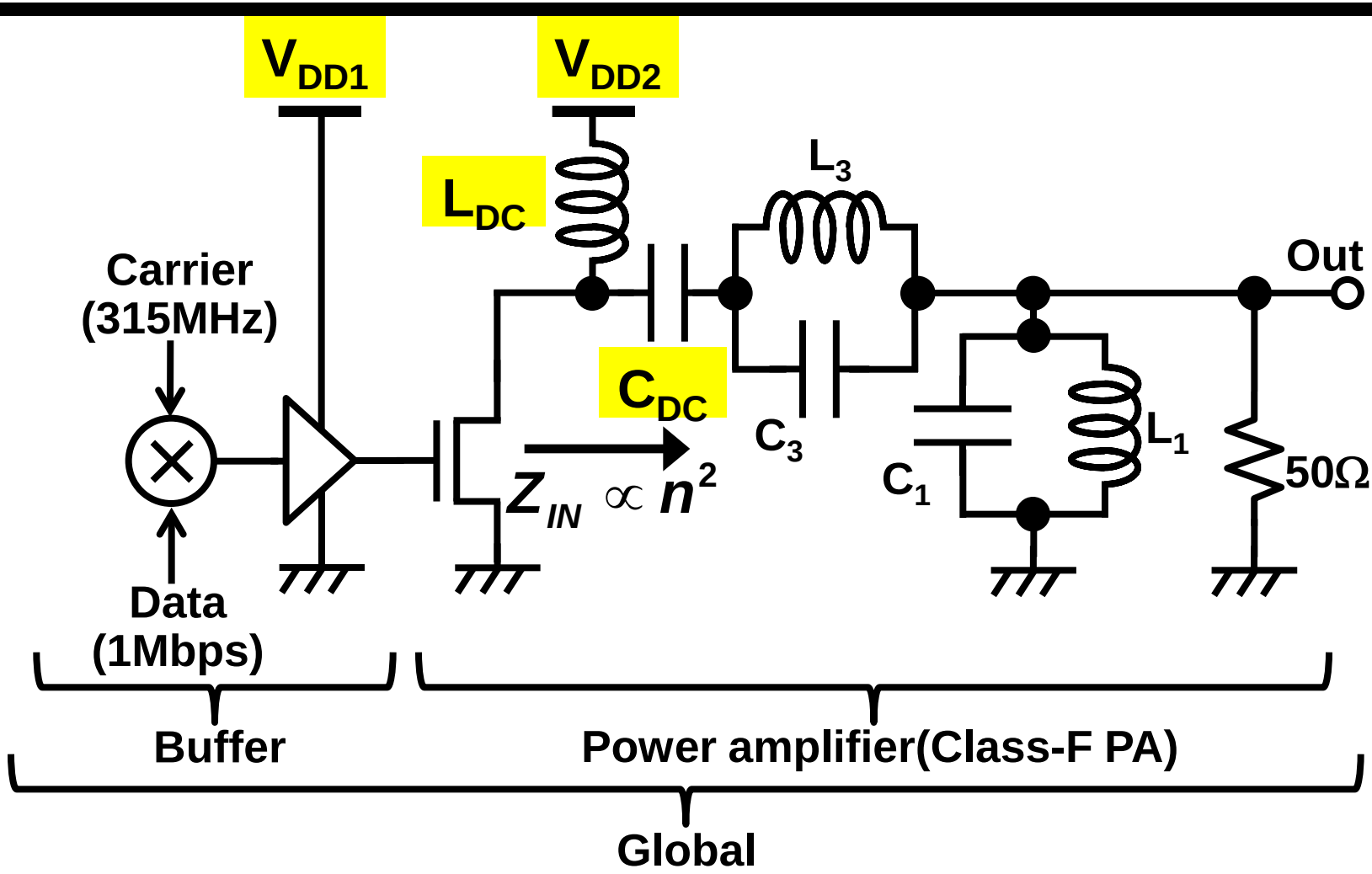


Block diagram of all 0.5V RX



Only 1-MHz clock instead of a 315-MHz carrier frequency is supplied to RX for sampling clock. RX input (V_{IN}) is directly sampled by intermittent samplers without LNA.

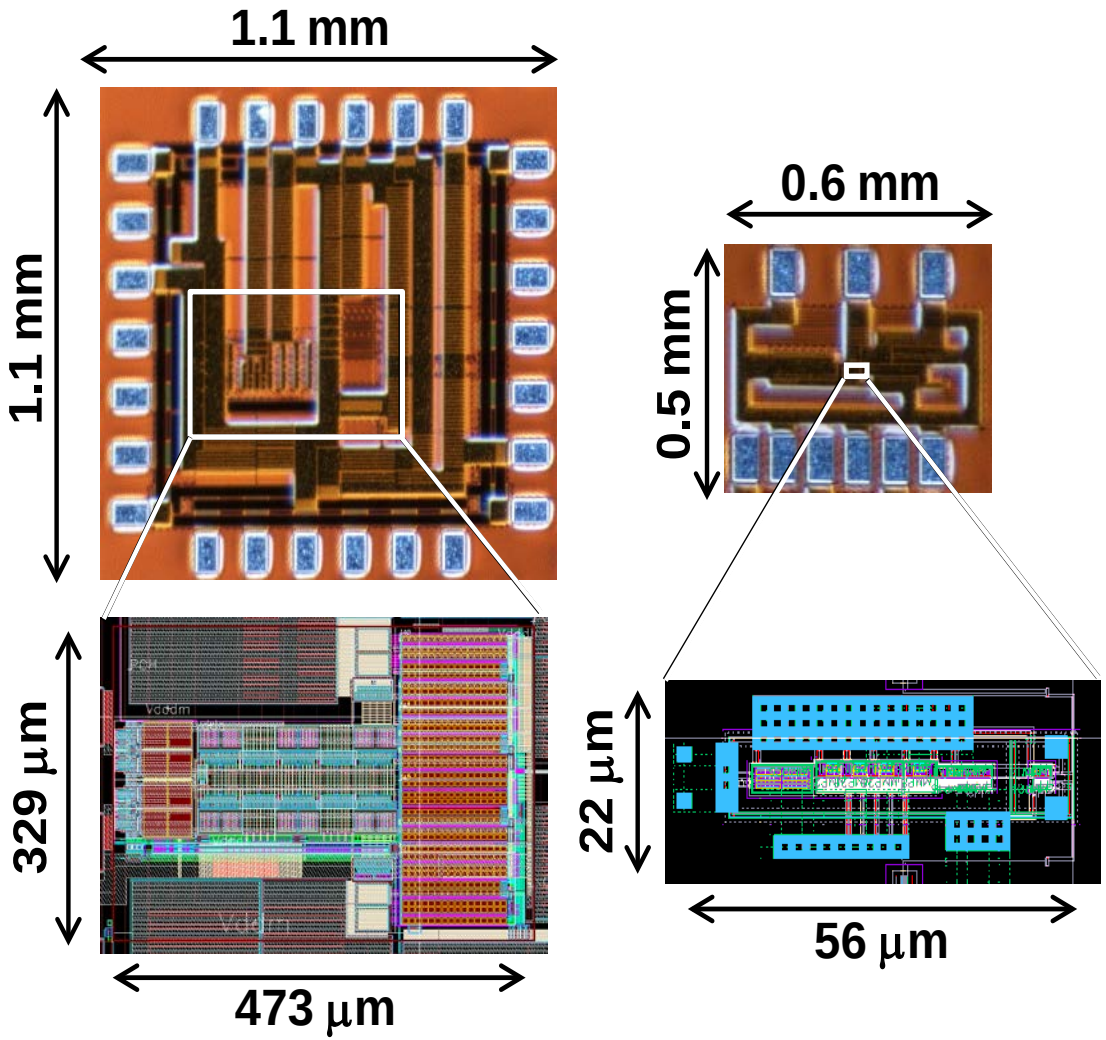
Schematic of dual V_{DD} TX with class-F PA



Minimize global power consumption of TX at P_{OUT} =-20dBm.

➔Dual V_{DD} scheme optimizes V_{DD1}, V_{DD2}, L_{DC}, and C_{DC} at P_{OUT} =-20dBm.

Die photo and layout



RX

TX

40nm CMOS

Performance summary

		Unit	[3]	[4]	This work
CMOS technology		nm	90	130	40
Supply voltage	RX	V	1, 1.2	-	0.5
	TX	V	1, 1.2	1	0.52, 0.2
Carrier frequency		MHz	2400	400	315
Data rate		Mbps	5	0.2	1
Modulation		-	OOK	FSK	OOK
RX sensitivity		dBm	-75	-	-55
TX output power		dBm	0	-17	-20
Power	RX	μW	534	-	38
	TX	μW	253	90	36
Energy	RX	pJ/bit	134	-	38
	TX	pJ/bit	2530	450	36

Our transceiver achieves the lowest energy of 38pJ/bit to date. The newly proposed intermittent sampling and dual V_{DD} scheme reduce the power of RX and TX to 1/315 and 2/3.