A 24.5-53.6pJ/pixel 4320p 60fps H.264/AVC Intra-Frame Video Encoder Chip in 65nm CMOS

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Next-generation HDTV

- **Resolution**
  - SD
  - 720p
  - 80p
  - 4Kx2K
  - Ultra HDTV (Super Hi-Vision) ≥7680 pixels

- Frame Rate
  - 24~30fps
  - ≥60fps
Block Diagram

Intra Prediction Engine

Coarse Mode Decision → candidate modes → Fine Mode Decision → REC

Source Pixels

CABAC Engine

Arithmetic Encoding → Context Model → B Split → Binarization

Coded Bits

Async. FIFOs

recon. pixels

bypass bins
Architecture Optimization

• **Intra Prediction**
  – Coarse-to-fine mode decision
  – Interlaced block reordering
  – Probability-based reconstruction
  – 74% overall complexity reduction

• **CABAC**
  – Pre-normalization
  – Hybrid path coverage
  – Bypass bin splitting
  – 31% performance increase
# Chip Specification & Photo

<table>
<thead>
<tr>
<th>Specification</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>e-Shuttle 65nm CMOS</td>
</tr>
<tr>
<td>Die area</td>
<td>8.82mm²</td>
</tr>
<tr>
<td>Core area</td>
<td>2.07mm²</td>
</tr>
<tr>
<td>Density</td>
<td>75.85%</td>
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<tr>
<td>Logic/SRAM</td>
<td>678.8K gates/27.1KB</td>
</tr>
<tr>
<td>Max. resolution</td>
<td>7680x4320p 60fps</td>
</tr>
<tr>
<td>Max. pixel rate</td>
<td>1991Mpixels/s</td>
</tr>
<tr>
<td>Max. CABAC rate</td>
<td>1.41Gb/s</td>
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</tbody>
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**Measured core power**
- 106.7mW @ 1.20V, 260MHz/330MHz* (4320p60)
- 15.1mW @ 0.90V, 65MHz/65MHz* (2160p60)
- 6.1mW @ 0.80V, 33MHz/33MHz* (2160p30)
- 2.0mW @ 0.80V, 9MHz/9MHz* (1080p30)

* Freq\_INTRA/Freq\_CABAC
Summary

• UHDTV Intra Encoder for H.264/AVC
  – 1991Mpixels/s, at least 9.4x faster previous designs
  – 1.41Gb/s CABAC improved by 31%

• Power Dissipation
  – 106.7mW for 4320p60
  – 2mW for 1080p30
  – 24.5~53.6pJ/pixel energy efficiency
  – At least 7x better power efficiency than previous designs
    (at least 3x better excluding technology factors)