A 0.35-0.8V 8b 0.5-35MS/s 2bit/step Extremely-Low Power SAR ADC

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1bit/step & 2bit/step SAR ADC

2x speed improvement

- \( n \) bit conversion with \( n/2 \) cycles

Three-fold of analog elements required

- 1.5x power, 3x area

[ref] Z. Cao, JSSC 2009

SAR: Successive Approximation Register
Threshold configuring comparator

- An offset added by intent
- Only 1 reference generator required

Low Power and high speed
Comparators are activated successively

Cycle 1
Output: 10xx
1001
Wide Range Threshold Configuring

- $V_{DD}/2$ biased current source
  - Input signal common mode is $V_{DD}/2$
  - Comparator holds supply voltage noise immunity

Simplified Comparator Schematic
Comparison with state-of-the-art works

Power Efficiency [fJ/conv.step] vs. Sampling Frequency [kS/s]

- ISSCC2011
- ESSCIRC2011
- VLSI 2011
- ISSCC2012
- ESSCIRC2011
- VLSI 2012
- This Work

Voltage levels:
- 0.3 V
- 0.4 V
- 0.5 V
- 0.6 V
- 0.7 V
- 0.8 V