

ASP-DAC'2013 University LSI Design Contest

1D-3

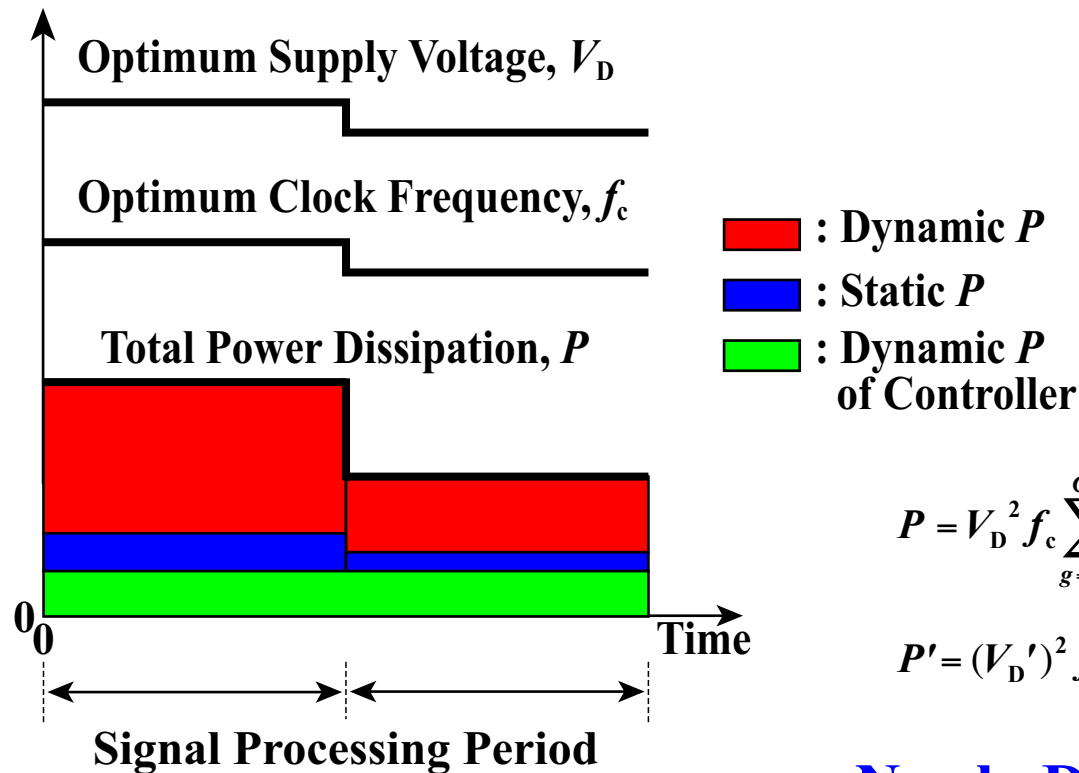
**A Low Power Multimedia Processor Implementing
Dynamic Voltage and Frequency
Scaling Technique**

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Dynamic Voltage and Frequency Scaling Technique



$$P = V_D^2 f_c \sum_{g=1}^G (\alpha_g C_{Lg}), \quad f_c' = \eta f_c, \quad V_D' \propto \eta V_D, \quad \eta < 1$$

$$P' = (V_D')^2 f_c' \sum_{g=1}^G (\alpha_g C_{Lg}) = \eta^3 V_D^2 f_c \sum_{g=1}^G (\alpha_g C_{Lg}) = \eta^3 P$$

Newly Developed Techniques in implementing the DVFS scheme :

1. Block Motion Estimation (BME)

Algorithm

2. DVFS Controller

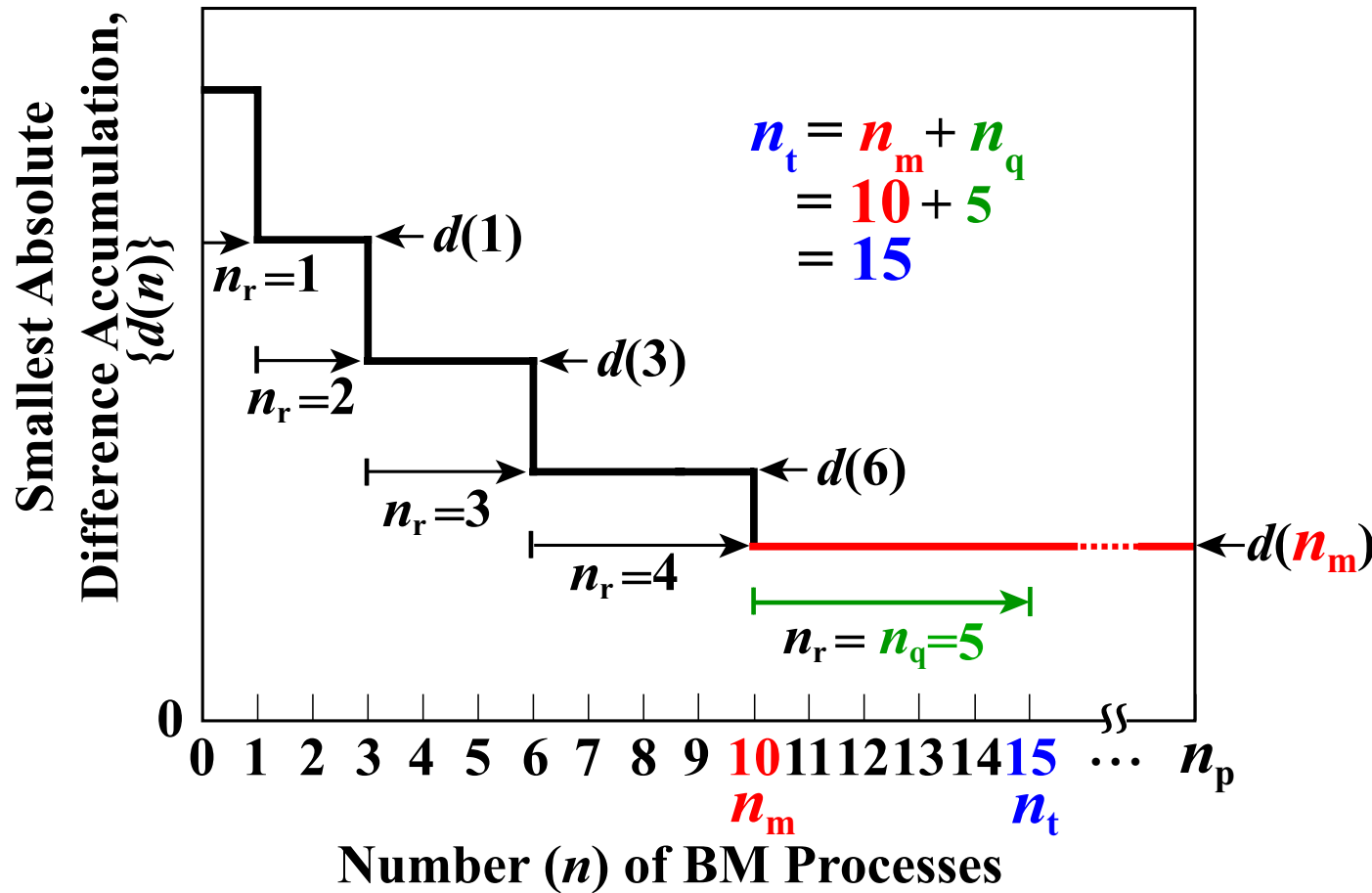
3. Built-in DC/DC Level Converter

4. PLL Clock Driver

DVFS Technique:

To supply optimum supply voltage (V_D) & optimum clock frequency (f_c) to the processor.

Adaptively Assigned Breaking-off Condition (A²BC) Block Motion Estimation (BME) Algorithm



$d(n_m)$:
Minimum absolute
difference
accumulation

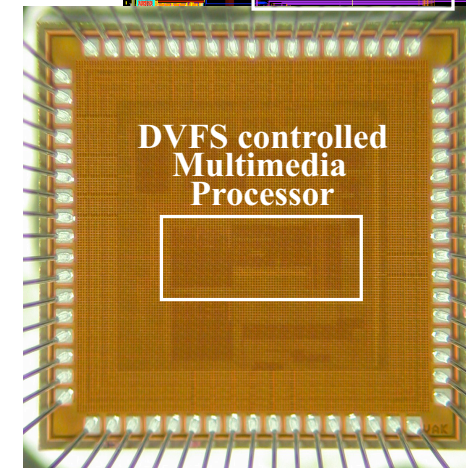
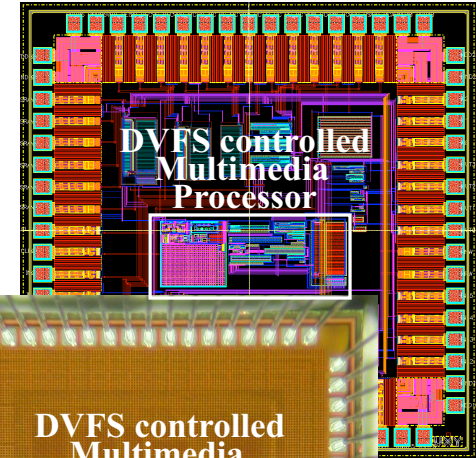
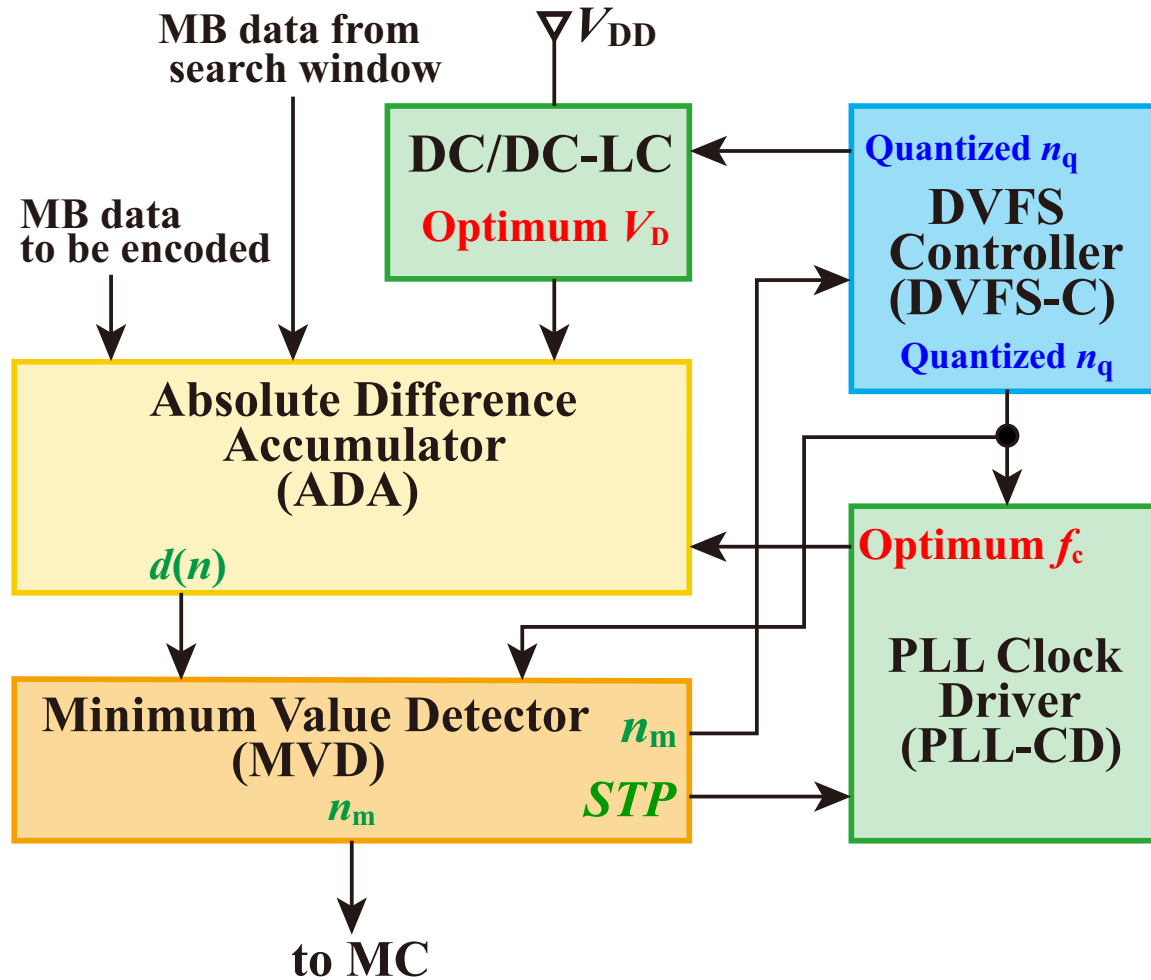
n_m :
Number of Block
Matching (BM)
processes at $d(n_m)$
is found

n_t :
Total number of
BM processes

n_r :
Number of BM
processes after the
value of $d(n)$
decreases

n_q :
Assigned Number
of BM processes

DVFS Controlled Multimedia Processor



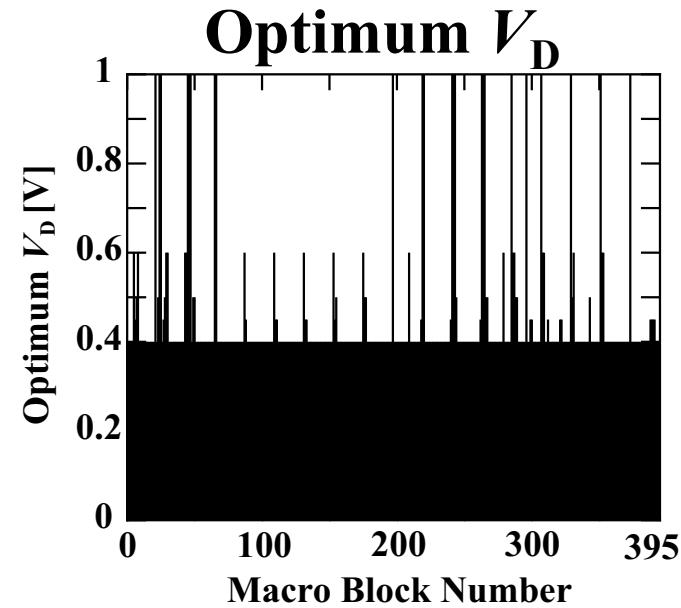
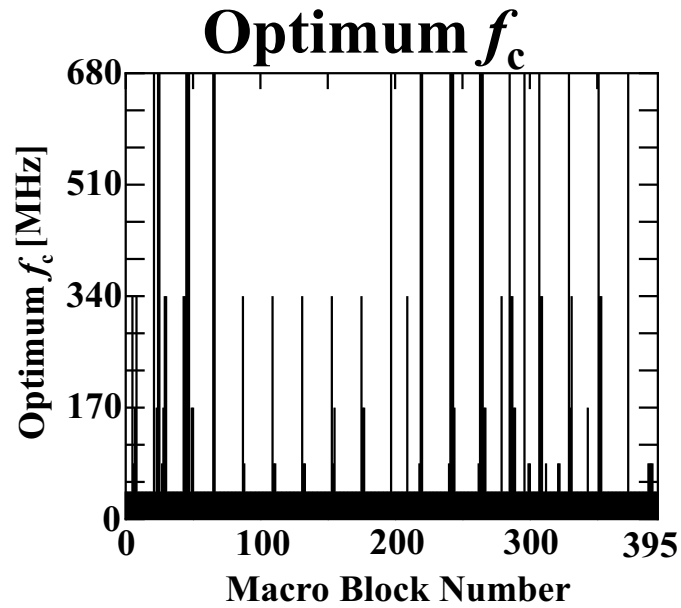
Chip Size: 2.5 mm × 2.5 mm

Si Area: 970 μm × 330 μm

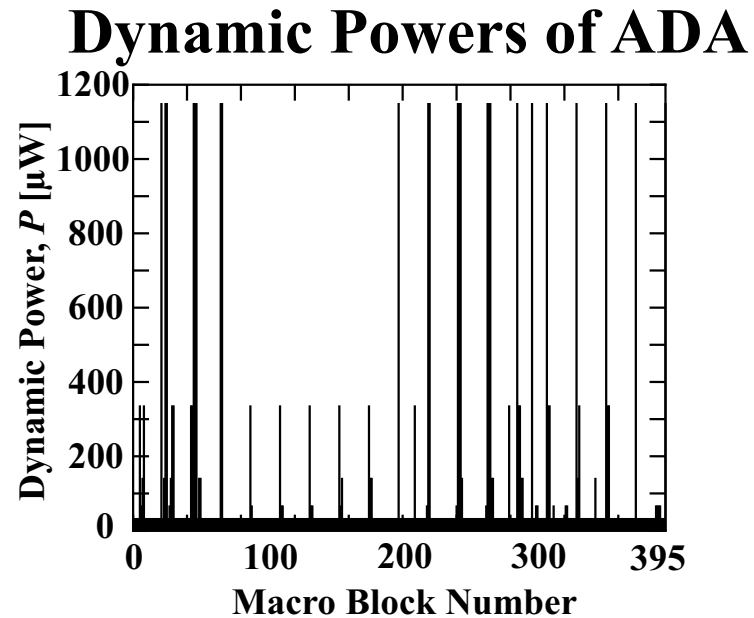
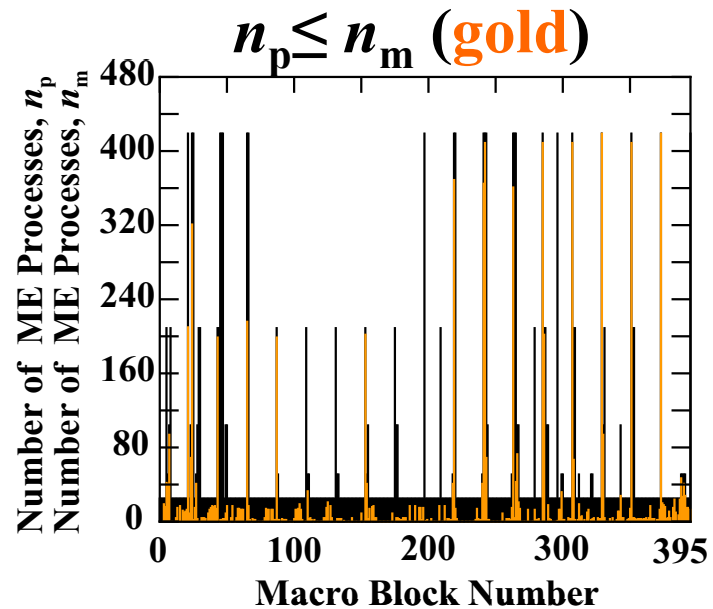
No. of MOSFETs: 50,000

Clock Frequency: 680 MHz

Characteristics of A²BC & DVFS for Each MB



198th Frame
of “Foreman”



Power Dissipation of DVFS Multimedia Processors

	Conventional	DVFS Controlled
Dynamic Power of ADA [μW]	1,177.5	34.74* ~ 92.50**
Dynamic Power of Peripheral Circuits [μW]	2,628.3	2.454* ~ 5.598**
Static Power of Peripheral Circuits [μW]	0	1.294* ~ 1.264**
Total Power [μW]	3,805.8	38.488* ~ 99.362**
Ratio [%]	100	1.011* ~ 2.611**

($V_{\text{DD}} = 1 \text{ V}$)

* Akiyo ~ **Foreman