

Poster ID : 1D-4

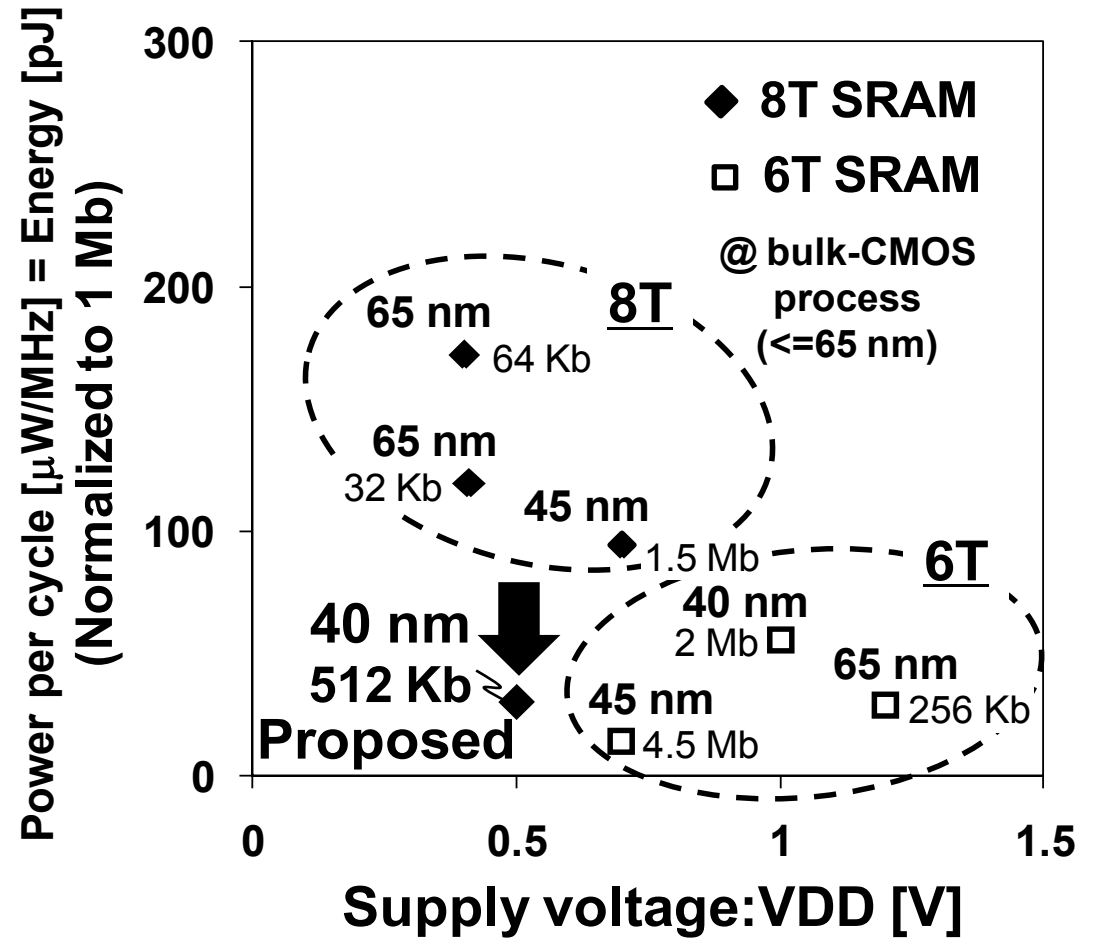
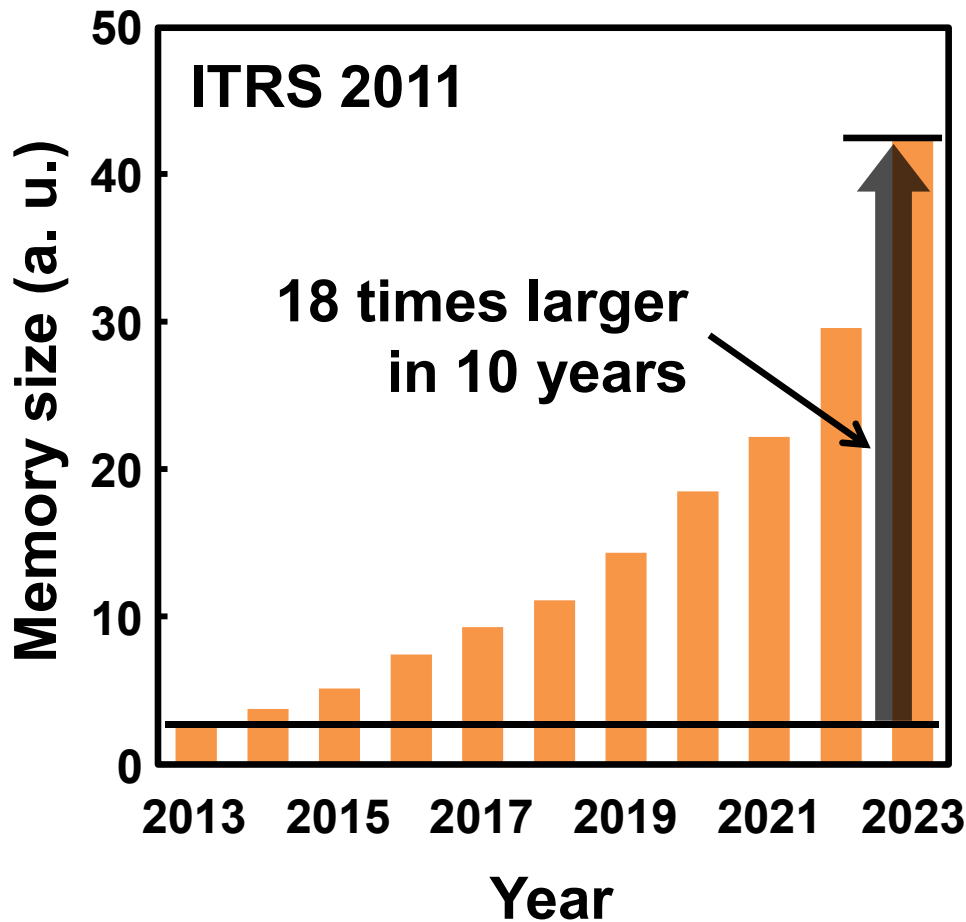
A 40-nm 0.5-V 12.9- μ W/MHz 8T SRAM Using Low-Power Disturb Mitigation Technique

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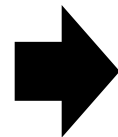
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Background

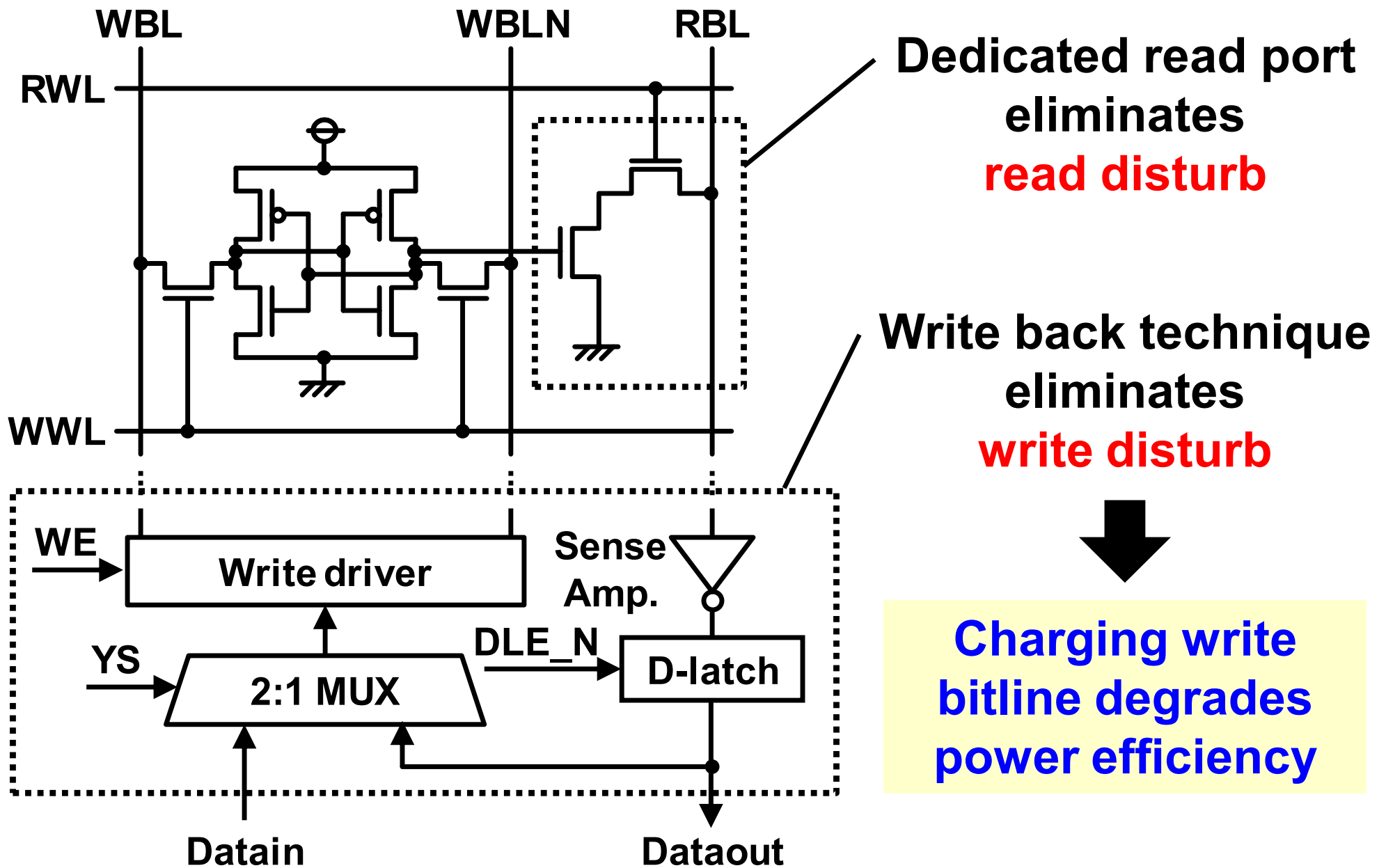


Increasing memory size

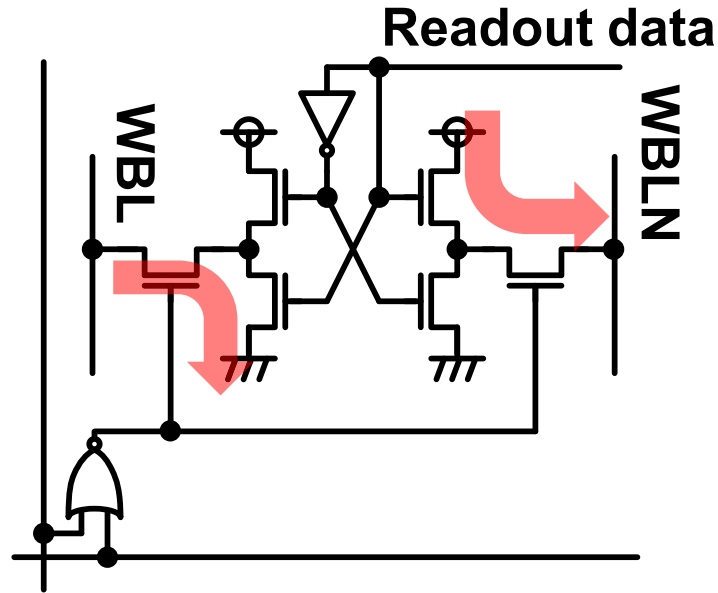
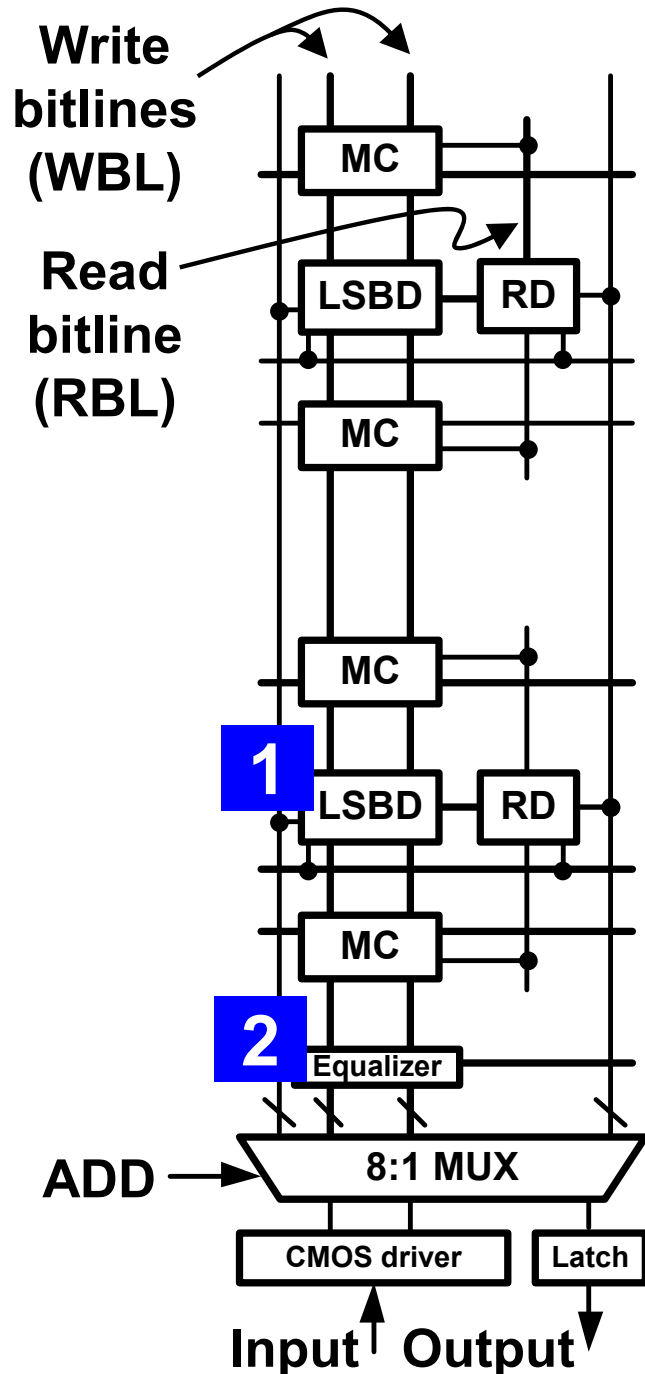


Low-voltage and low-power SRAM is required

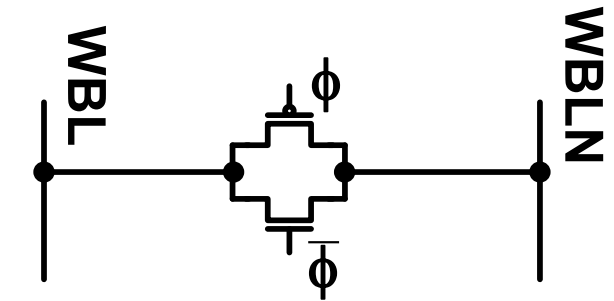
Conventional write back technique



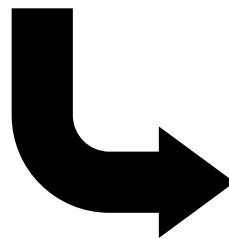
Proposed disturb mitigation technique



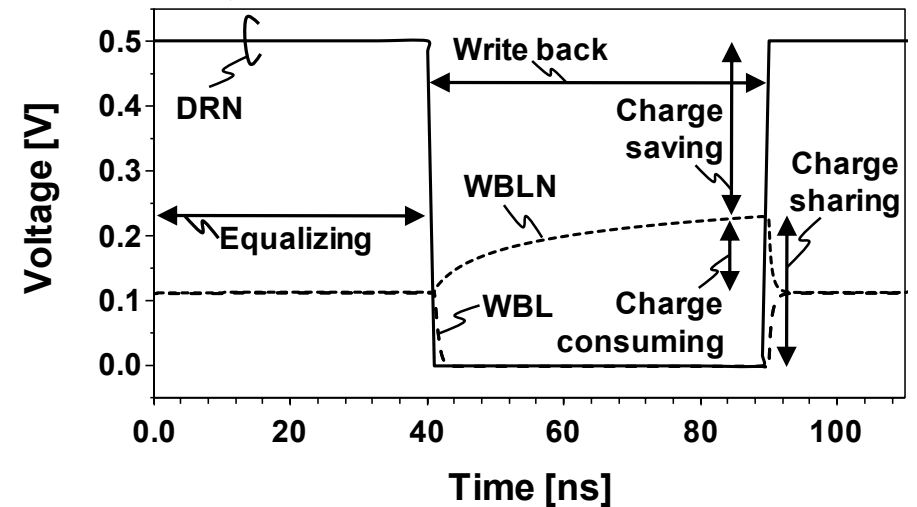
1. Low-swing bitline driver (LSBD)



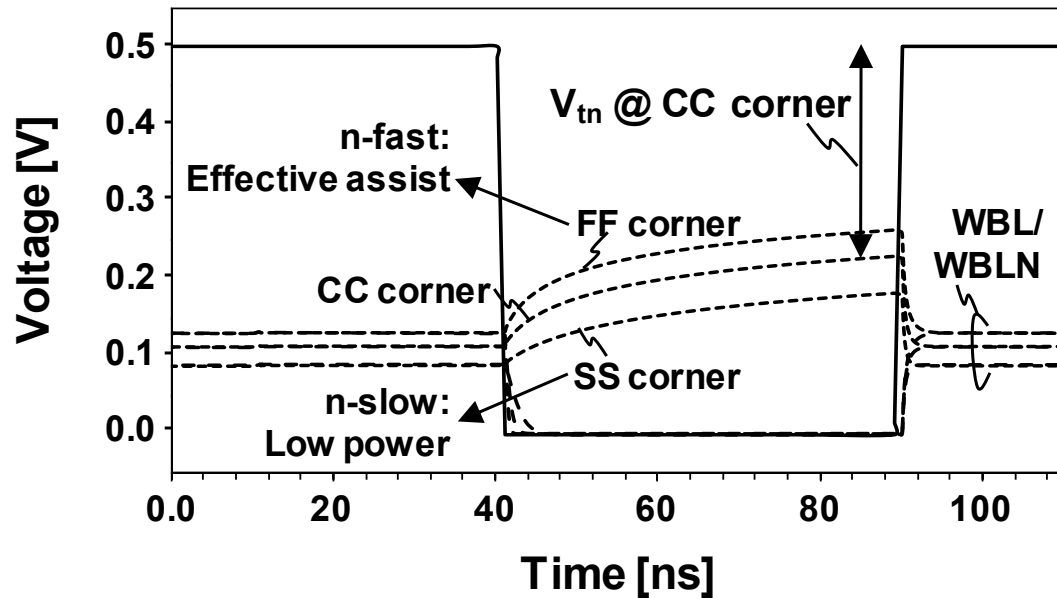
2. Precharge-less equalizer



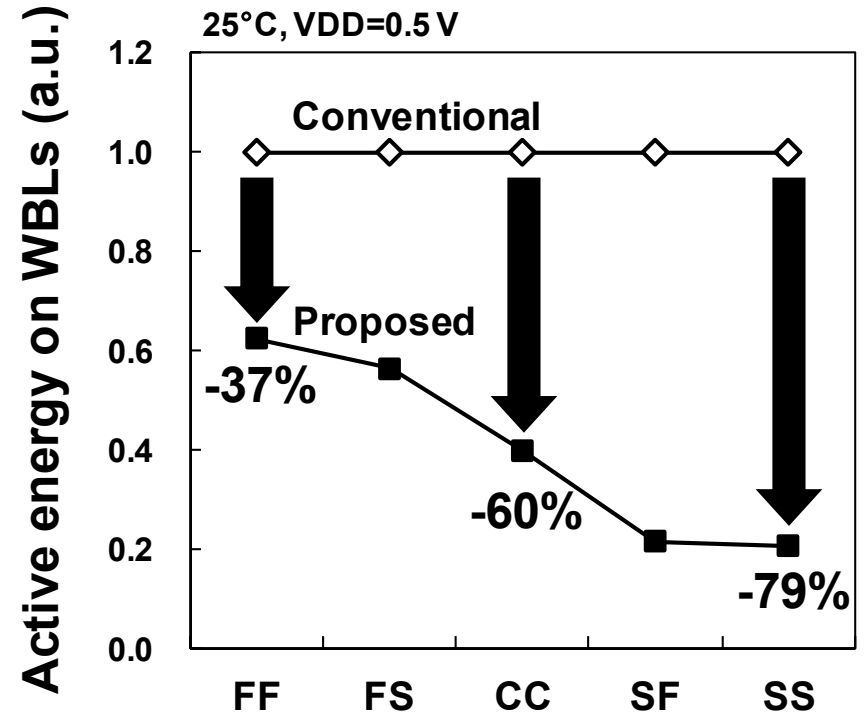
Low-swing write back



Active energy reduction on WBLs



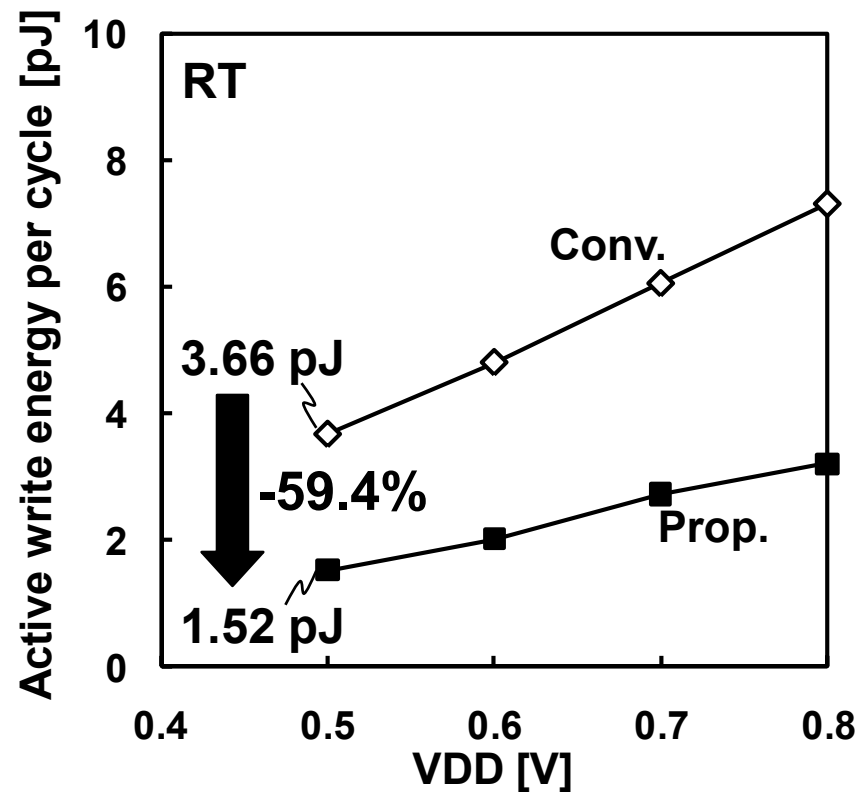
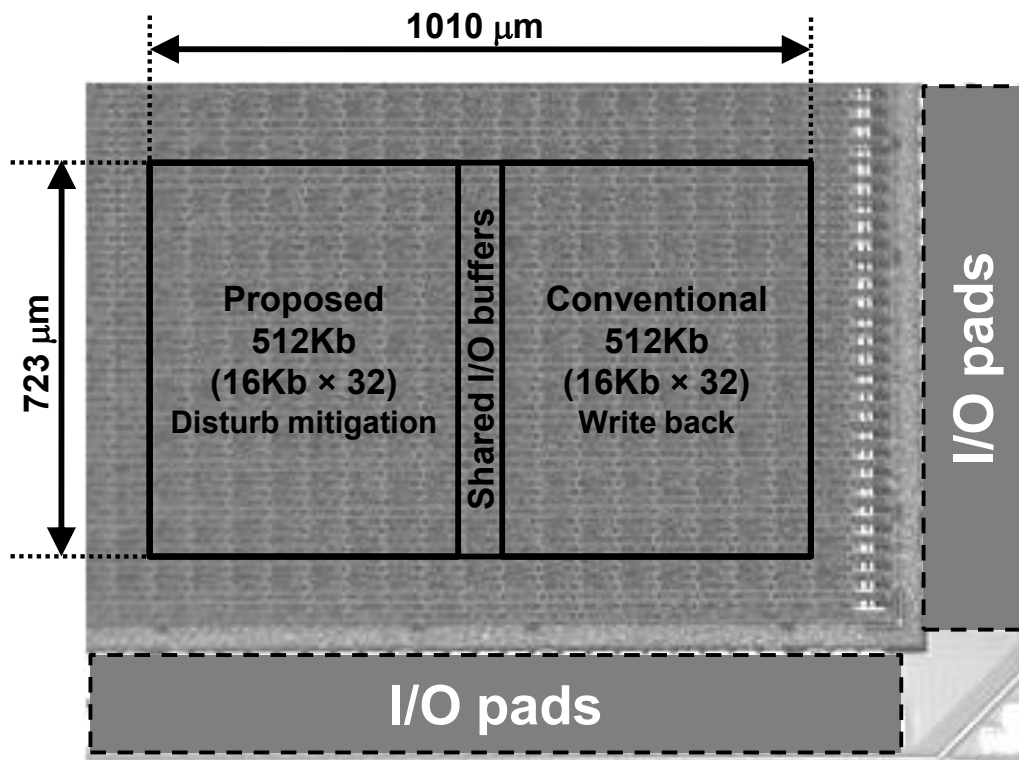
WBL swing depends on a process corner



60% active energy reduction on WBLs

Measurement results

1D-4



40-nm 512Kb 8T SRAM
test chip

59.4% active energy
reduction in total