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A 40-nm 0.5-V 12.9-μW/MHz 8T SRAM Using Low-Power Disturb Mitigation Technique

Shusuke Yoshimoto\textsuperscript{1}, Masaharu Terada\textsuperscript{1},
Shunsuke Okumura\textsuperscript{1}, Toshikazu Suzuki\textsuperscript{2},
Shinji Miyano\textsuperscript{2}, Hiroshi Kawaguchi\textsuperscript{1},
and Masahiko Yoshimoto\textsuperscript{1}

\textsuperscript{1}Kobe University, Kobe, Japan
\textsuperscript{2}Semiconductor Technology Academic Research Center (STARC), Yokohama, Japan
Increasing memory size → Low-voltage and low-power SRAM is required.
Conventional write back technique

- Dedicated read port eliminates read disturb
- Write back technique eliminates write disturb

Charging write bitline degrades power efficiency
Proposed disturb mitigation technique

1. Low-swing bitline driver (LSBD)
2. Precharge-less equalizer

Low-swing write back
Active energy reduction on WBLs

- WBL swing depends on a process corner

- 60% active energy reduction on WBLs
Measurement results

Proven
512Kb
(16Kb × 32)
Disturb mitigation

Conv.
512Kb
(16Kb × 32)
Write back

Active write energy per cycle [pJ]

0 1 2 3 4 5 6 7 8 9 10
VDD [V]

1.52 pJ
3.66 pJ
-59.4%

Prop.

Conv.

40-nm 512Kb 8T SRAM test chip

59.4% active energy reduction in total