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I-LUTSim: An Iterative Look-Up Based Thermal Simulator for 3-D ICs

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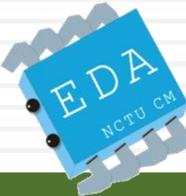

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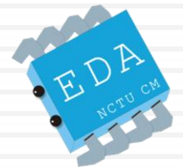
Outline

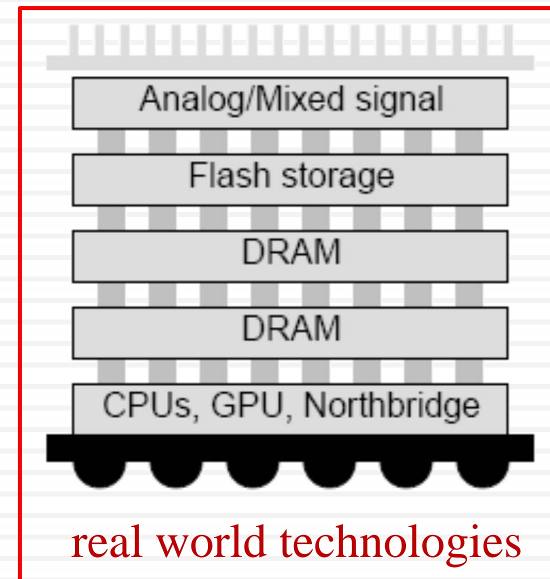
- Thermal Issues in 3-D ICs
- Motivation & Problem Formulation
- I-LUTSim
- Experimental Results & Summary

Thermal Issues in 3-D ICs

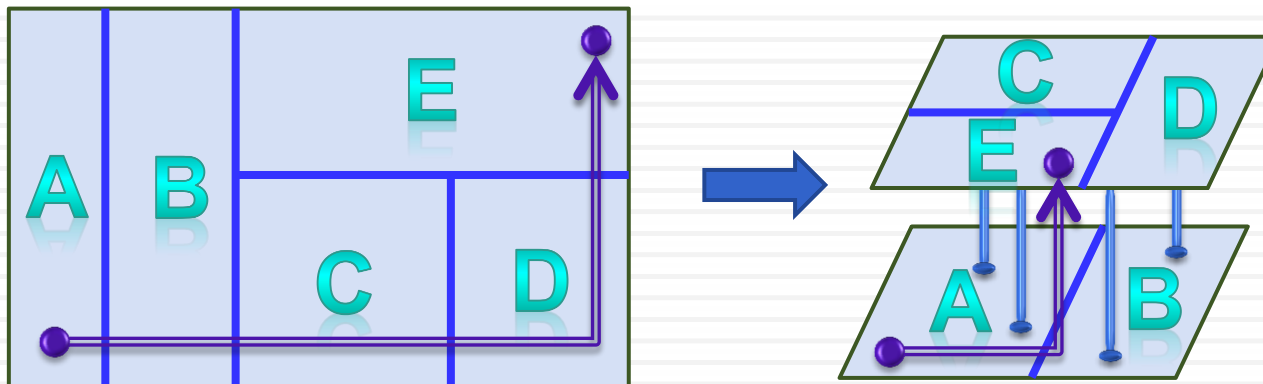


Why Staking Chips in 3-D?

- Pros of 3-D IC
  - Reduce the global wire-length
  - Reduce the power consumption
  - Increase the chip density
  - Heterogeneous integration

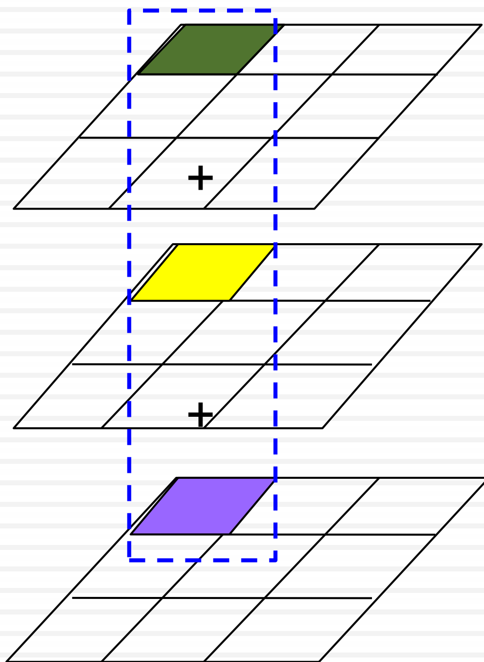


real world technologies

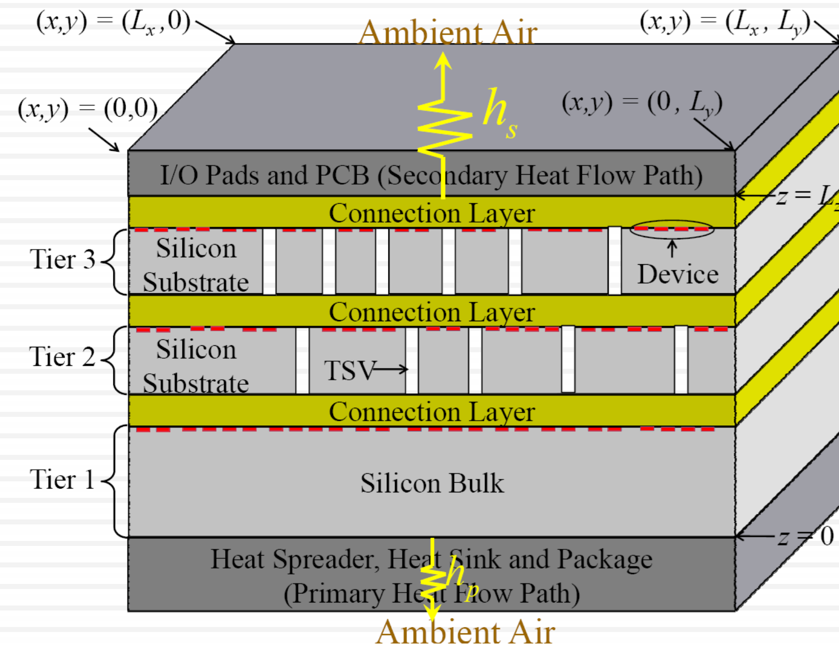


Accumulated Power

- Thermal issues of 3-D ICs will be worse than that of 2-D ICs



Accumulating power density is higher than that of 2-D ICs

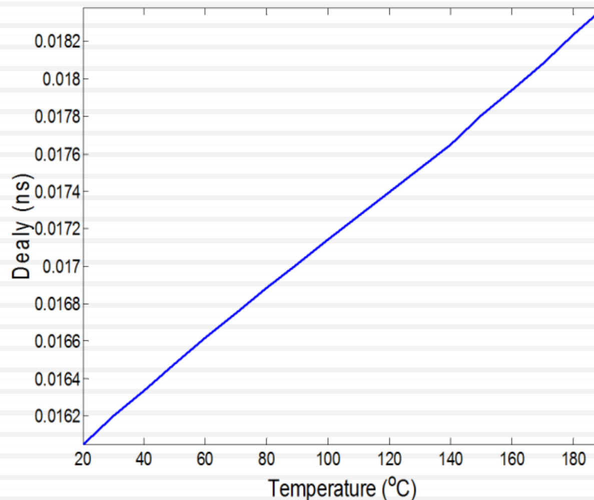


Low thermal conductivity of dielectric in interconnect layers

Thermal Issues (1/2)

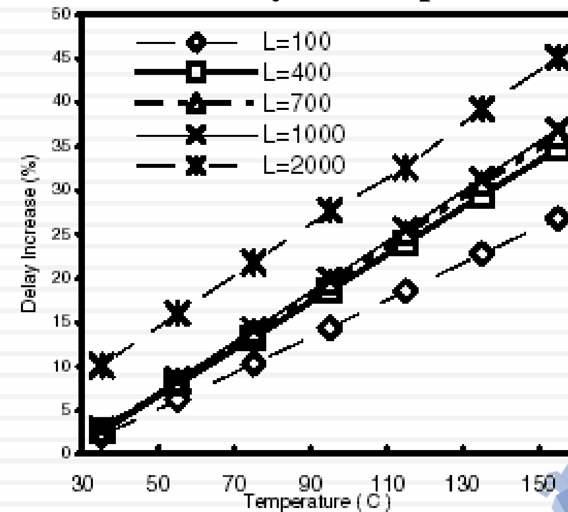
- Thermal related issues in VLSI design
  - The delay of devices and wires varies as temperature increases
  - The non-uniform temperature distribution causes the non-uniform wire and gate delay

Gate Delay vs. Temperature

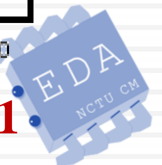


HSPICE simulation data @65nm note for a NAND gate

Wire Delay vs. Temperature

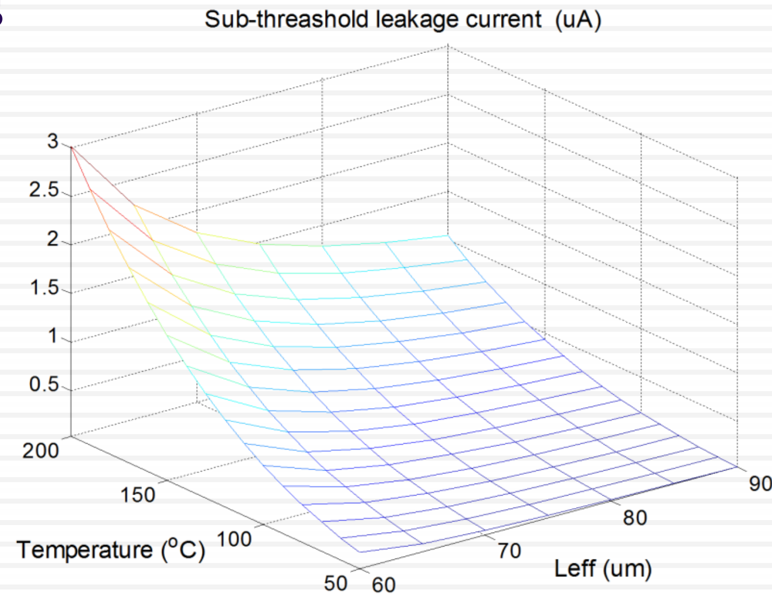


K. Banerje@ISPD 2001



Thermal Issues (2/2)

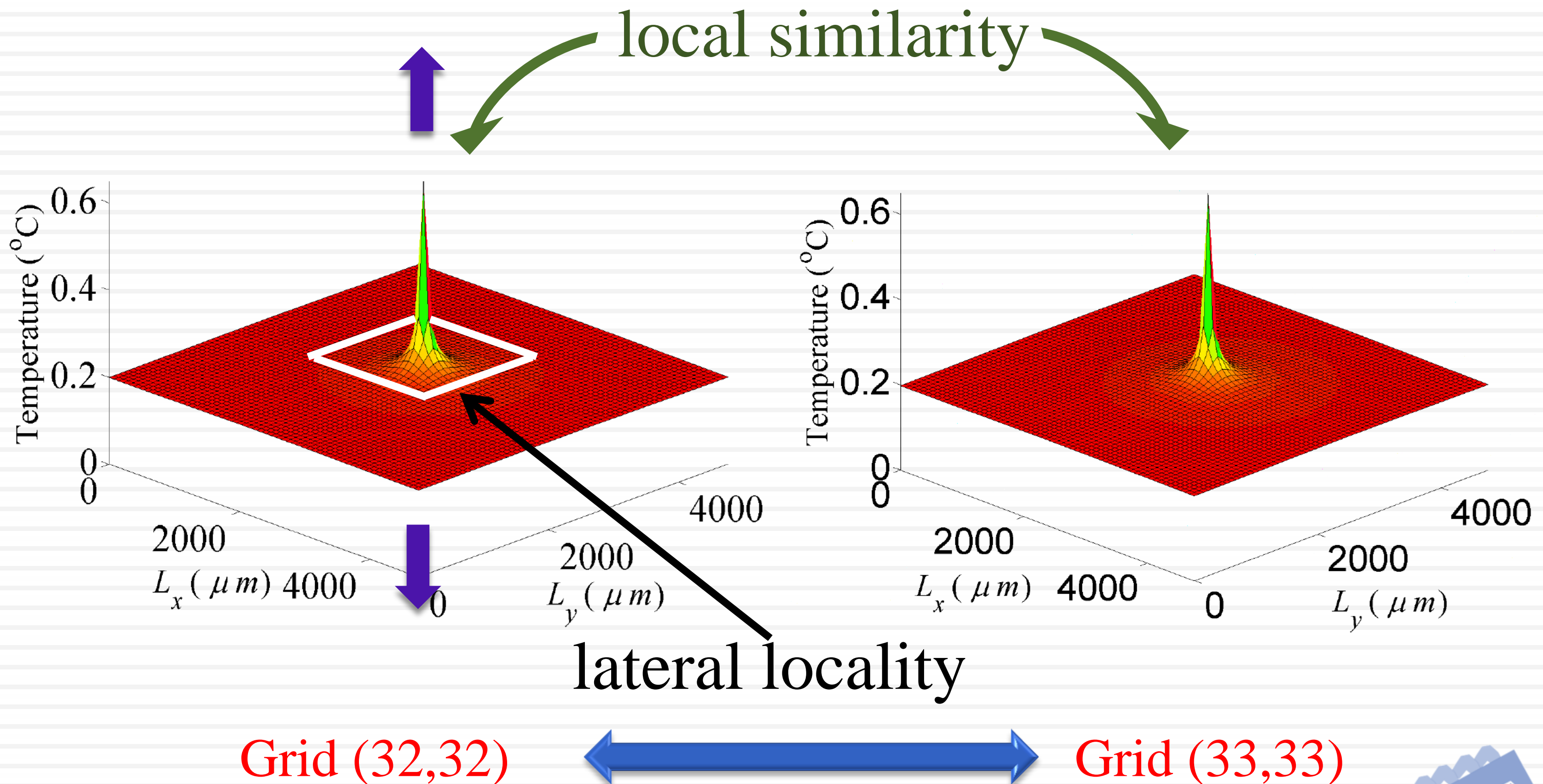
- Thermal related issues in VLSI design
  - The mean-time-to-failure (MTTF) of wires exponentially decreases as temperature increases
  - Leakage current of devices exponentially increases as temperature increases
  - Thermal Runaway



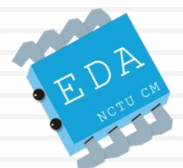
HSPICE simulation data @65nm note

Thermal Properties

- ***Lateral Locality*** and ***Local Similarity***



Motivation & Problem Formulation

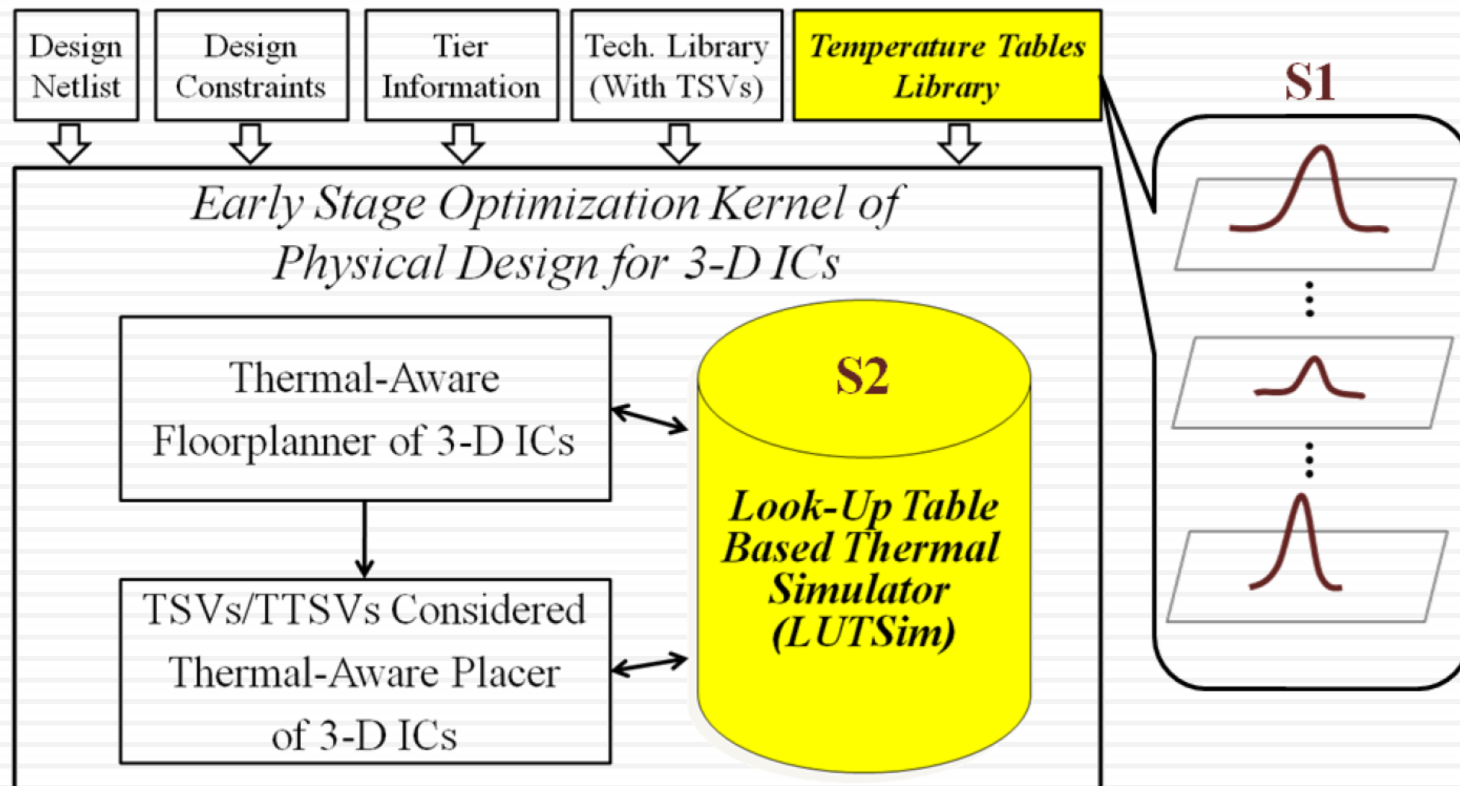


Motivation (1/2)

- During the early physical design stages as floorplan /placement
  - The macros/cells will be moved repeatedly
  - The temperature distribution needs to be re-analyzed after each moving
  - Solving the large scale modified nodal analysis (MNA) system is impractical
  - Need an effective method to calculate the chip temperature without losing the accuracy

A Look-up Table Based Thermal Simulator

Motivation (2/2)



- For timing analysis: timing library in .lib
- For thermal analysis: need a thermal library

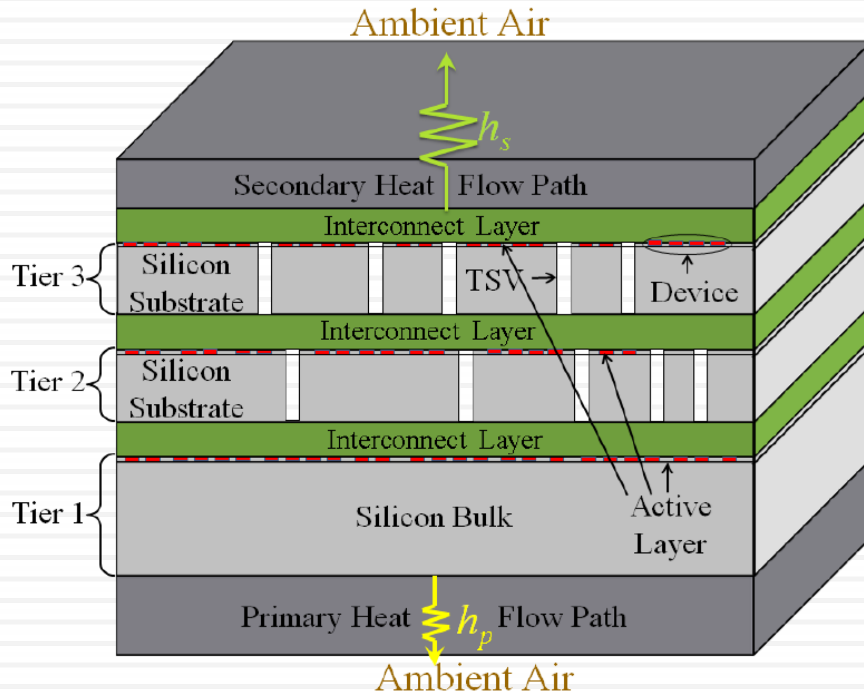
Why Tables Can be Pre-Constructed?

- The following information can be obtained beforehand for table construction
  - Thicknesses of silicon substrates and bulk, and material of TSV/TTSV are manufacturing parameters
  - Tier counts
  - Heat transfer coefficients of heat flow paths along package
  - Effective thermal conductivity of interconnect layers
  - The outline of chip

All can be determined before floorplan stage

Problem Formulation

Thermal model for early design stage



Steady State heat transfer equation

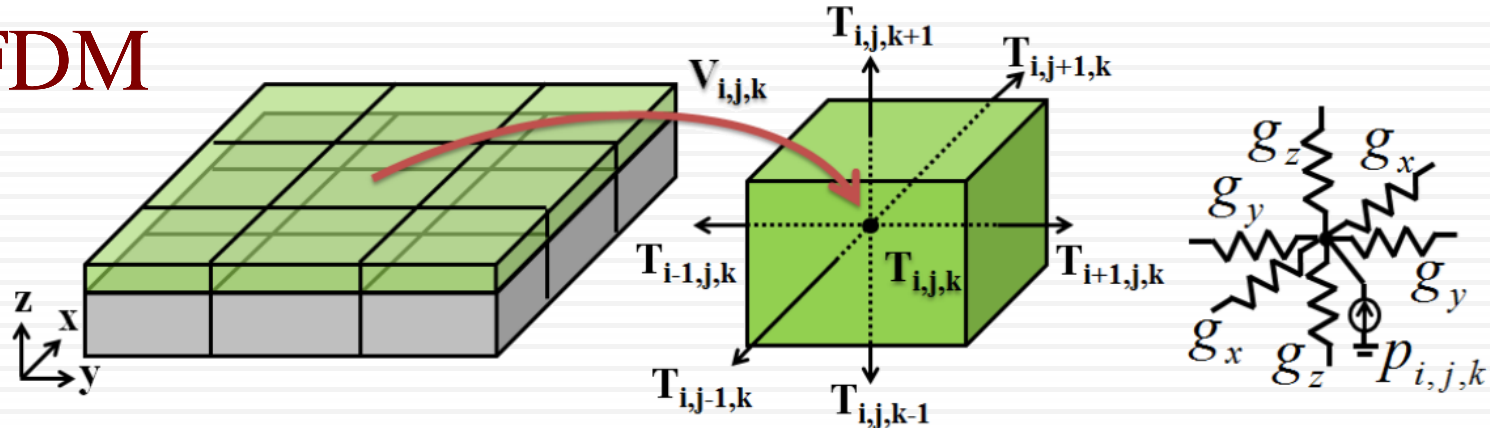
$$\nabla \cdot \left[\kappa(\mathbf{r}) \nabla T(\mathbf{r}) \right] = -p(\mathbf{r})$$

subject to the boundary condition

$$\kappa(\mathbf{r}_{b_s}) \frac{\partial T(\mathbf{r}_{b_s})}{\partial \vec{n}_{b_s}} + h_{b_s} T(\mathbf{r}_{b_s}) = f_{b_s}(\mathbf{r}_{b_s})$$

Spatial Discretization and Duality

FDM



MNA

$$\mathbf{GT} = \mathbf{p}$$

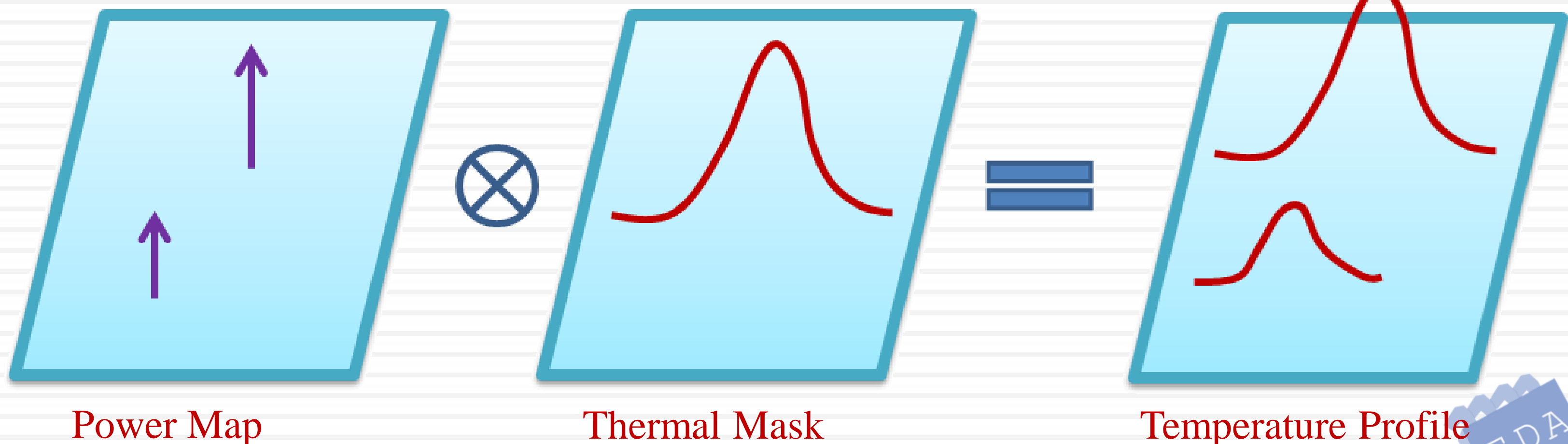
G : thermal conductance matrix
T : vector of nodal temperatures
p : vector of power sources at nodes

Thermal quantity	unit	Electrical quantity	unit
P, Heat flow, power	W	I, Current	A
T, Temperature difference	K	V, Voltage	V
R_{th}, Thermal resistance	K/W	R, Electrical resistance	Ω
C_{th}, Thermal capacitance	J/K	C, Electrical capacitance	F

Previous Works (1/2)

- Power blurring is a superposition based method
  - Calculating temperature profile by performing the convolution of power map and thermal mask
  - Thermal mask can be obtained by
    - FDM/FEM simulation
    - Thermal measurement with infrared camera

Kemper@ THERMINIC07

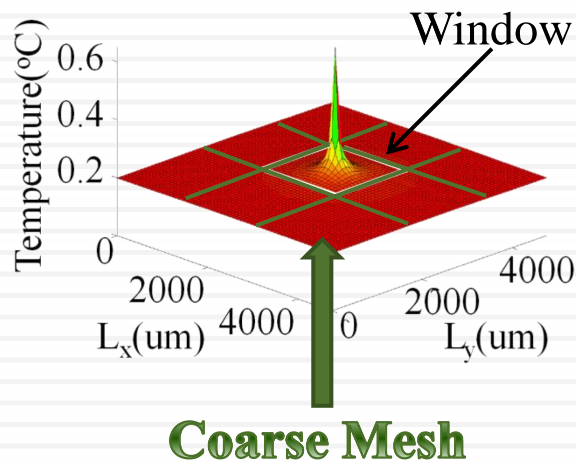


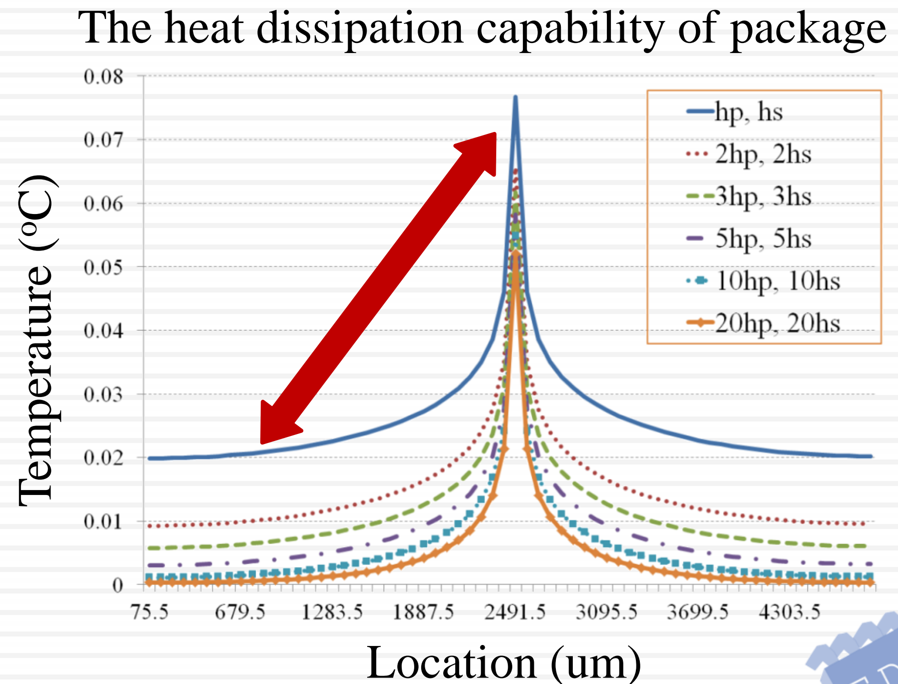
Previous Works (2/2)

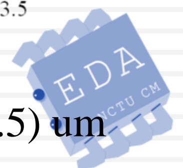
- Ultrafast temperature profile calculation in IC chips
  - Theoretical base: Green's function — Kemper@THERMINIC07
  - Only for 2-D ICs
- Junction-level thermal analysis of 3-D integrated circuits using high definition power blurring — Melamed @TCAD12
  - Extending the power blurring method for 3-D ICs structure
  - Separate response masks are generated for every homogenous environment
  - Circuit with high variations of thermal conductivities will make it less effective or inapplicable

Contributions

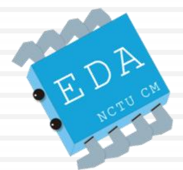
- A double-mesh table is proposed to capture the marginal value of the thermal response
- I-LUTSim only uses one set of homogeneous thermal table library







I-LUTSim



The Kernel of I-LUTSim

- MNA equation for homogenous condition (ignored TSVs/TTSVs)

$$\mathbf{G}_h \mathbf{T}_h = \mathbf{p} \Rightarrow \mathbf{T}_h = \mathbf{G}_h^{-1} \mathbf{p} = \mathbf{m}_0$$

Double-Mesh Table

- MNA equation for in-homogenous condition (with TSVs/TTSVs)

$$(\mathbf{G}_h + \Delta \mathbf{G}_{TSV})\mathbf{T} = \mathbf{p}$$

$$\mathbf{T} = (\mathbf{G}_h(\mathbf{I} + \mathbf{G}_h^{-1} \Delta \mathbf{G}_{TSV}))^{-1} \mathbf{p}$$

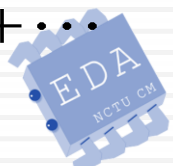
$$= \mathbf{G}_h^{-1} \mathbf{p} + (-1) \mathbf{G}_h^{-1} \Delta \mathbf{G}_{TSV}^{-1} \mathbf{G}_h^{-1} \mathbf{p}$$

$$+ (-1)^2 \mathbf{G}_h^{-1} \Delta \mathbf{G}_{TSV} \mathbf{G}_h^{-1} \Delta \mathbf{G}_{TSV}^{-1} \mathbf{G}_h^{-1} \mathbf{p} + \cdots$$

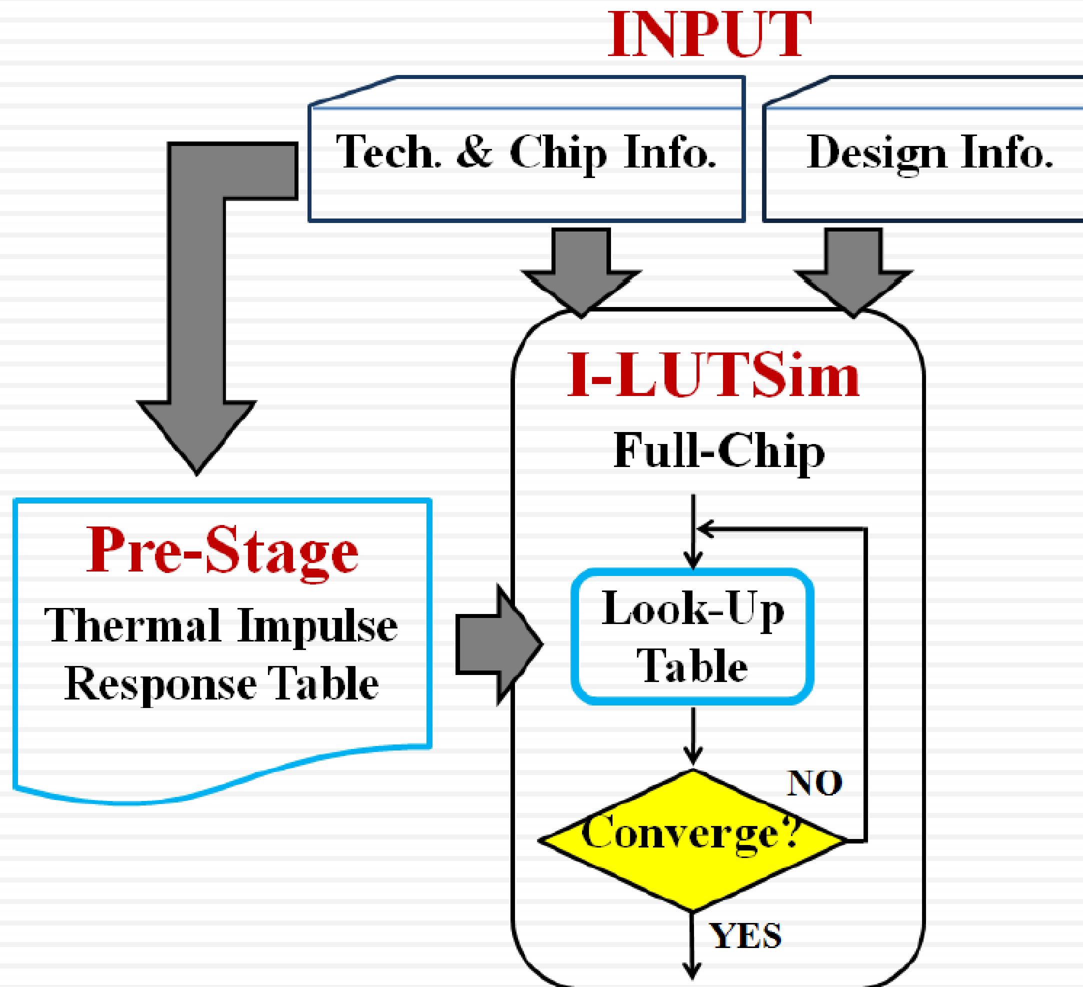
$\mathbf{m}_0$, $\mathbf{m}_1$, $\mathbf{m}_2$, $\mathbf{P}_i$

$$\mathbf{T} = \mathbf{m}_0 + (-1) \mathbf{G}_h^{-1} \Delta \mathbf{G}_{TSV} \mathbf{m}_0 + (-1)^2 \mathbf{G}_h^{-1} \Delta \mathbf{G}_{TSV} \mathbf{m}_1 + \cdots$$

$\mathbf{m}_1$ $\quad$ $\mathbf{m}_2$

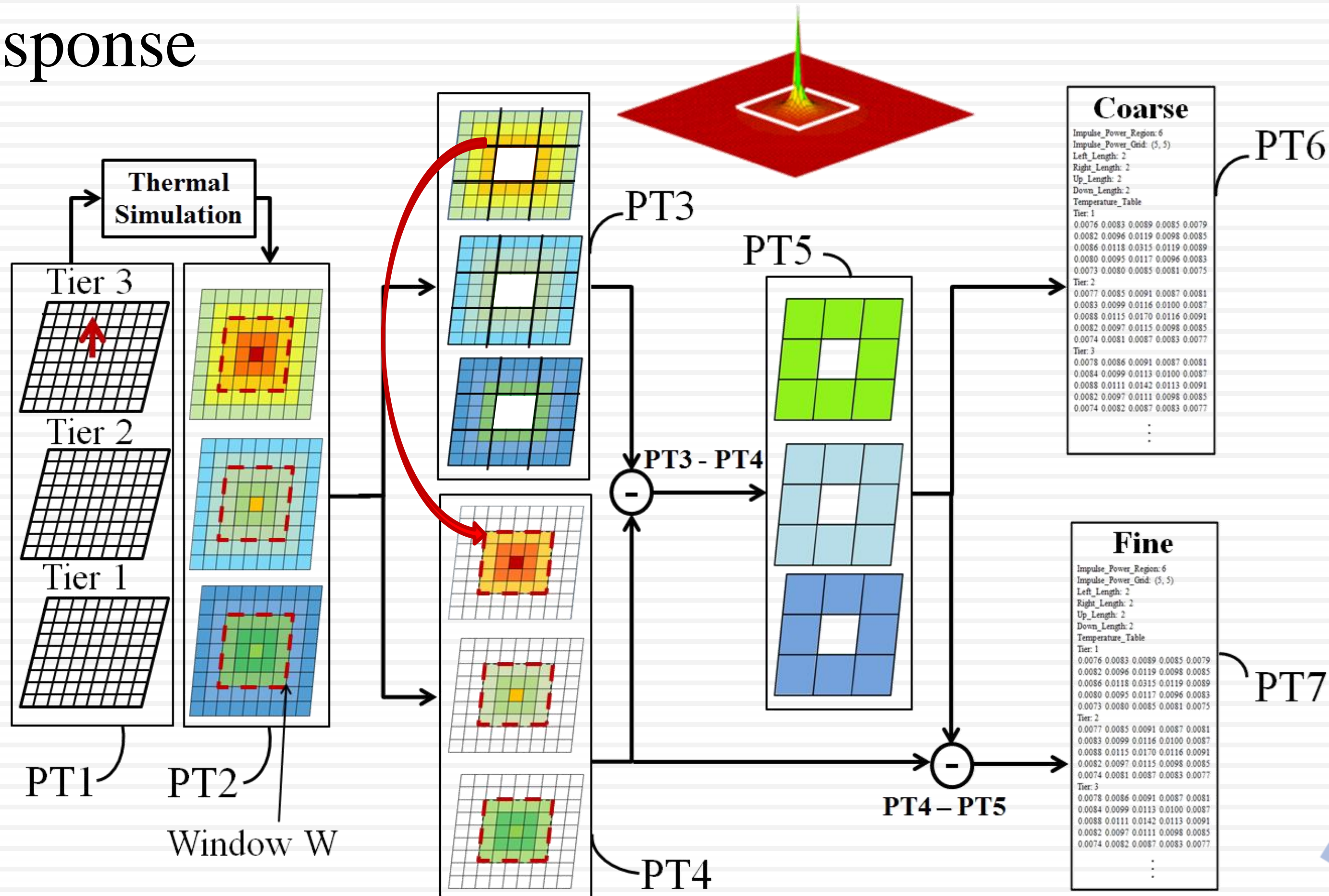


Flowchart



Double-Mesh Table (1/3)

- Double-mesh table of the unit power temperature response



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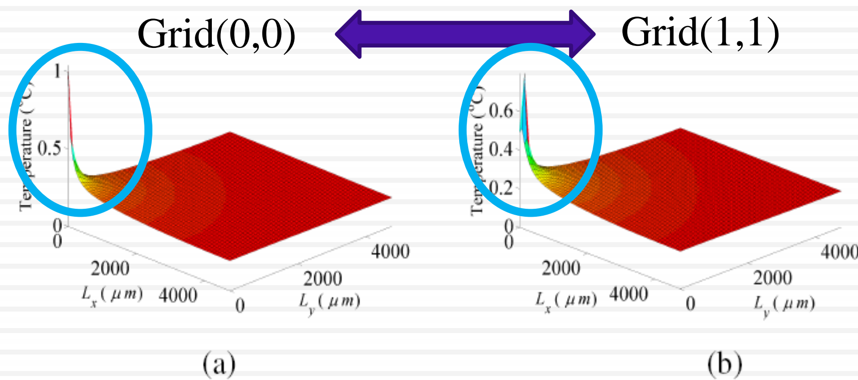
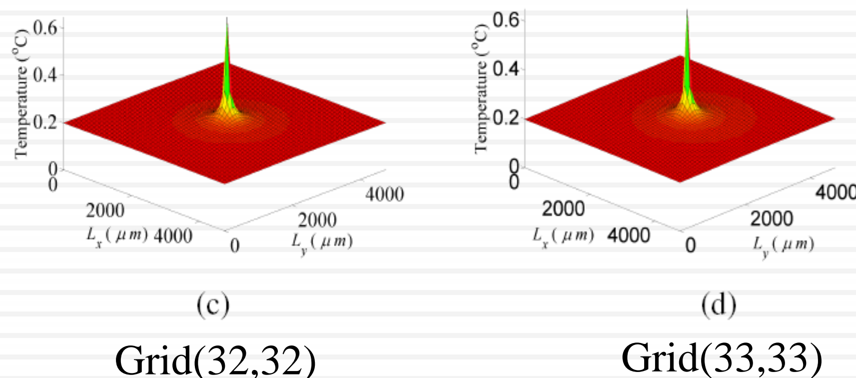
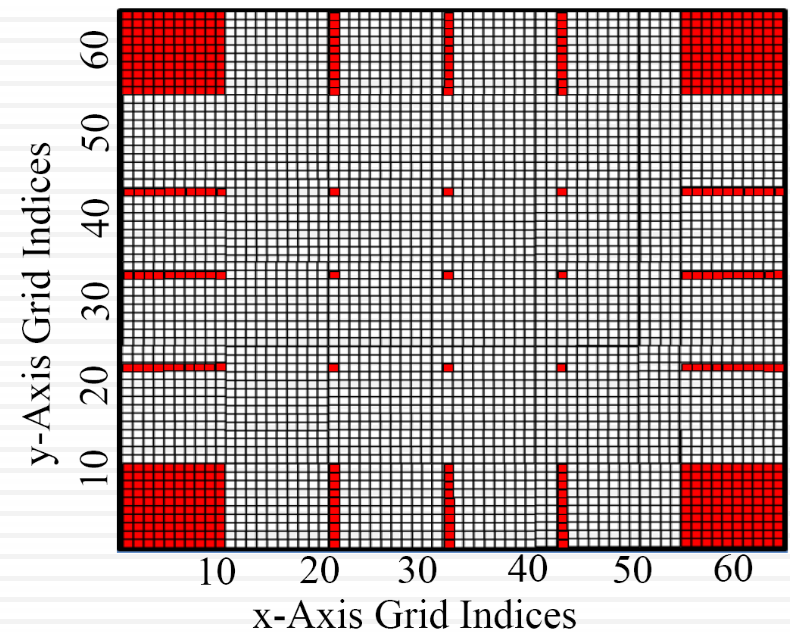
Double-Mesh Table (2/3)

- Use *local similarity* to select the representative grids for constructing fine-mesh tables







Double-Mesh Table (3/3)

- Execute the table shifting and interpolation process for the grids having no pre-built table

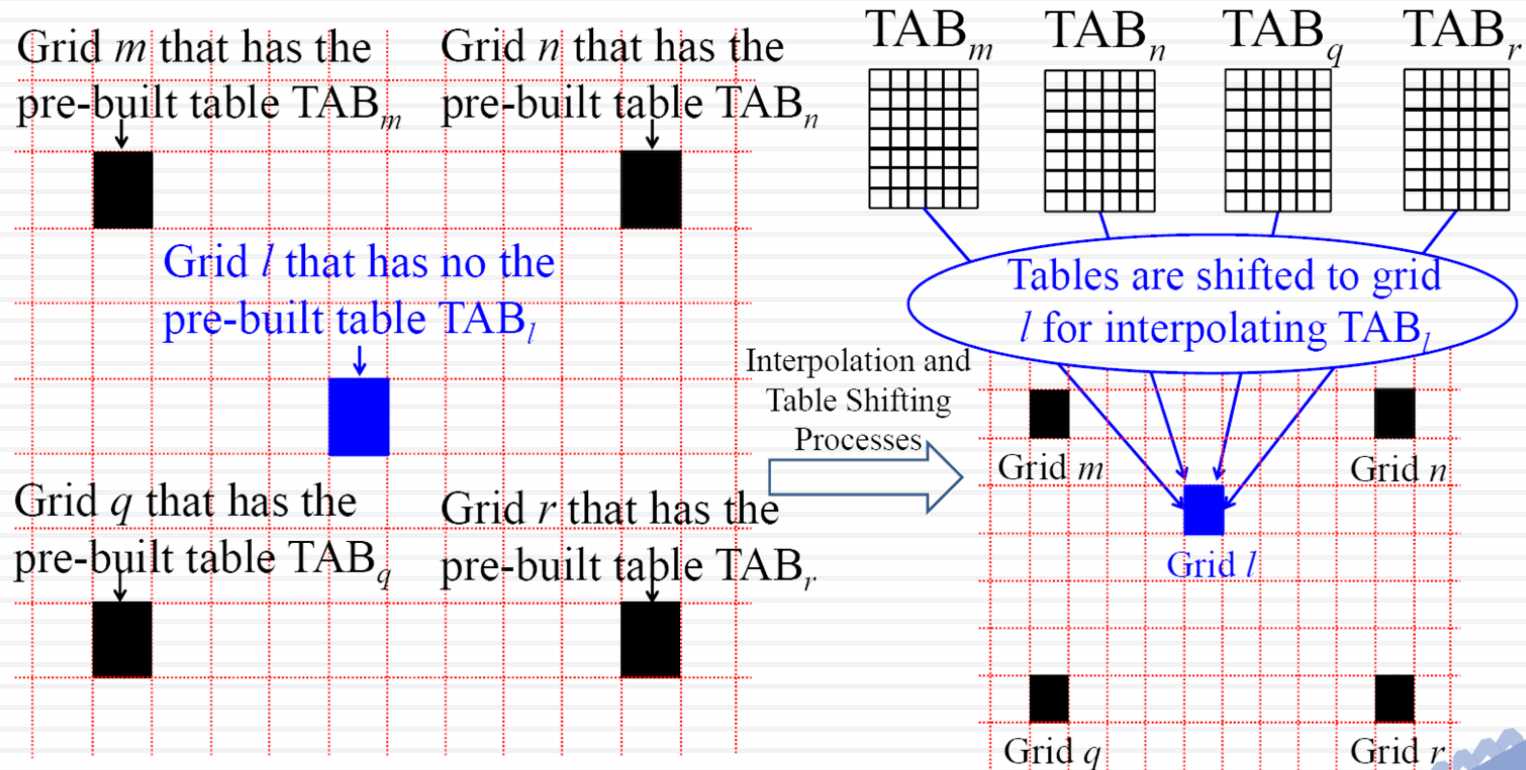
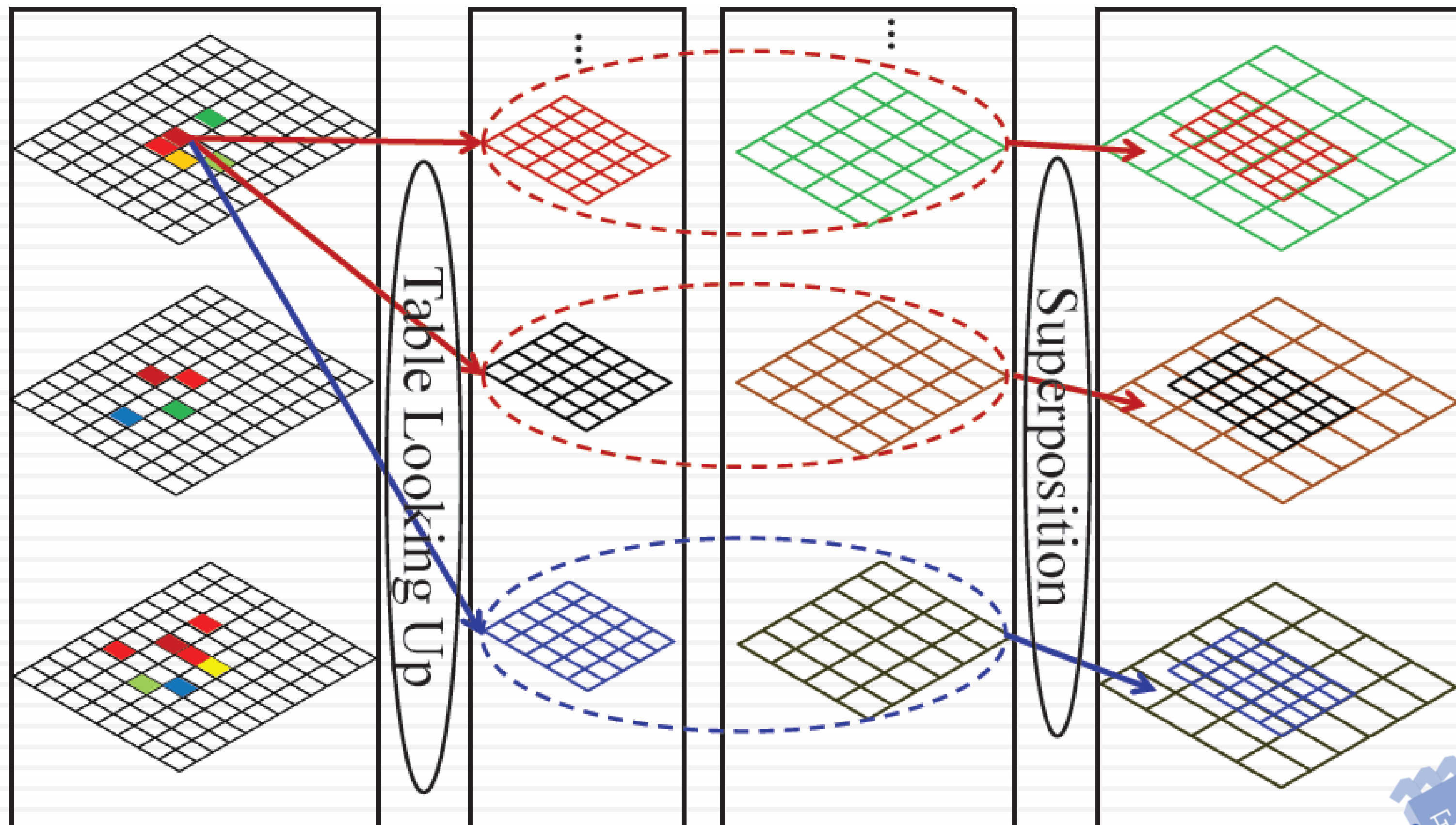


Table Look-Up

- The superposition based table look-up



Complexity Analysis

- The complexity of using double table
  - $O((N_W+N_C+1)N)$ for solving T_h
  - $O((N_W+N_C+1)(N+(q+1)N_{TSV})$ for calculating T^q

    N : Total number of grids

    N_W : Number of fine grids in the window

    N_C : Number of coarse grids

    N_{TSV} : Number of grids has TSVs/TTSVs passing through

  Since N_{TSV} is smaller than N, the complexity for solving T_q is $O((q+2)N)$

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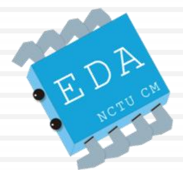
Experimental Results & Summary



Experimental Results (1/3)

- Experimental environment
  - C++ language
  - Intel Core 2 Quad 2.83GHz CPU machine with 8 GB memory
- Parameter setting of tables
  - The mesh size of equivalent circuit (N) : $64\times64\times15$ (10)
  - The window size of fine-mesh tables (N_W) : 10×10
  - The size of coarse-mesh tables (N_C) : 3×3

Experimental Results (2/3)

- Table construction time

Tier Count	Construction Time (s)	
	Fine Mesh	Coarse Mesh
2	21.98	354.43
3	93.66	3213.83

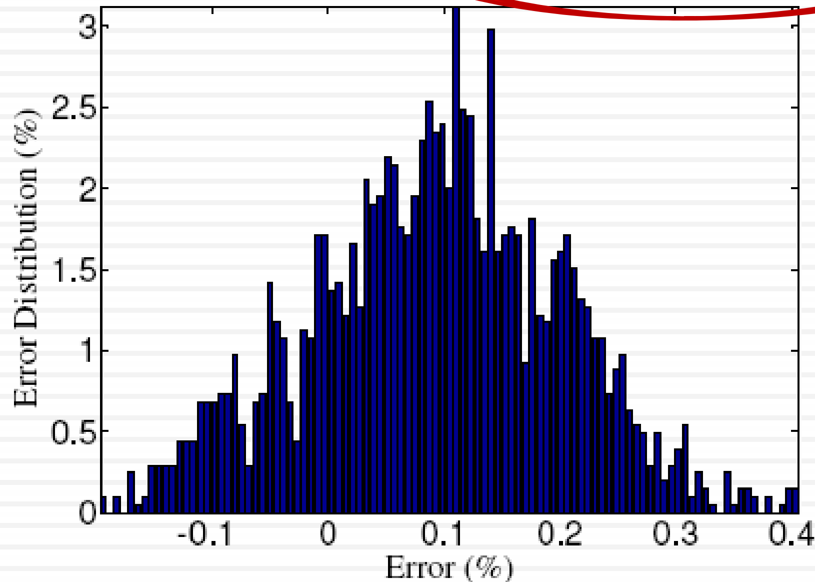
- Test cases
  - The geometry of each tier : 4832μm × 4832μm × 50μm
  - Industrial 90 nm standard cells

Test Chip	Tier Count	Cell Count	TSV Count	Total Power (W)
Case1	2	0.5M	222	1.1
Case2	3	8.3M	3320	5.8
Case3	3	8.4M	4000	6.3
Case4	3	8.2M	4000	6.0

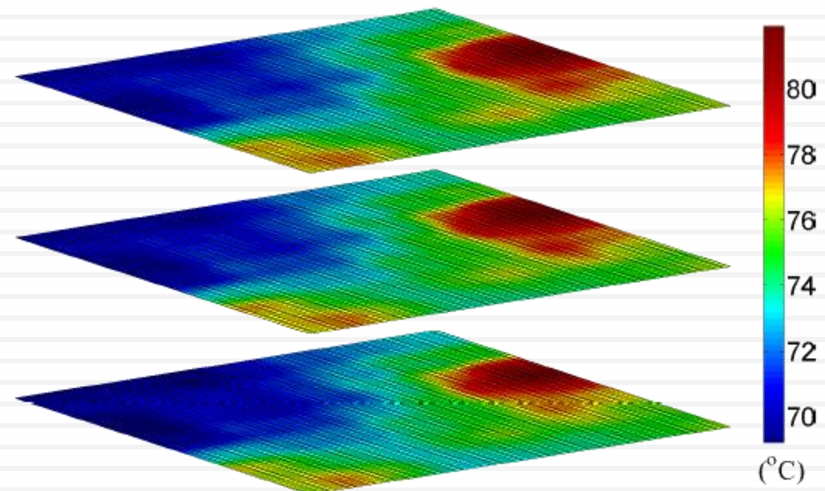
Experimental Results (3/3)

Test Chip	SuperLU Runtime (s)	GMRES			I-LUTSim			
		Runtime (s)	Max Err. (%)	Speedup	Runtime (s)	Trun. Order	Max Err. (%)	Speedup
Case1	3.92	3.92	0.73	1.10	0.002	2	0.69	196.00
Case2	17.68	8.18	0.78	2.16	0.269	3	0.76	65.72
Case3	18.40	6.83	0.81	2.69	0.282	3	0.81	65.48
Case4	17.26	7.49	0.75	2.30	0.416	4	0.75	41.49

18x



Error distribution comparing with Ansys

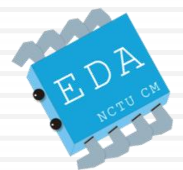


Temperature profile of Case3

Summary

- Conclusion
  - An efficient table look-up based thermal analyzer for 3-D ICs is developed and demonstrated by the experimental results
- Future work
  - To further extend our application scope, we are taking the power consumption and the non-uniform distributed thermal conductivity issue of interconnects into account

Thank you for your attention!



Q & A time