Optimization of Overdrive Signoff

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Outline

- Motivation
- Design Cone
- Dominance of Modes
- Problems and Methodologies
- Experimental Setup and Results
- Conclusions and Ongoing Works

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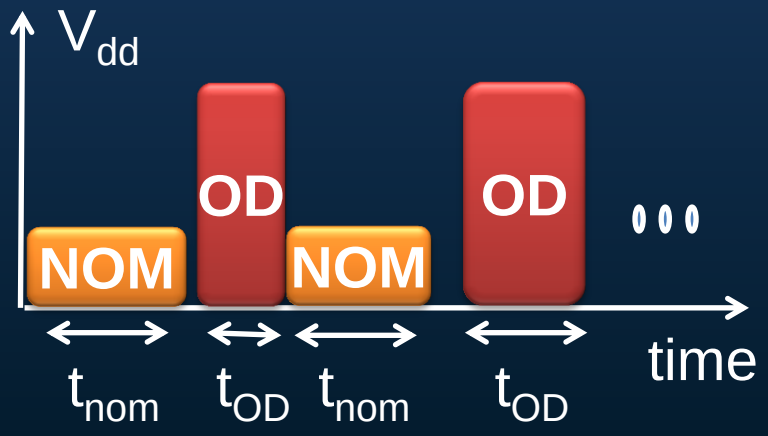
Motivation

- Mode = (voltage, frequency) pair
- Multi-mode operation requires multi-mode signoff
  - Example: nominal mode and overdrive mode
- Selection of signoff modes affects area, power
- Our Goal: Optimally select signoff modes

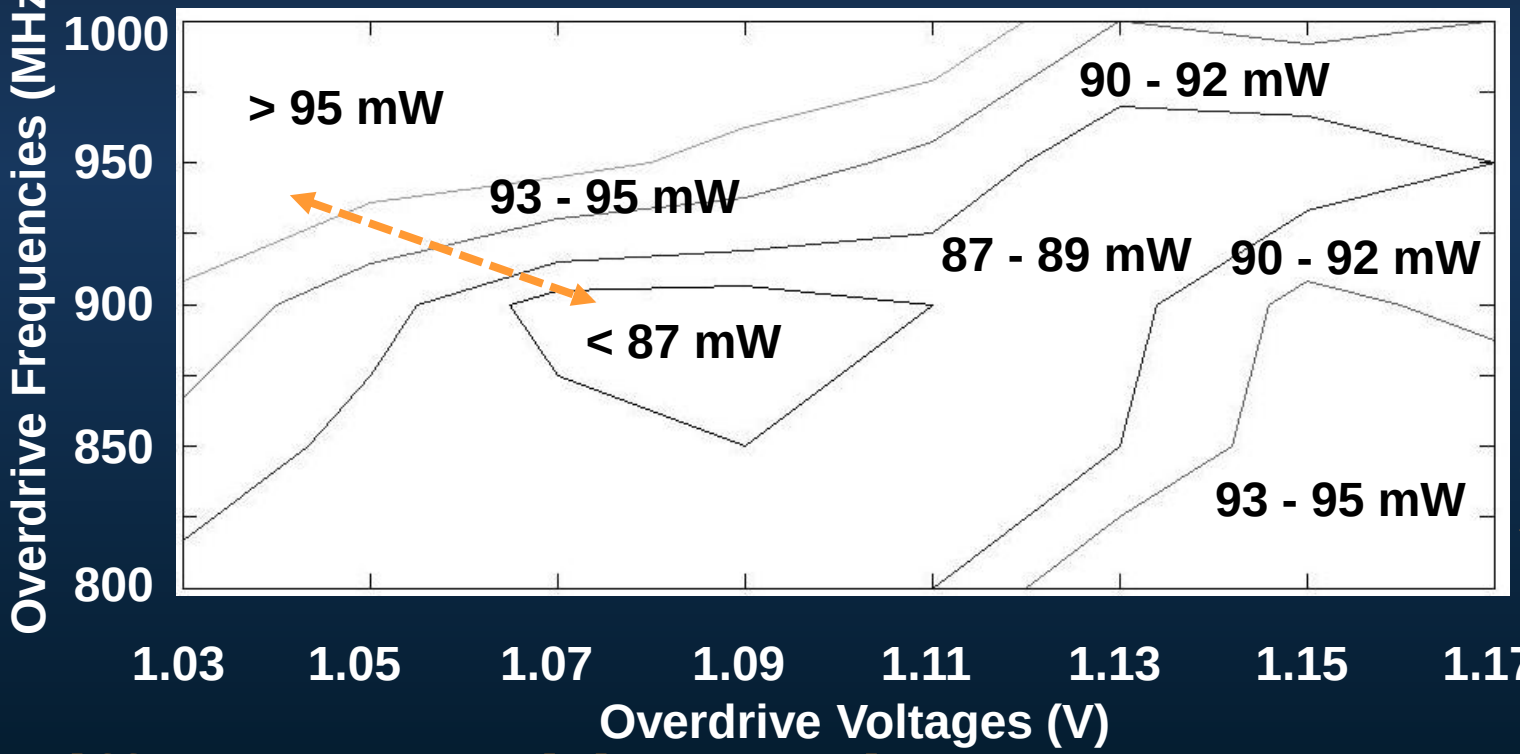
  ⇒ Improve performance, power, or area

  ⇒ Reduce overdesign



Fix Nominal Mode

- The average power of circuits signed off with different overdrive modes
- Average power = r x P_{OD} + (1-r) x P_{nom}
  - r is the duty cycle of overdrive mode

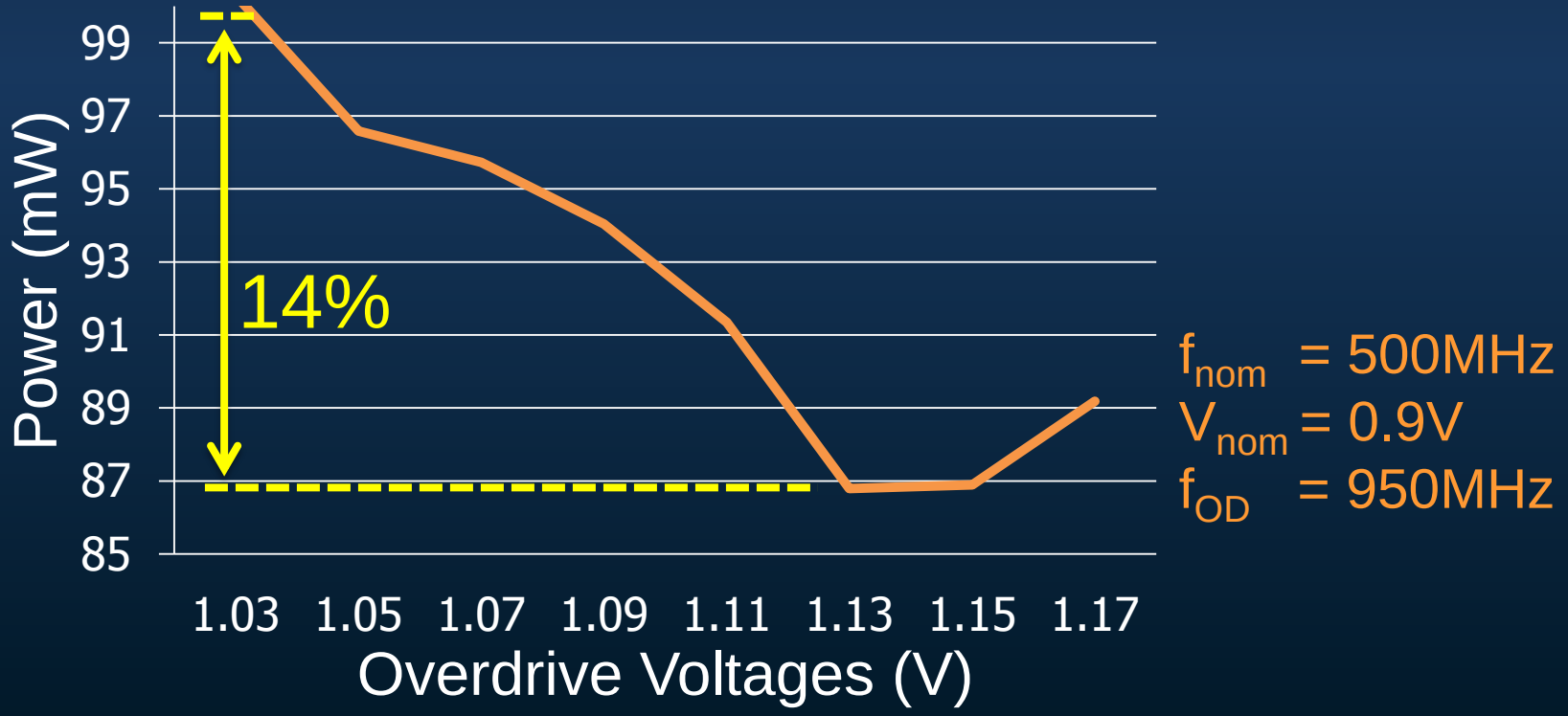


f_{nom} = 500MHz
V_{nom}= 0.9V

Different overdrive modes ⇒ 20% power range

Fix Nominal Mode + OD Frequency

- Power of circuits signed off with different overdrive voltages
- Low signoff voltage ⇒ large # of buffers
- High signoff voltage ⇒ high dynamic power



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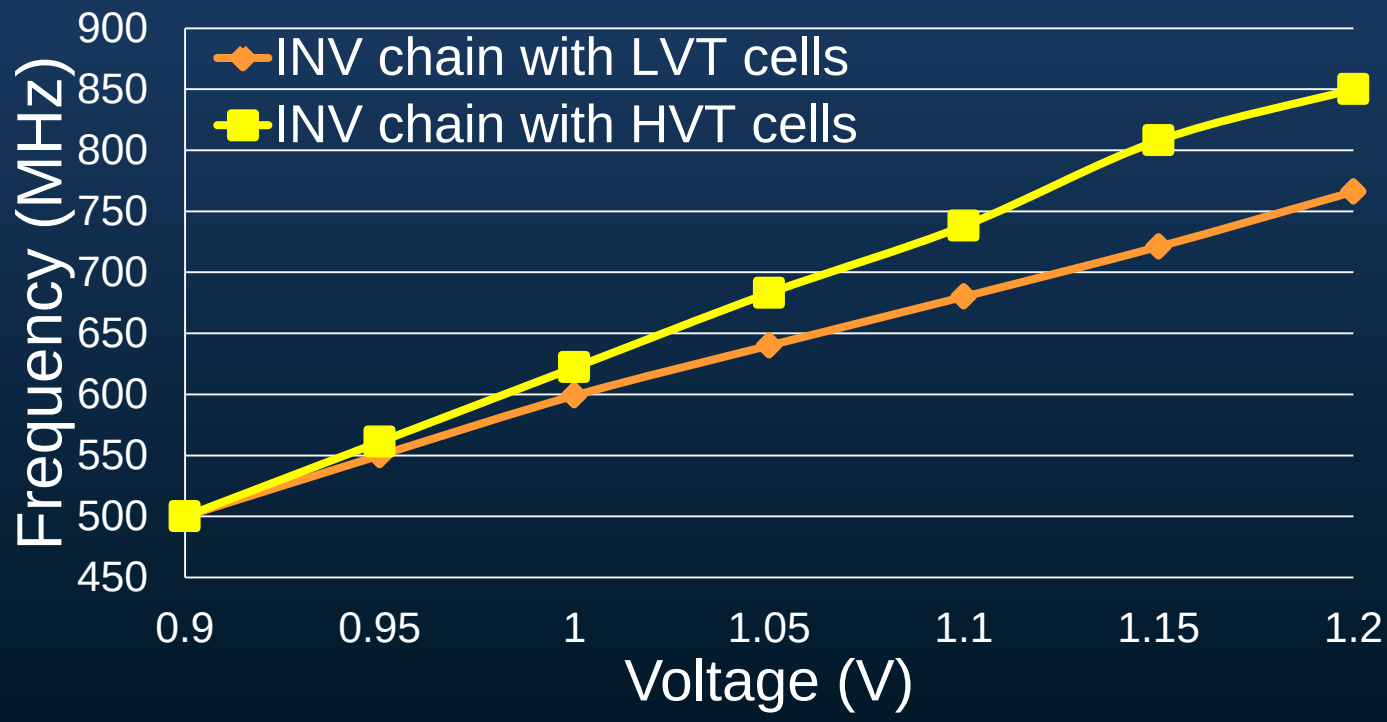
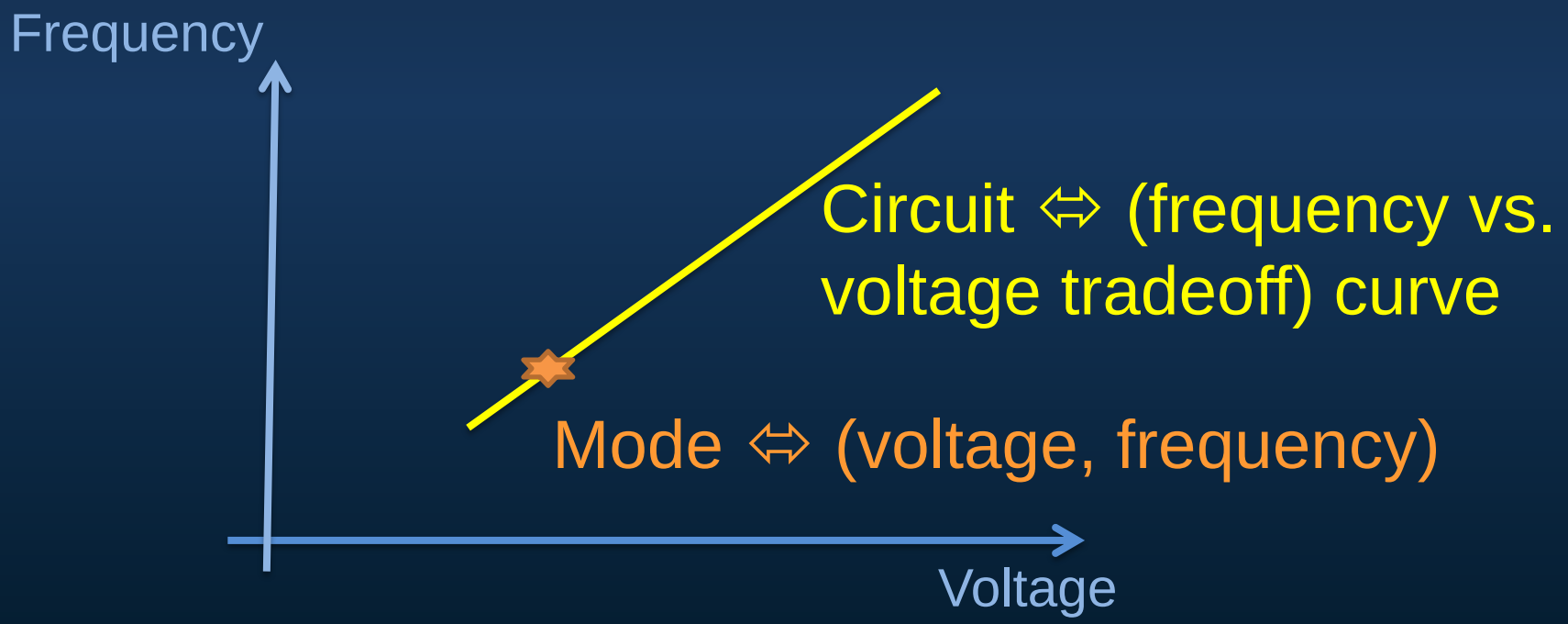
Tradeoff between Frequency & Voltage

- Voltage scaling ⇒ frequency vs. voltage tradeoff curves
- Maximum frequency increases essentially linearly with supply voltage
- We approximate such curves as straight lines



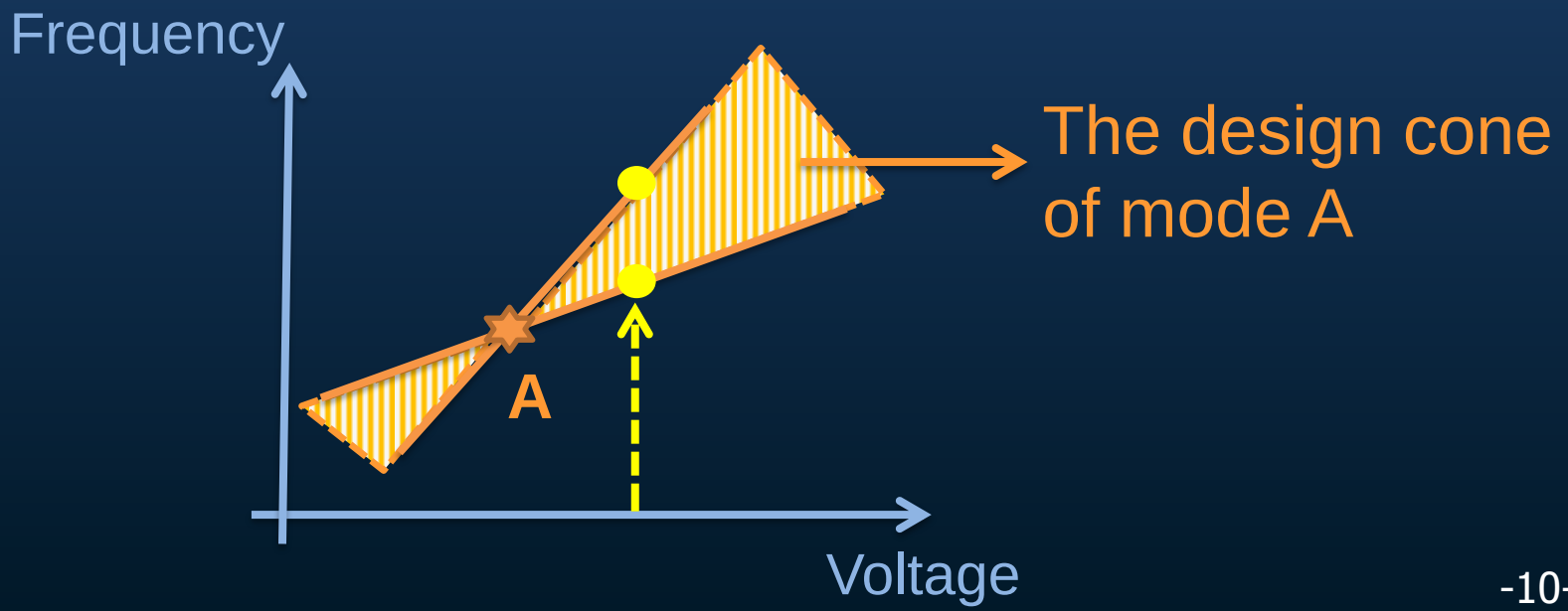
Design Space for Signoff

- Design space for signoff is the set of all possible combinations of signoff modes
- Example: design space for two-mode signoff is all combinations of two points in the plane



Design Cone

- Design cone is the union of all the feasible operating modes (frequency, voltage pairs) for circuits signed off at one mode
- Determined by tradeoff between frequency and voltage (slopes of frequency vs. voltage tradeoffs)
- Indicates the solution space for signoff mode selection



Estimation of Design Cone

- Slope of frequency vs. voltage tradeoff (MHz/V) mainly determined by threshold voltages
- Gate type, fanout have little influence

V_T	Fanout	Gate Types		
		INV	NAND	NOR
LVT	4	887	800	936
LVT	16	776	787	877
HVT	4	1167	1176	1260
HVT	16	1126	1217	1246

- Wire resistance also has little influence
  - 10,000X change in resistance $\Rightarrow$ <2% change in slopes

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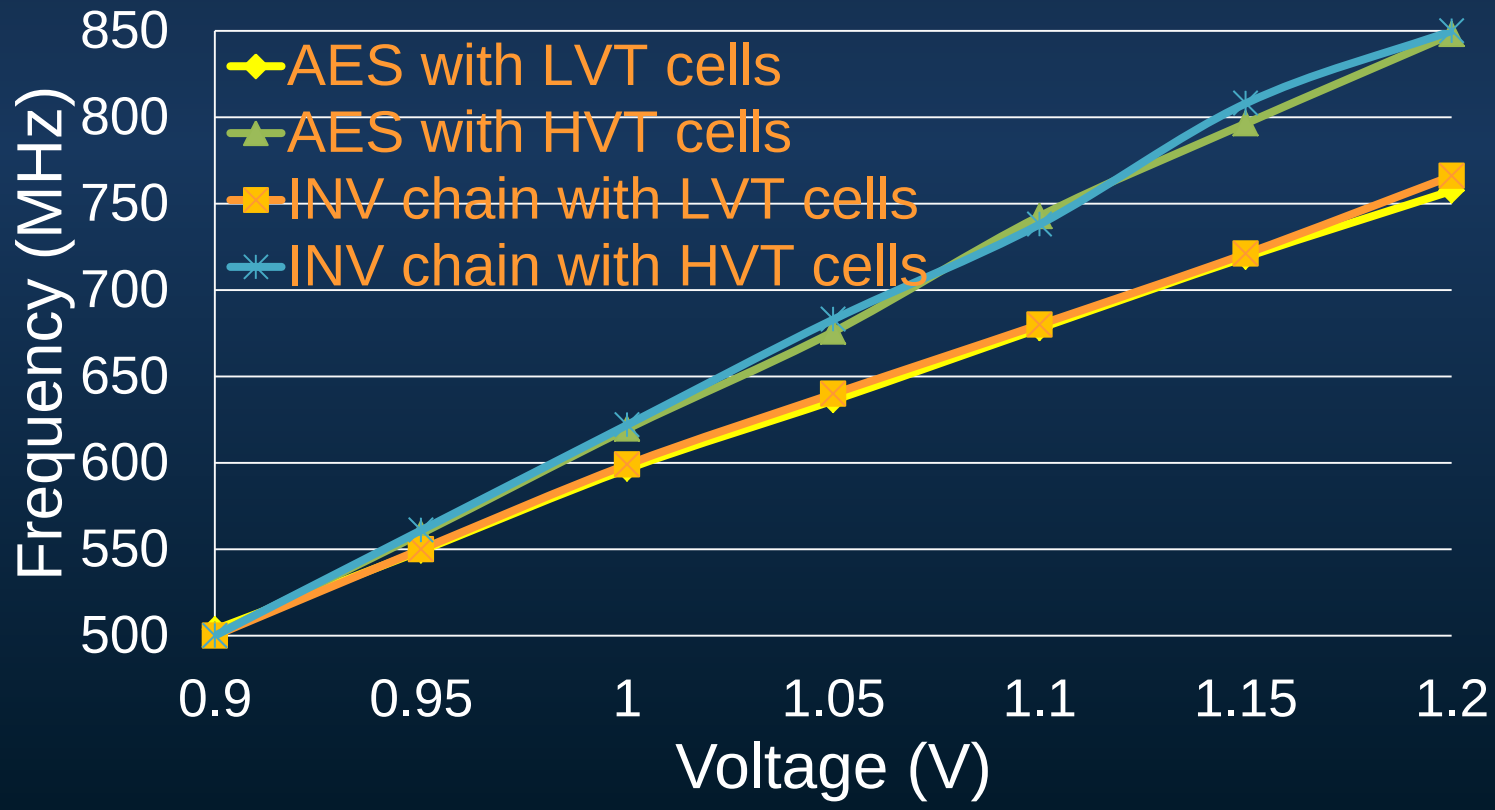
Estimation of Design Cone

- Slope of frequency vs. voltage tradeoff (MHz/V) mainly determined by threshold voltages

We use inverter chains with LVT- and HVT-only cells to estimate the boundary of design cone



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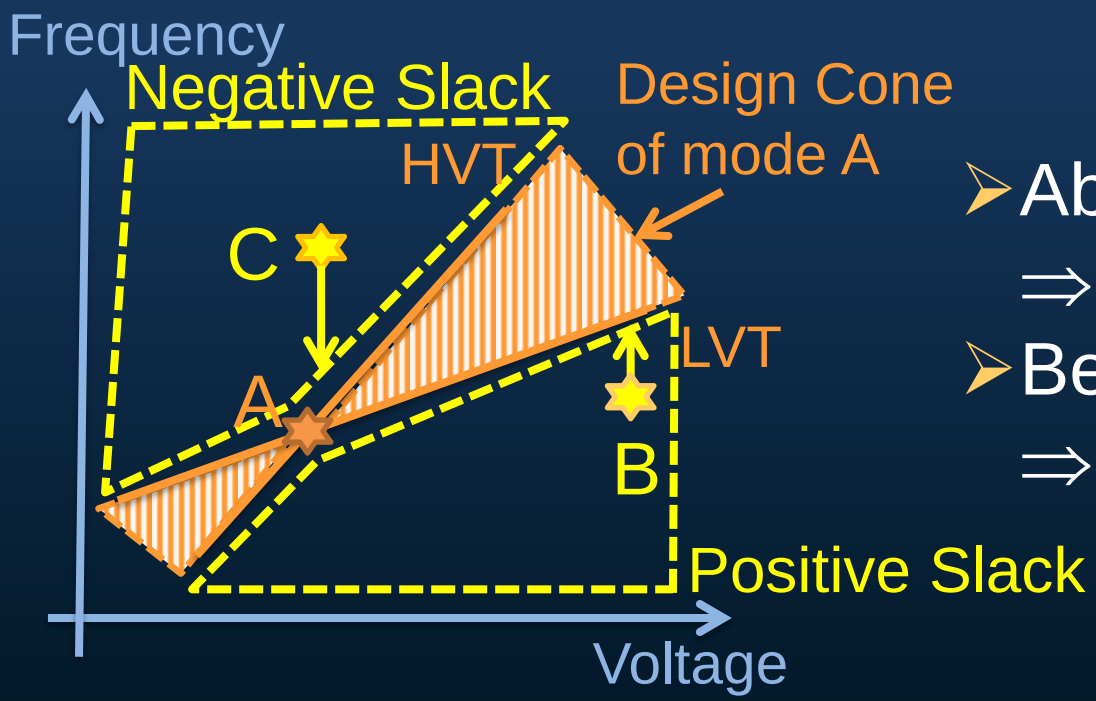
Dominance

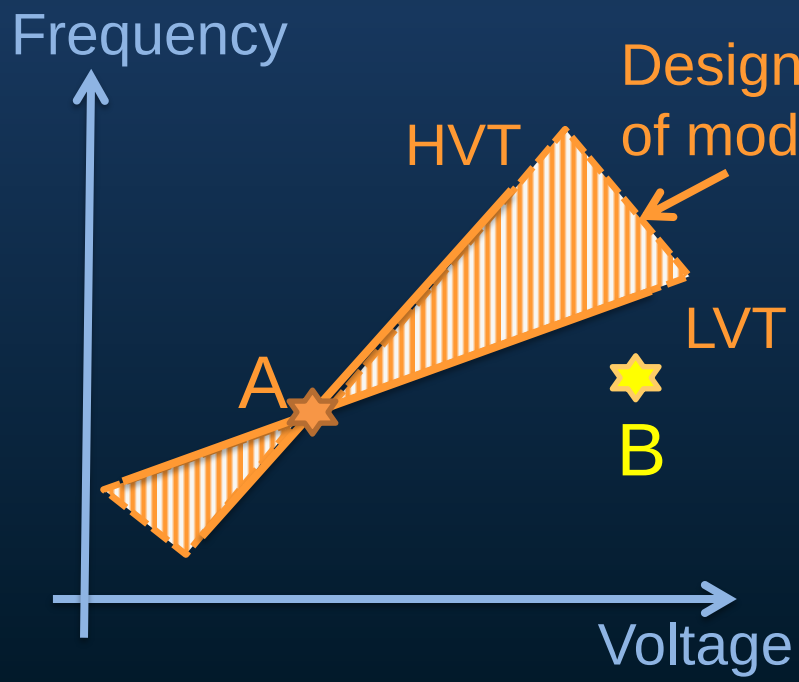
- One mode is outside of the design cone of the other ⇒ positive / negative timing slacks



- Above the design cone ⇒ Negative timing slacks
- Below the design cone ⇒ Positive timing slacks

Dominance

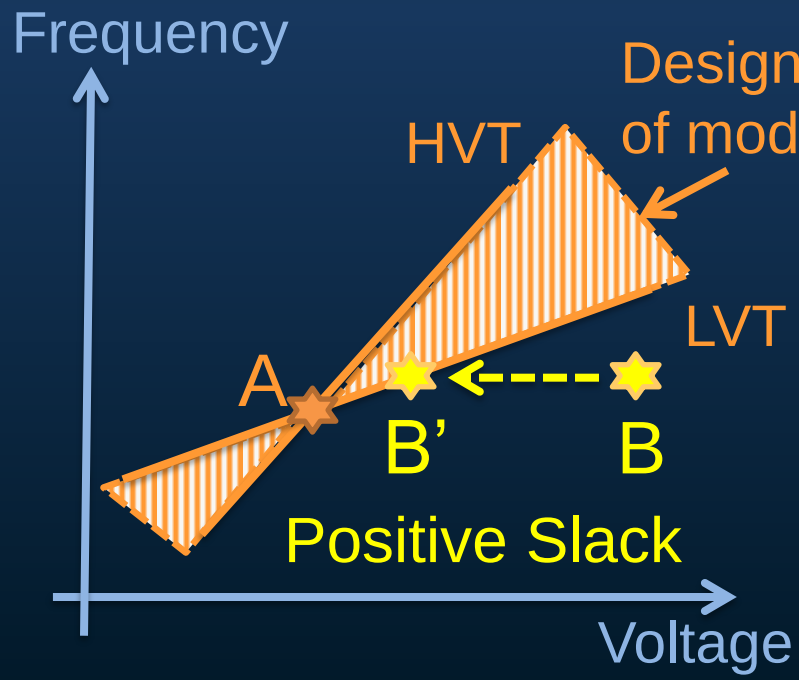
- One mode is outside of the design cone of the other ⇒ positive / negative timing slacks
- M_2 shows positive timing slacks w.r.t. M_1 ⇒ M_1 is the dominant mode



➢ Mode A is the dominant mode

Dominance

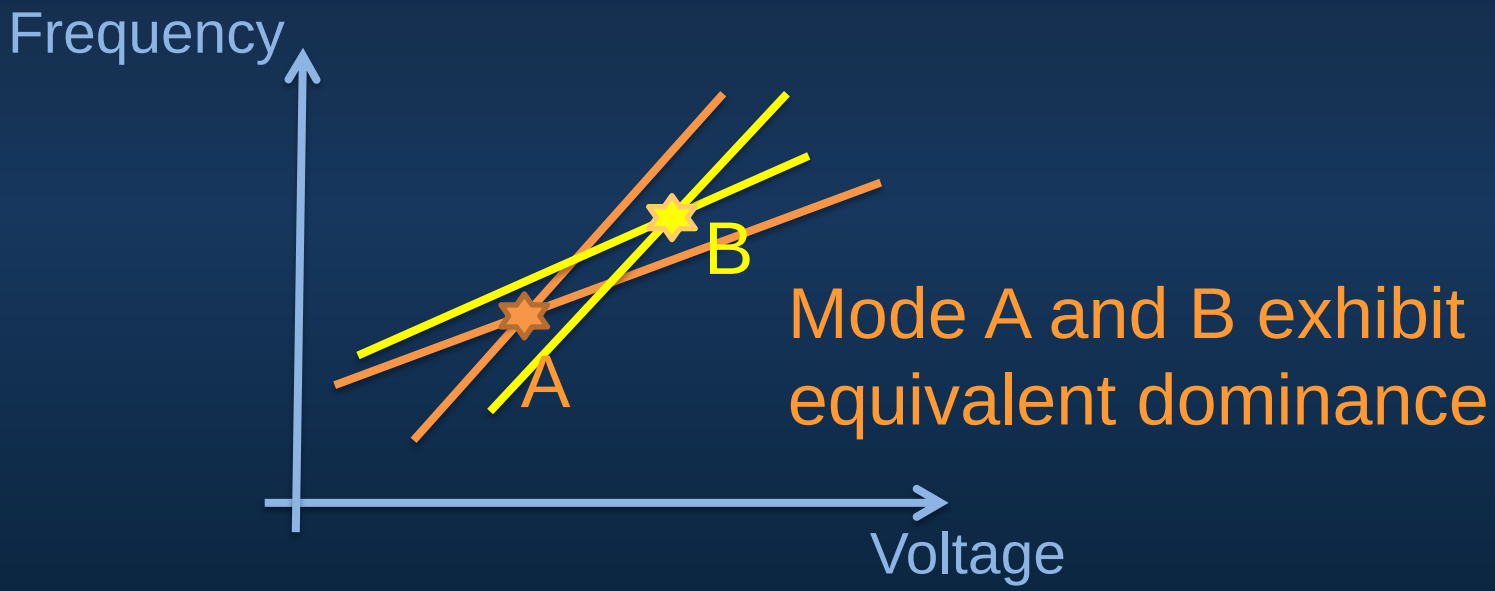
- One mode is outside of the design cone of the other ⇒ positive / negative timing slacks
- M_2 shows positive timing slacks w.r.t. M_1 ⇒ M_1 is the dominant mode
- Positive timing slacks indicate overdesign



- ➢ Mode A is the dominant mode
- ➢ Shift mode B to B'
  - ⇒ reduce voltage and power
  - ⇒ retain same performance

Equivalent Dominance

- When two modes exhibit equivalent dominance
  - No one is dominated by the other
  - They are in each other's design cone



Multi-mode signoff at modes which do not exhibit equivalent dominance leads to overdesign

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The 3+1 Problems

- Overdrive signoff has four parameters
  - Nominal mode: f_{nom}, V_{nom}
  - Overdrive mode: f_{OD}, V_{OD}

- Given f_{nom}, f_{OD} and V_{nom}, search for V_{OD}
- Given f_{nom}, f_{OD} and V_{OD}, search for V_{nom}

  $\Rightarrow$ Minimize power

- Given V_{nom}, V_{OD} and f_{nom}, search for f_{OD}
- Given V_{nom}, V_{OD} and f_{OD}, search for f_{nom}

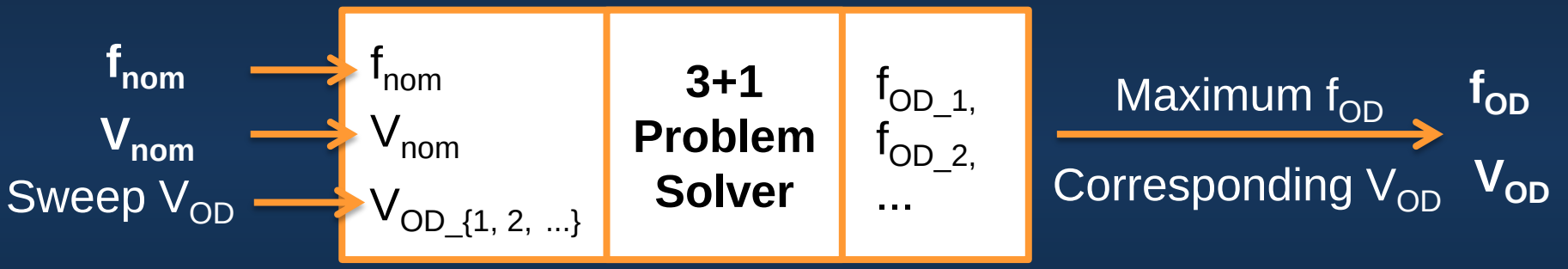
  $\Rightarrow$ Maximize performance under power constraints

The 2+2 Problems

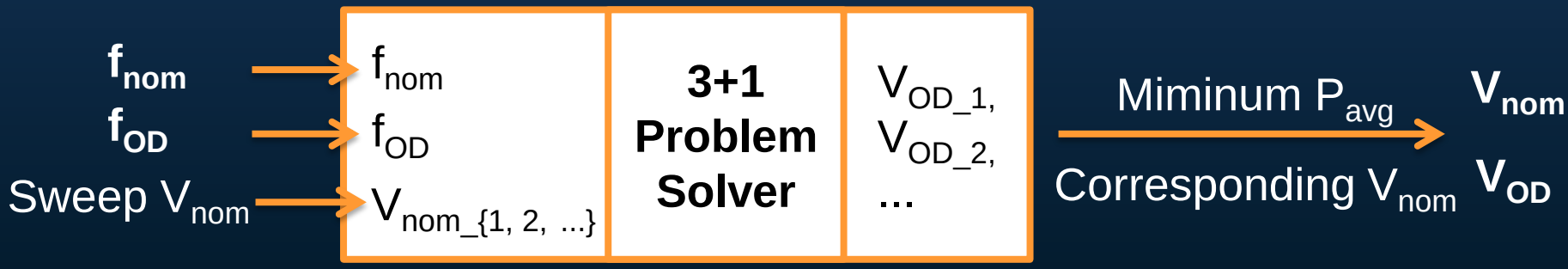
- Overdrive signoff needs four parameters
  - Nominal mode: f_{nom}, V_{nom}
  - Overdrive mode: f_{OD}, V_{OD}
- FIND_OD: given (f_{nom}, V_{nom}), search for (f_{OD}, V_{OD})
  $\Rightarrow$ maximize f_{OD}
  s.t. average and peak power satisfy constraints
- FIND_VOLT: given f_{nom} and f_{OD}, search for V_{nom} and V_{OD}
  $\Rightarrow$ minimize average power

Reduction from 2+2 to 3+1

- 2+2 problems can reduce to 3+1 problems by sweeping one unknown parameter
- Reduction of FIND_OD problem



- Reduction of FIND_VOLT problem

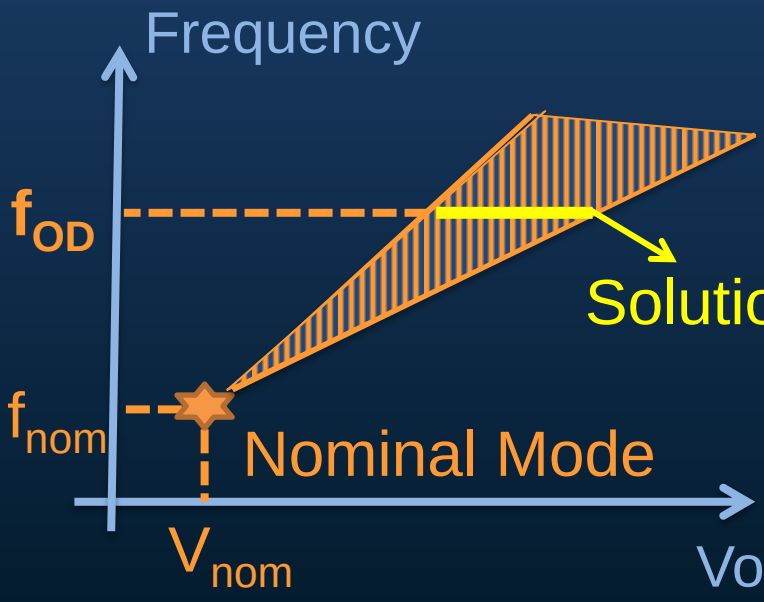


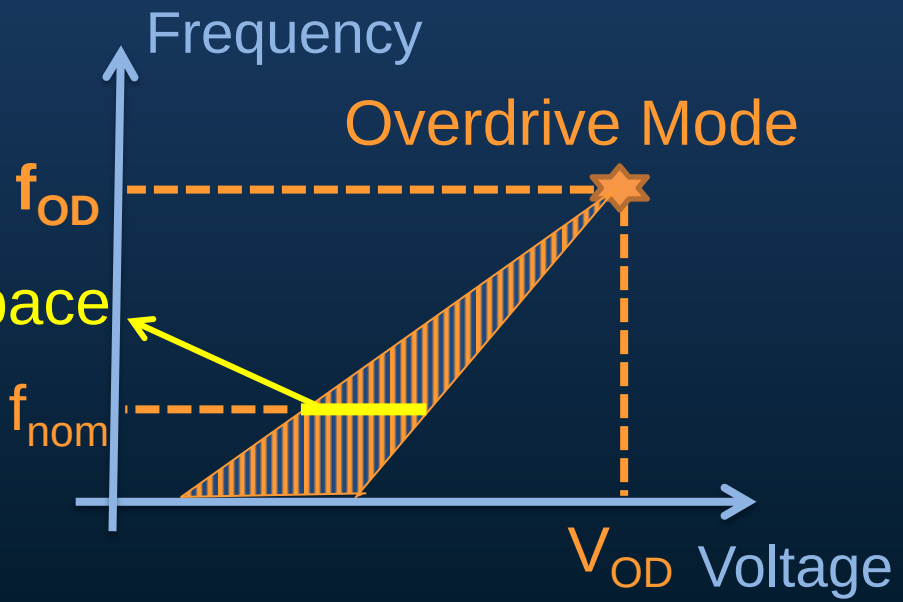
Methodologies for 3+1 Problems

- Given f_{nom}, f_{OD} and V_{nom}, search for V_{OD}
- Given f_{nom}, f_{OD} and V_{OD}, search for V_{nom}

  $\Rightarrow$ Minimize power

Exhaustive search on the solution space defined by given parameters and design cone



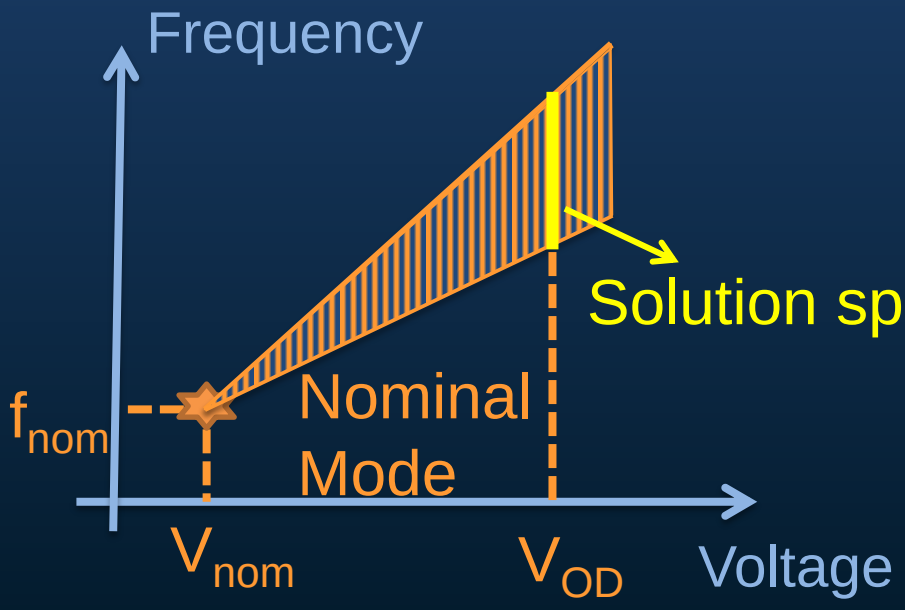


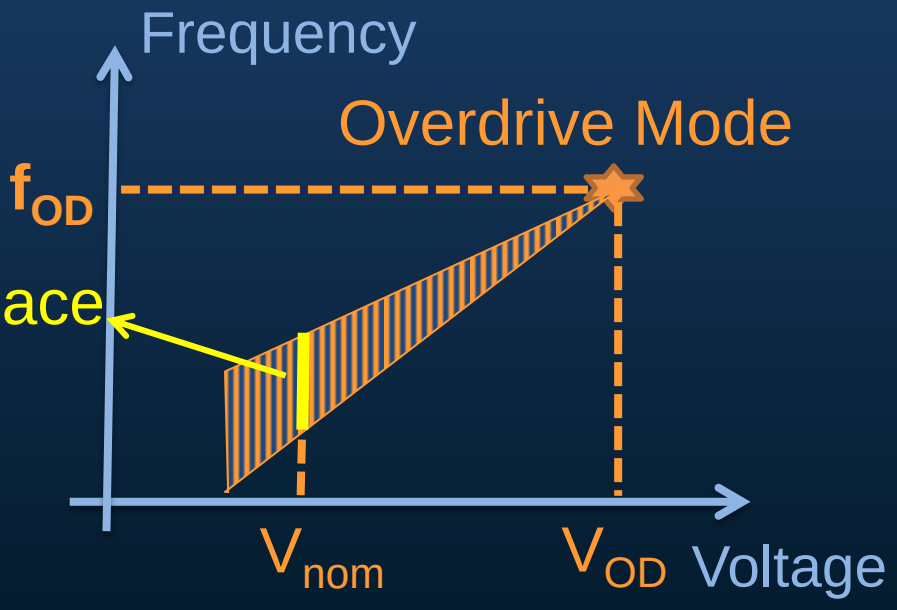
Methodologies for 3+1 Problems

- Given V_{nom}, V_{OD} and f_{nom}, search for f_{OD}
- Given V_{nom}, V_{OD} and f_{OD}, search for f_{nom}

  $\Rightarrow$ Maximize performance under power constraints

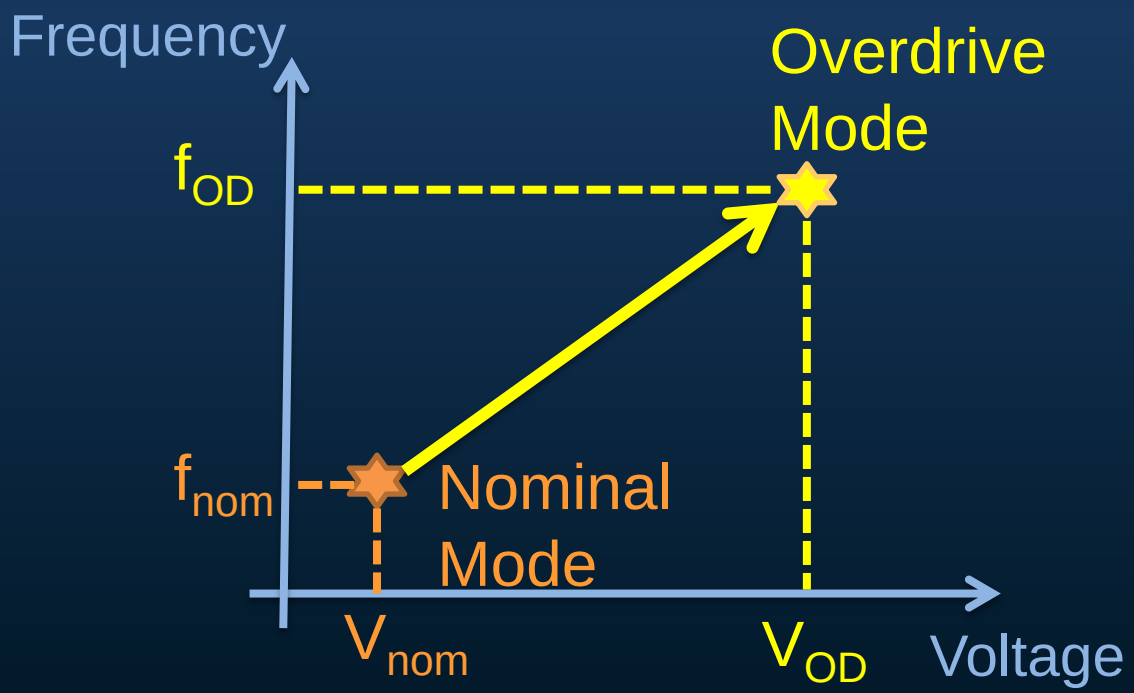
Scale frequency along the solution space until the power constraint is hit





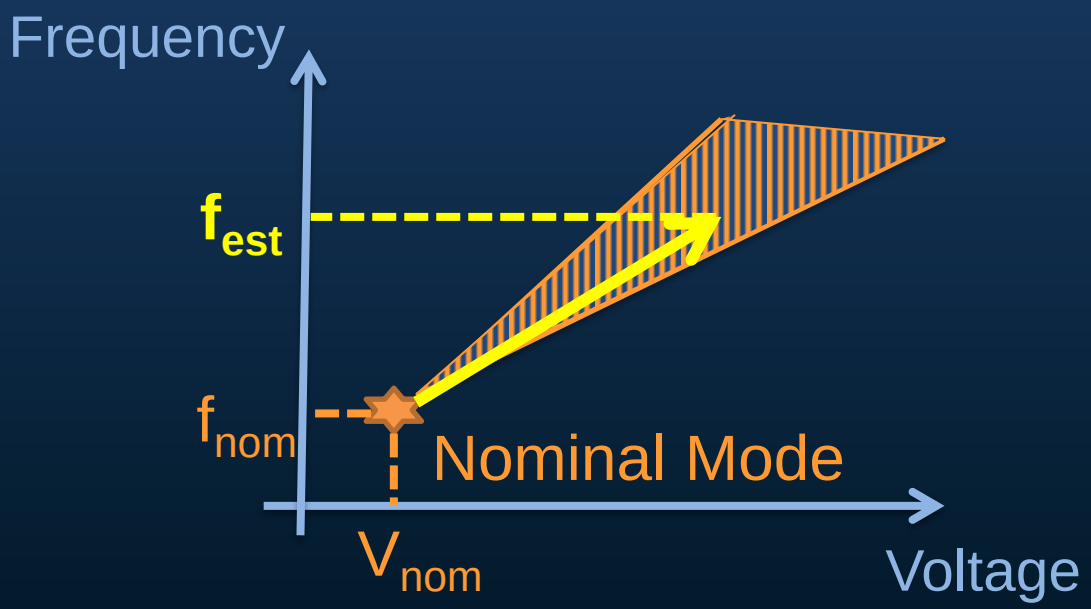
Common Design Practice Today: Signoff & Scale (FIND_OD)

- Sign off circuit at nominal mode
- Scale the voltage to increase frequency until the power constraint is hit
- Simplifies the design process, but ignores second (OD) mode in the signoff



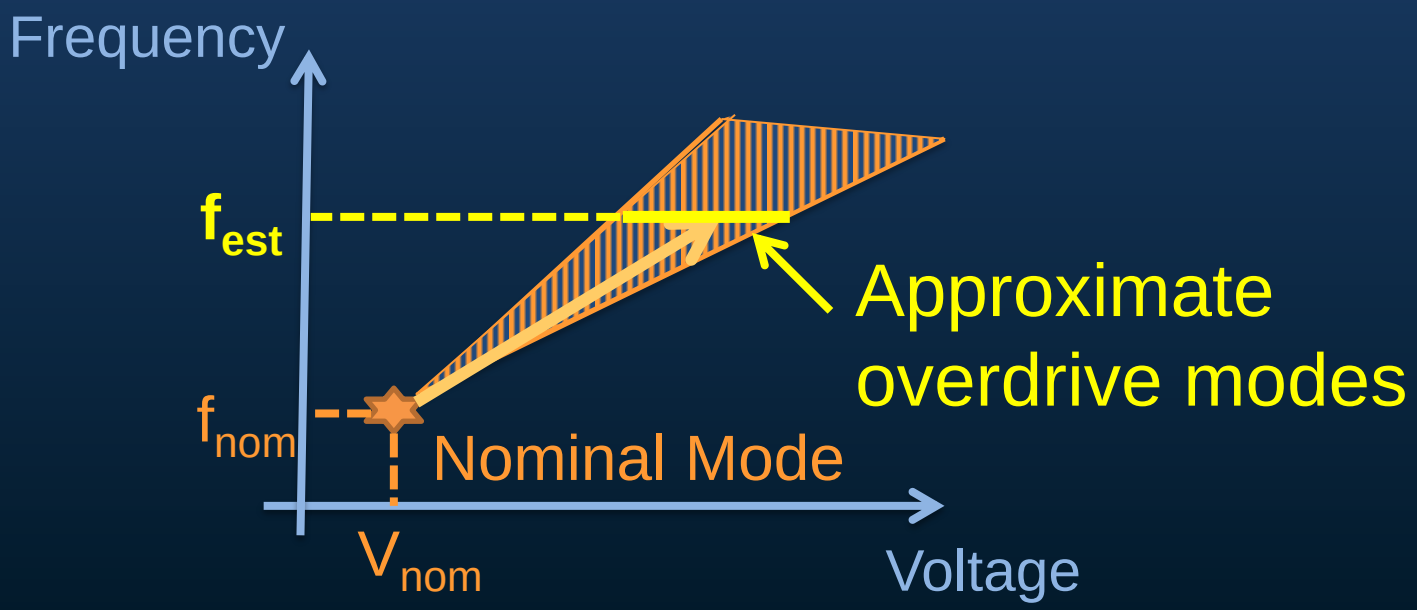
Proposed Flow (FIND_OD)

- Signoff & scale at nominal mode to estimate the maximum overdrive frequency (f_{est})



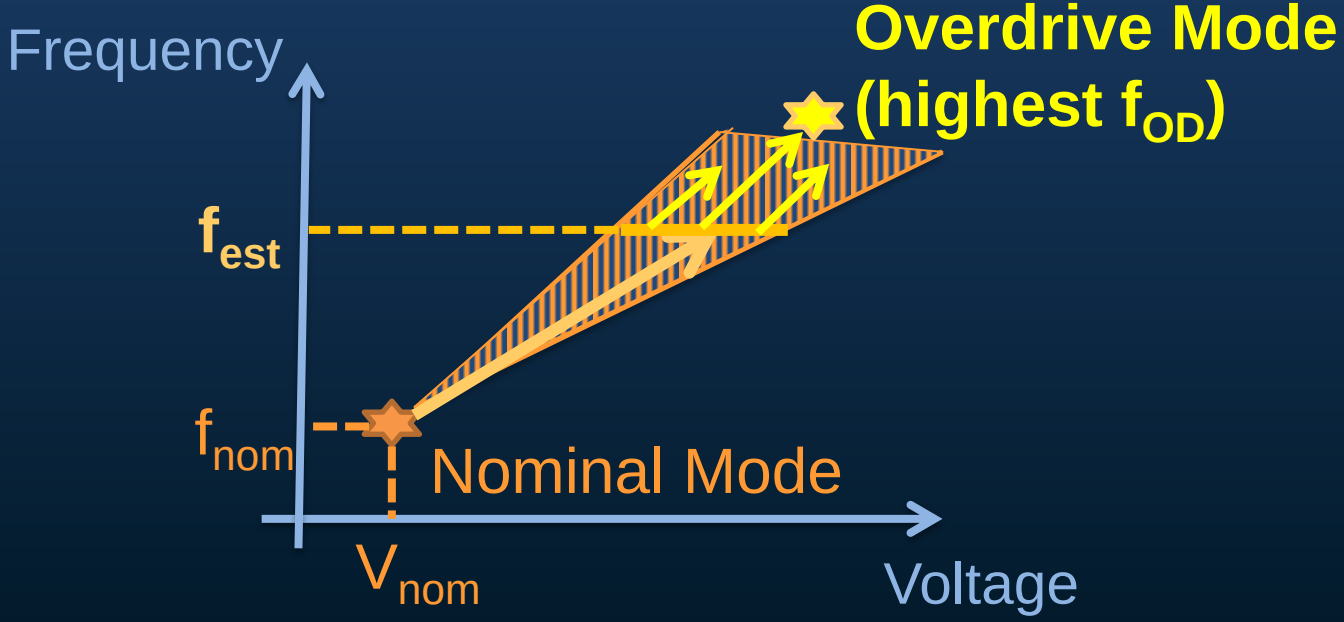
Proposed Flow (FIND_OD)

- Signoff & scale at nominal mode to estimate the maximum overdrive frequency (f_{est})
- Determine several approximate overdrive modes based on f_{est} and the design cone



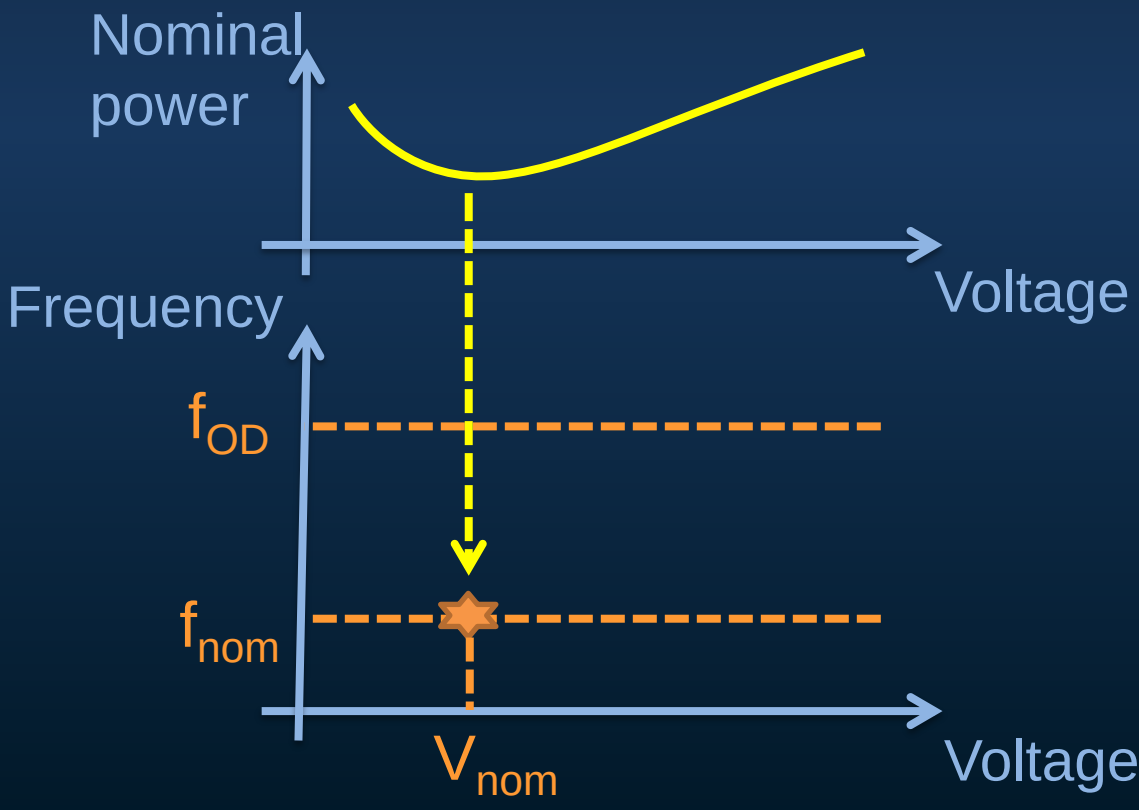
Proposed Flow (FIND_OD)

- Signoff & scale at nominal mode to estimate the maximum overdrive frequency (f_{est})
- Determine several approximate overdrive modes based on f_{est} and the design cone
- Implement voltage scaling on each approximate overdrive mode until hit the power constraint



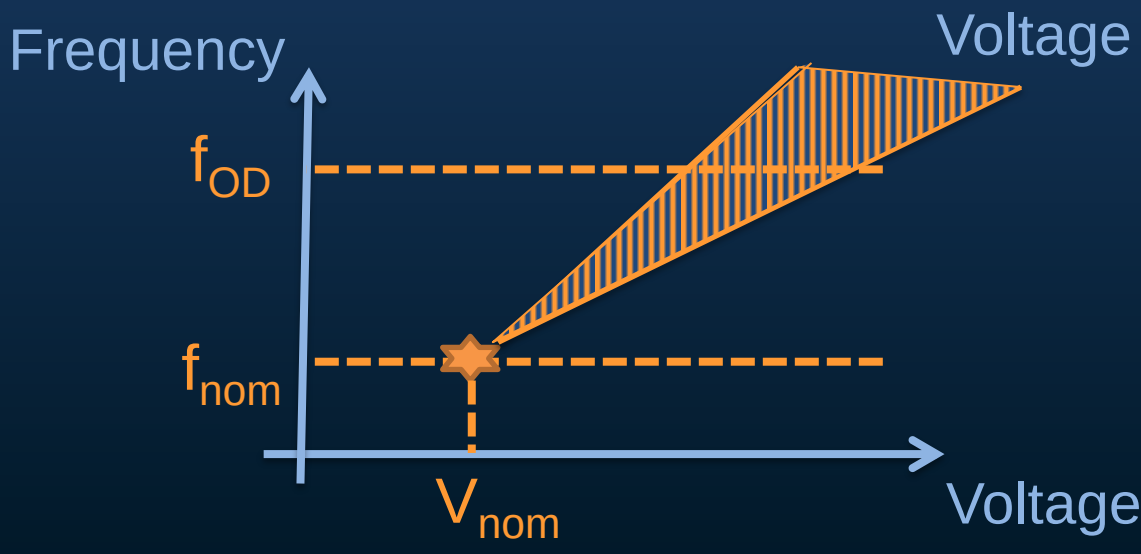
Proposed Flow (FIND_VOLT)

- Exhaustive search for V_{nom} ⇒ minimum power at nominal mode



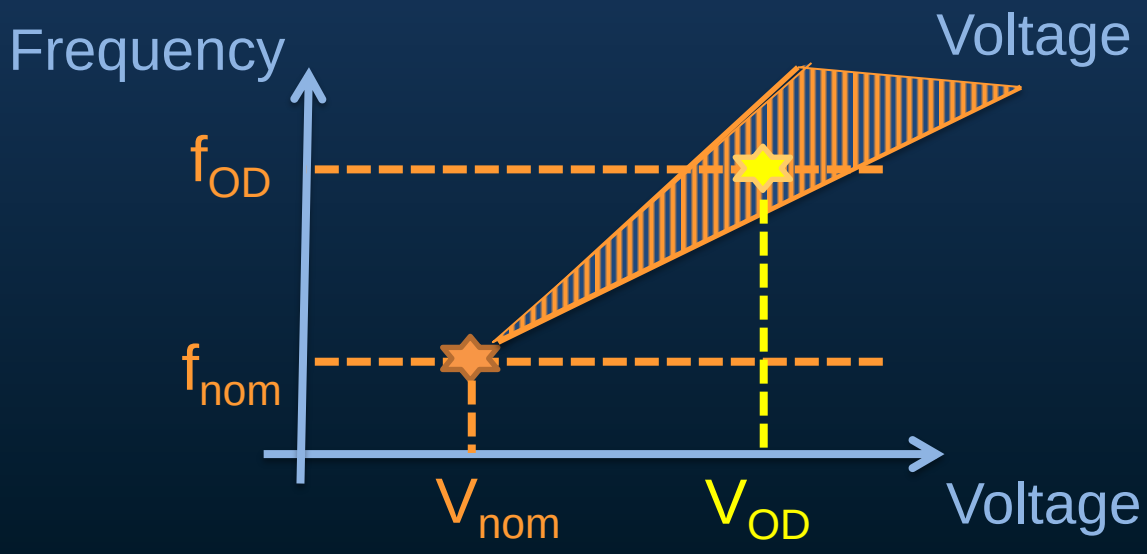
Proposed Flow (FIND_VOLT)

- Exhaustive search for V_{nom} $\Rightarrow$ minimum power at nominal mode
- Estimate the design cone of selected mode



Proposed Flow (FIND_VOLT)

- Exhaustive search for V_{nom} $\Rightarrow$ minimum power at nominal mode
- Estimate the design cone of selected mode
- Exhaustive search for V_{OD} within the design cone $\Rightarrow$ minimum average power



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Experimental Setup

- Design: AES (~15K instances) from *OpenCores*
- Technology: TSMC 65nm
- Comparison
  - Signoff&Scale applies traditional signoff and scale methodology
  - Proposed implements our proposed flow
  - Exhaustive Search uses exhaustive search

Experimental Results (FIND_OD)

- Proposed flow improves performance by 7%
- Flow requires about 22% runtime compared to exhaustive search with similar area (-0.01%), power (+3%) and performance (-0.5%)

	Signoff & Scale	Proposed Flow	Exhaustive Search
f_{OD} (MHz)	711	764	768
V_{OD} (V)	1.14	1.14	1.15
Area (μm^2)	31029	32016	32020
P_{OD} (mW)	49.13	49.14	49.76
P_{avg} (mW)	21.73	20.90	20.24
# P&R runs	1	7	32

Nominal mode: f_{nom} = 500MHz V_{nom} = 0.9V

Experimental Results (FIND_VOLT)

- Flow requires about 27% runtime compared to exhaustive search with similar area (-0.01%), power (+8%)

	Proposed Flow	Exhaustive Search
V_{nom} (V)	0.92	0.91
V_{OD} (V)	1.02	1.01
Area (μm^2)	30948	30960
P_{OD} (mW)	41.08	30.38
P_{avg} (mW)	22.28	20.61
# P&R runs	9	33

f_{nom} = 500MHz / f_{OD} = 600MHz

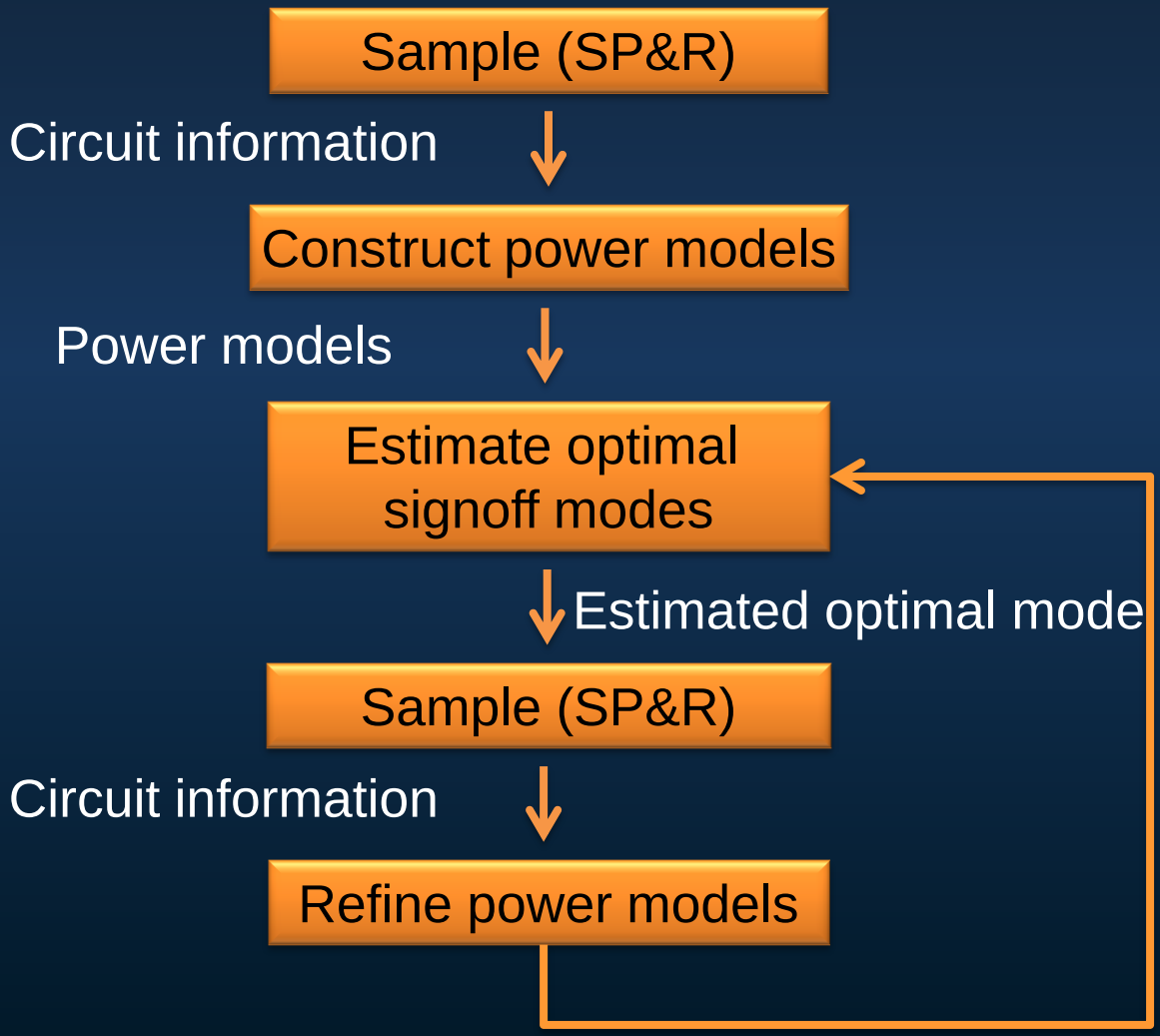
Signoff & Scale is not applicable to FIND_VOLT

Recent Updates

- Problem: too many SP&R runs
- Approach:
  - Use power models for global optimization
  - Avoid implementing circuits at each mode
- Construct power model adaptively
- Small constant # runs is enough $\Rightarrow$ scalable

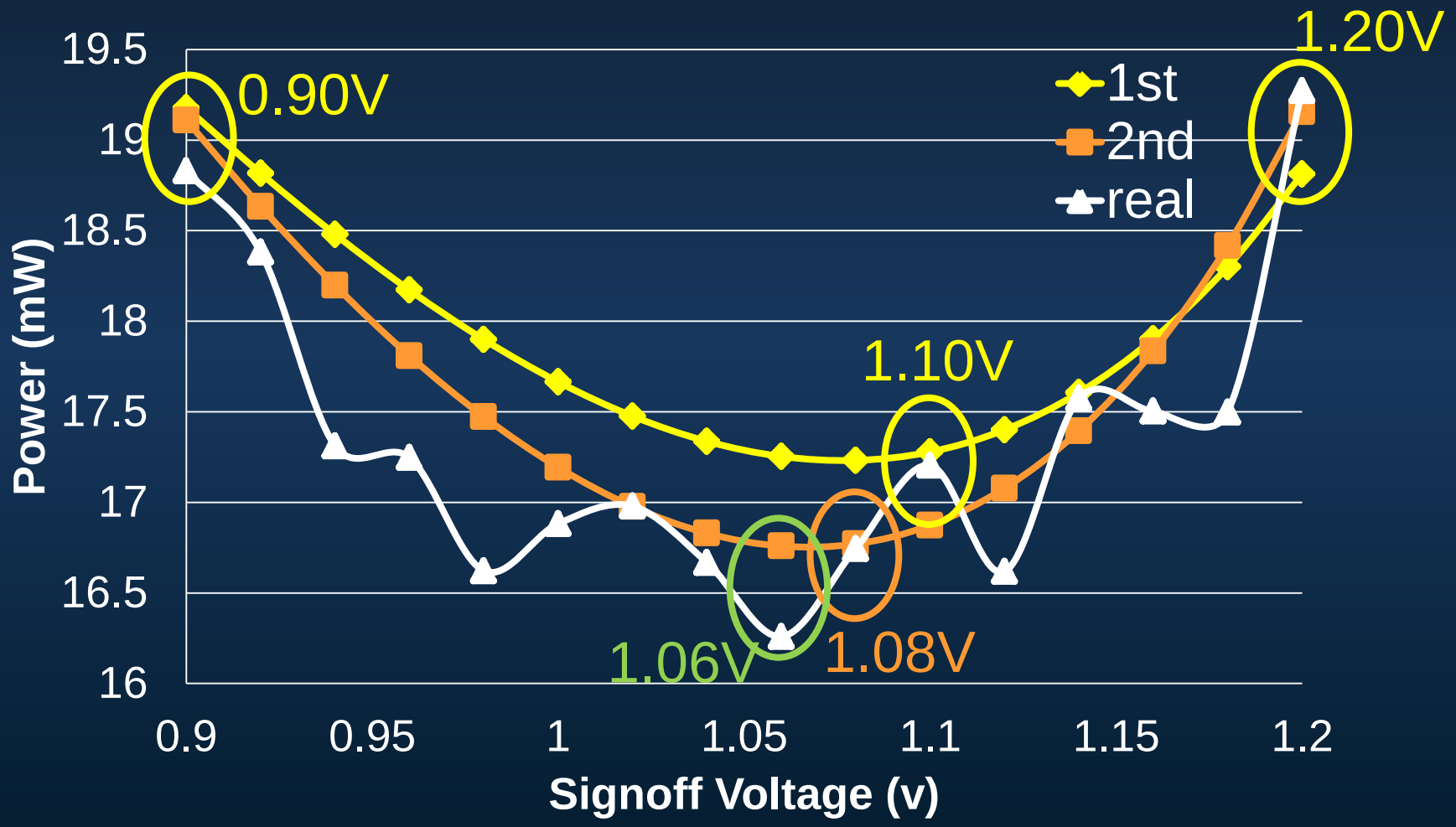
Global Optimization Flow

- Iteratively sample and refine the power models



Example

- Performance of the proposed global optimization



Frequency = 800MHz , Voltage = ?

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Conclusions & Ongoing Works

- Conclusions
  - Study the problem of signoff mode selection
  - Propose the concept of design cone
  - Show that mutual equivalent dominance is required for signoff mode selection to avoid overdesign
  - Propose methodologies for signoff mode selection
- Ongoing Works
  - More accurate estimation of design cone
  - Consider additional tradeoffs of design metrics such as area, reliability

Acknowledgments

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Thank You!