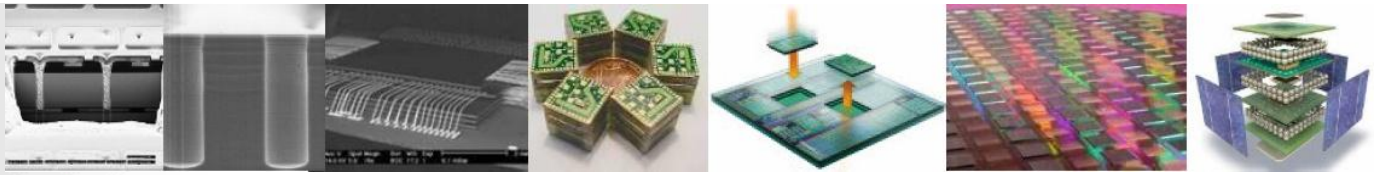
Session 4C

Power Optimization for Application-Specific 3D Network-on-Chip with Multiple Supply Voltages



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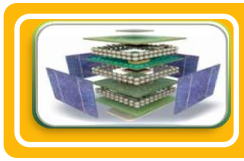
Outline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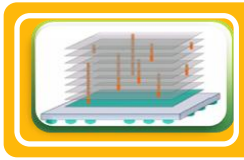
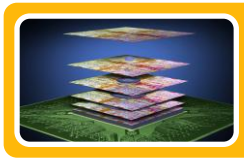
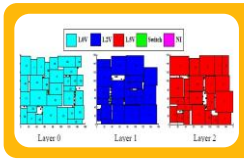

MSV-driven Layer Assignment


3D NoC Synthesis


Experimental Results


Conclusion

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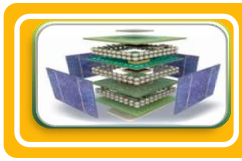
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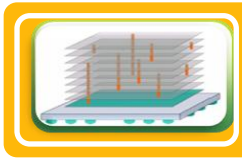
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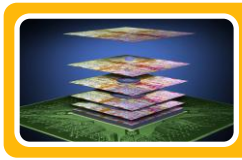
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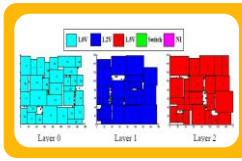
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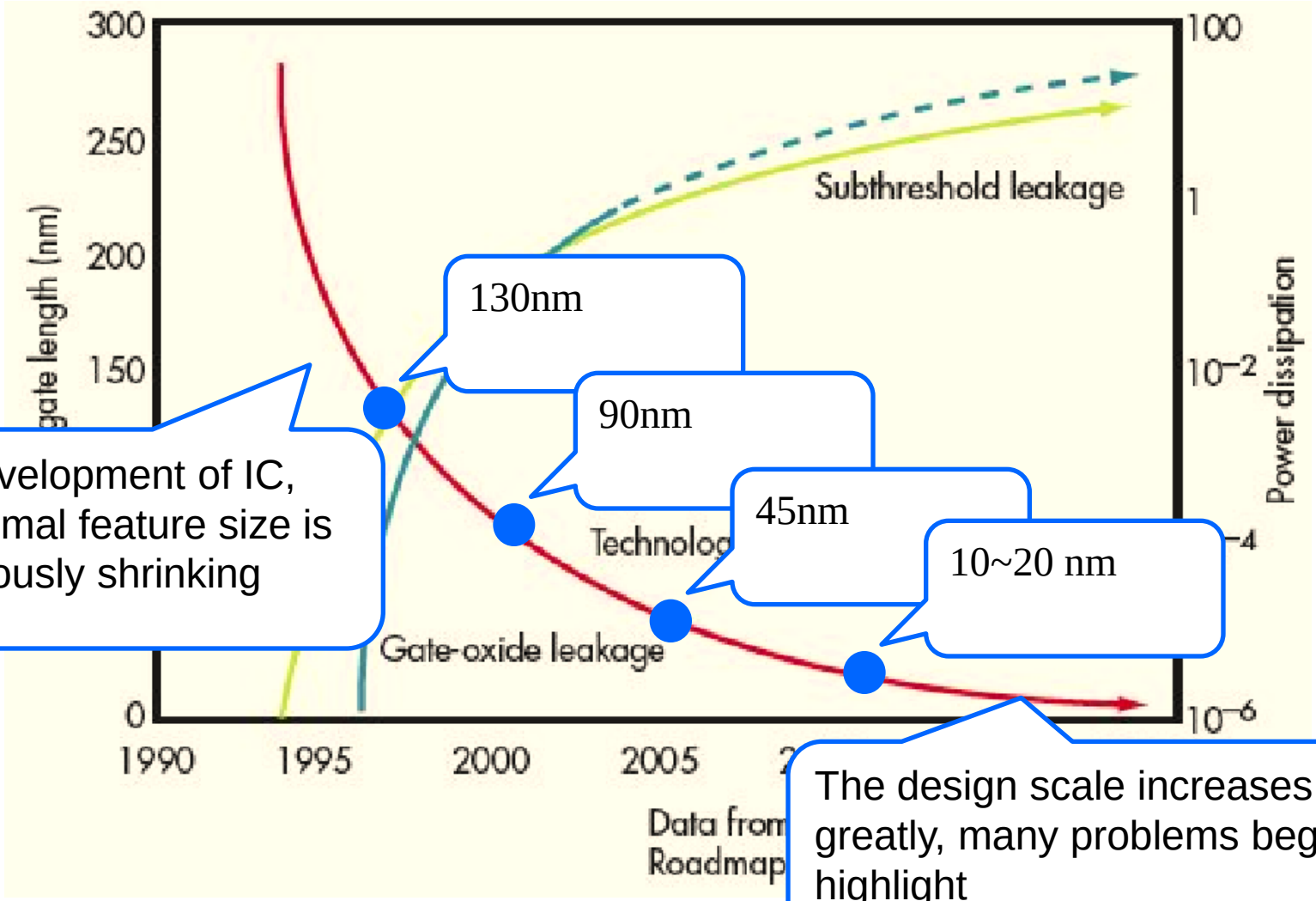
Challenge in Moore's law

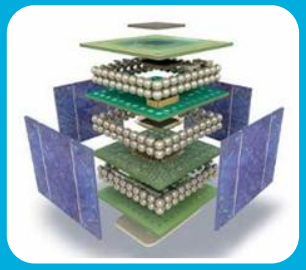


With development of IC, the minimal feature size is continuously shrinking

The design scale increases greatly, many problems begin to highlight

Challenge in Moore’s law

Moore's law is facing huge challenges

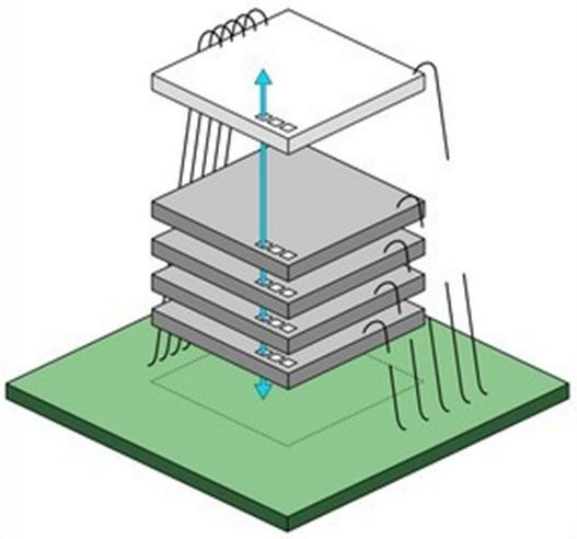


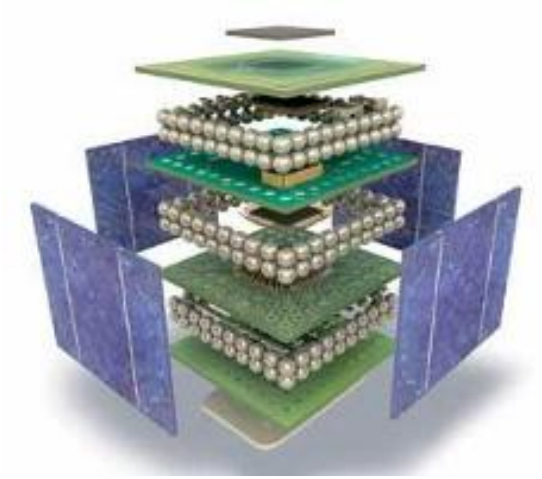
Power Consumption

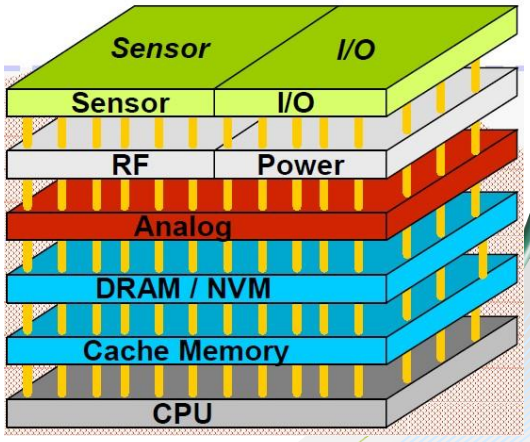
- Waste power
- Thermal problem

3D Integration

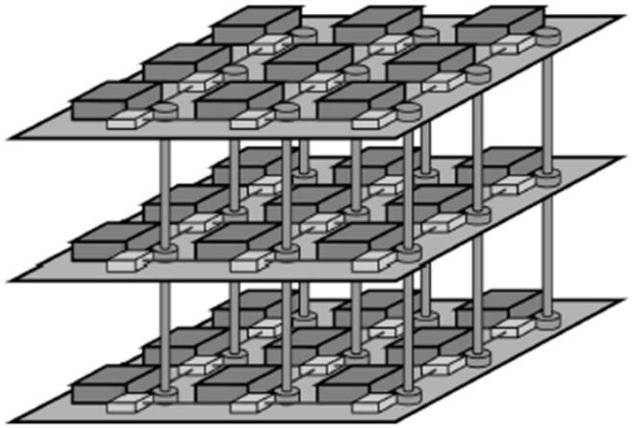
- Three-dimensional (3D) integration
  - Decreasing wire delay, increasing integration density and improving performance
  - Faced with heat dissipation and temperature problem



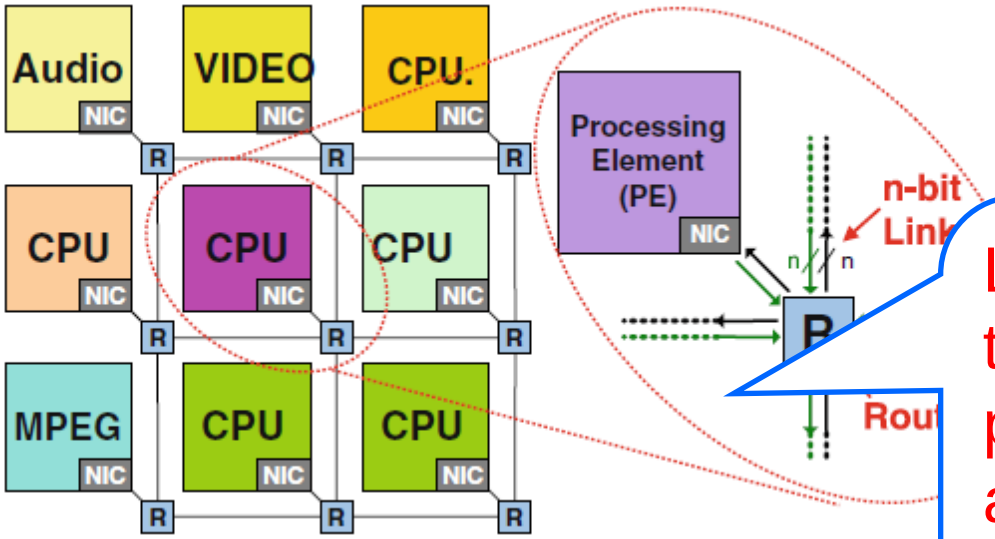




Network-on-chip



- Network-on-chip (NoC)
  - Brings networks into chip
  - Greatly reduce communication Cost



; of 3D

Lead to power waste, thermal problem, performance reduction and even hardware mistakes

Power Consumption

Total chip power

Core power

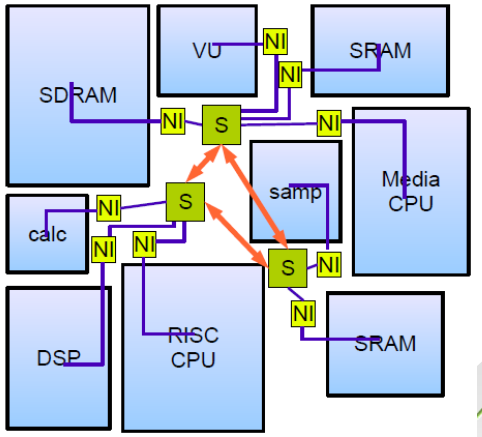
Communication power

capacitance

Voltage level

frequency

$$P_{core} = CV^2 f$$

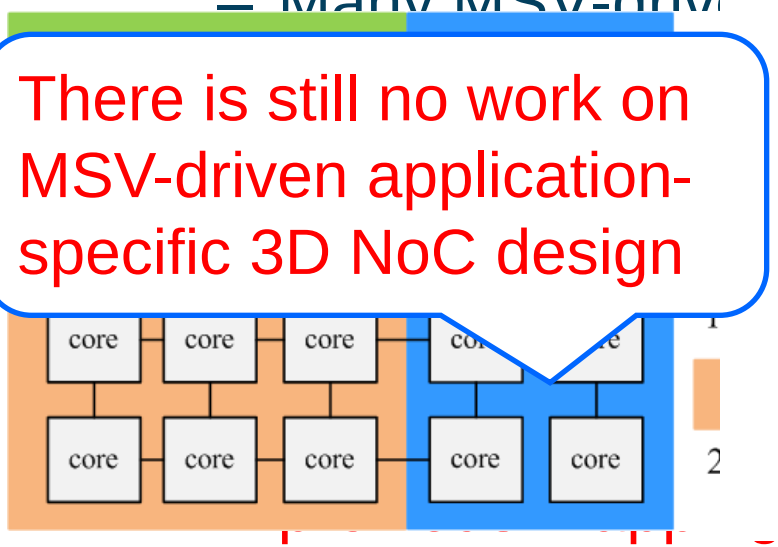


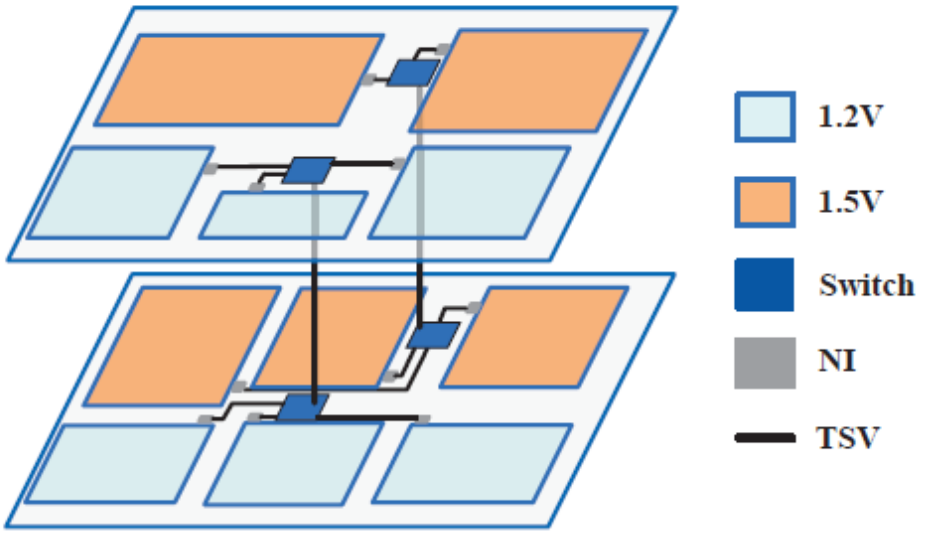
40% of the total power [GLSVLSI'11]

Multiple Supple Voltage

- Multiple Supple Voltage (MSV)
  - Partitions the circuit into domains of different voltage levels (Voltage Island)
  - Reducing power by assigning lower voltage to some blocks on chip
  - Many MSV-driv

There is still no work on MSV-driven application-specific 3D NoC design





NoC synthesis

- Communication power can be optimized through a good NoC synthesis
- Many designers proposed 3D NoC synthesis methods[ICCD'08, TCAD'10,ASPDAC'10]
- However, none of them considered the layer assignment problem, which can greatly affects the vertical communication power
- Besides, few of previous work thought of the usage of MSV technology on core power optimization

Challenges in MSV-driven 3D NoC

- Unlike traditional 2D … ign

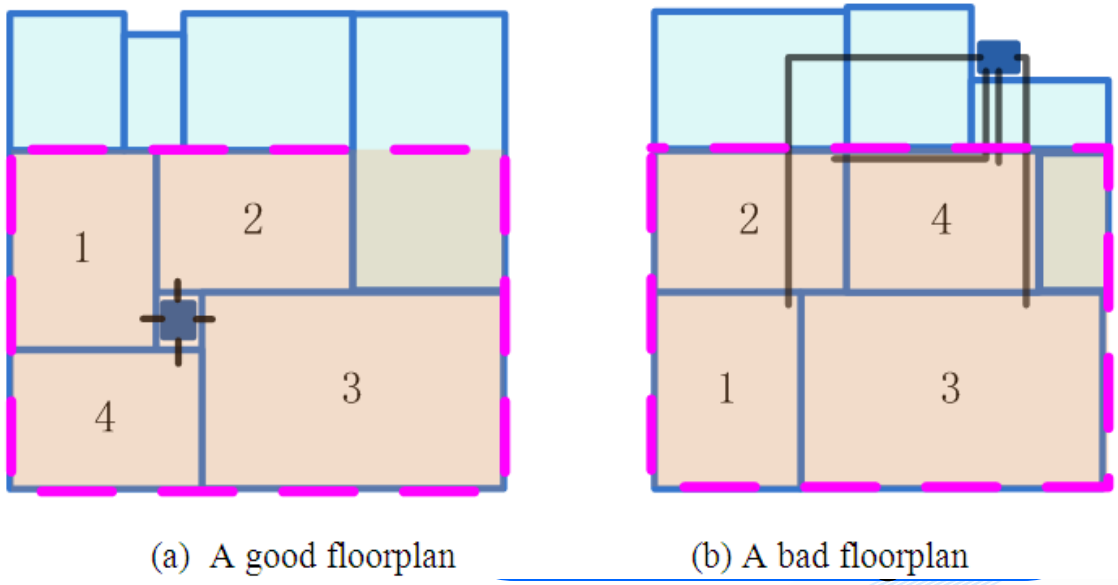
Affect the communication between layers

voltage levels affect core power directly

All previous work based on given floorplan or during

voltage levels cannot be simply assigned to each layer

A bad floorplan will lead to bad assignment and hence large communication power



(a) A good floorplan (b) A bad floorplan

Contributions

- In this paper, a MSV-driven framework is proposed for application-specific 3D NoC
  - 1. A unified ILP modeling method is proposed for taking into account both layer assignment and voltage level assignment
  - 2. 3D NoC synthesis is proposed with consideration of inter-layer communication optimization
  - 3. 3D NoC floorplanning with network component assignment considered is presented for communication power improvement.

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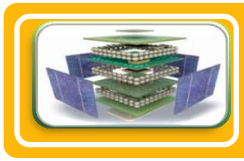
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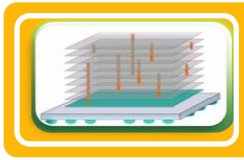
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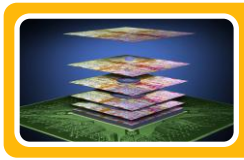
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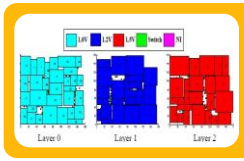
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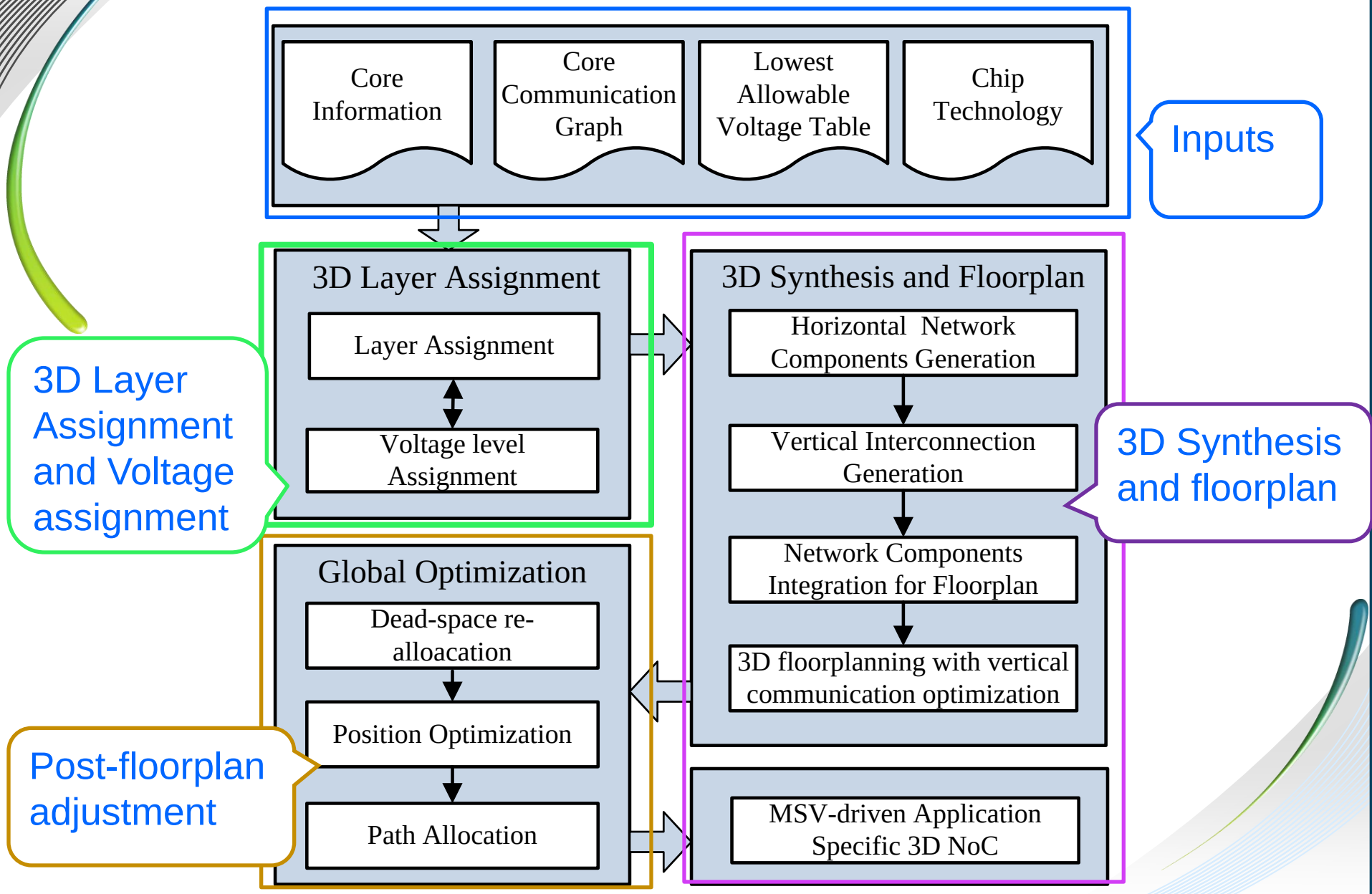
Overall Design Flow



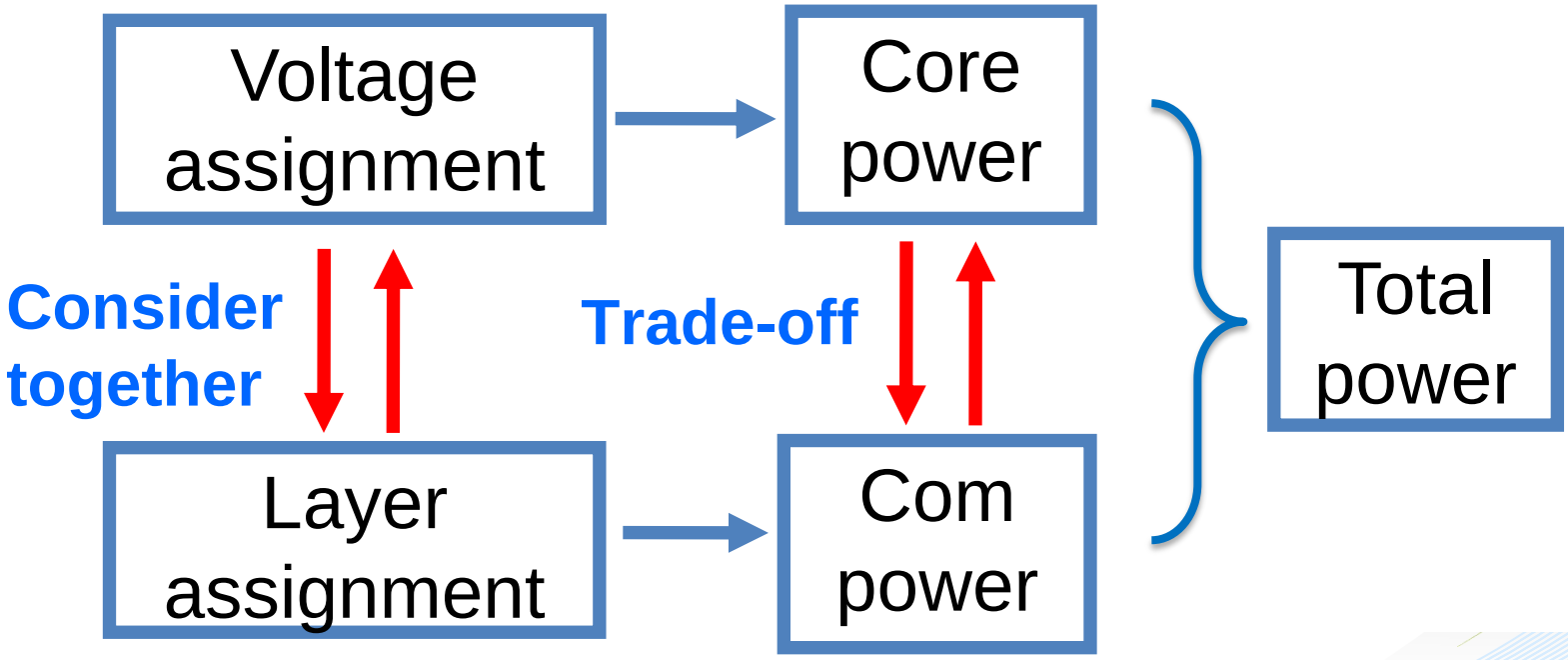
Overall Design Flow II

- Given:
  - (1) *N* cores with information of width and height
  - (2) communication graph
  - (3) *m* legal voltage levels
  - (4) the lowest allowable voltage table of each core and the corresponding power consumptions at different voltage levels
  - (5) the number of layers *n*
- The objective is:
  - Assigns *N* cores to *n* layers with a voltage assignment for each core, assigns network components on each layer, and determines the physical position of each core and component

The output is a generated legal 3D layout

MSV-driven Layer Assignment

- MSV-driven layer assignment
  - Two objects of achieving both optimizations of core power and communication power



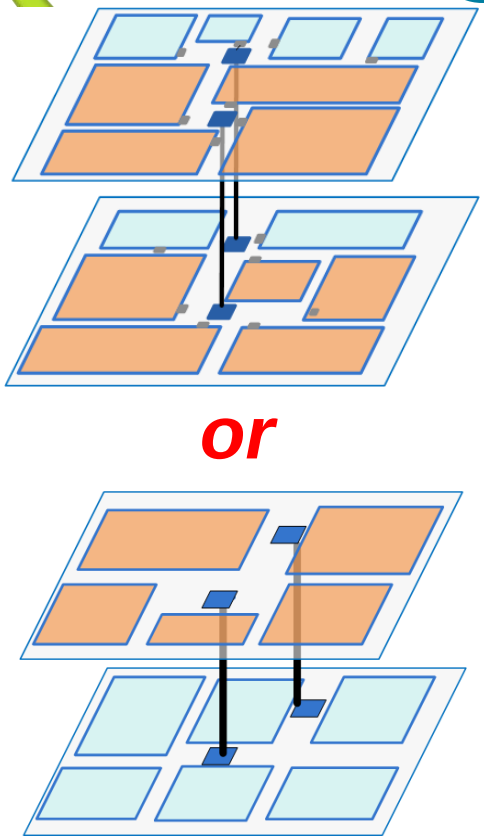
MSV-driven layer assignment

In this work, we assume that each layer aims to use the least number of voltage levels

m voltage levels → **Assigned** → *n* layers

MLA (m, n)

$vlmap$



or

?

Multiple P/G networks on each

To solve the I/R drop of P/G

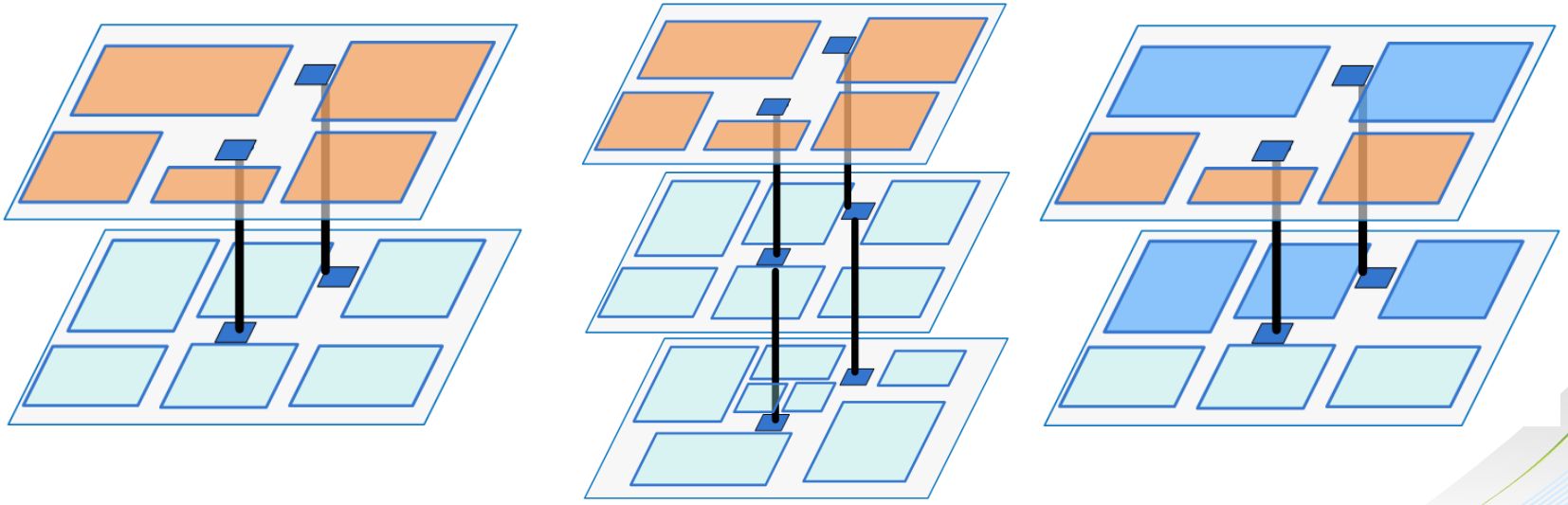
Multiple voltages on each layer

Easy to assign P/G networks as

Communication between voltage islands is cheaper as the interconnection between layers is much shorter

How to do together?

- *How to solve MLA (m, n)?*
  - *m* = *n*: Single voltage level in each layer
  - *m* > *n*: Single voltage level in multi-layers
  - *m* < *n*: Multi-voltage levels in each layer



The case of *m*= *n*

$MLA\ (n, n)$

Total core power

Total communication cost

- Objective:

$$+ P_{com}$$

P_{vcom} — Vertical communication

P_{hcom} — Horizontal communication

power consumption of core *i* when assigned to layer *l*

Where

$$P_{core} = \sum_{l=1}^{n} \sum_{i=1}^{N} P_{il} \cdot x_{il}$$

If core *i* is assigned to layer *l*

Vertical cost including communication and voltage level conversion

$$P_{vcom} = Cost_{TSV} \cdot \sum_{i=1}^{N} \sum_{j=1}^{N} \sum_{l=1}^{m} \sum_{k=l+1}^{m} Com_{ij} \cdot v_{il} \cdot v_{jk}$$

communication amount between core *i* and core *j*

Constraints:

$$\sum_{l=1}^{n} x_{il} = 1 \ where \ x_{il} = 0 \ or \ 1, \forall 1 \le i \le N$$

Core *i* is assigned to one and only one layer

$$\sum_{l=0}^{v_i - 1} x_{il} = 0, \sum_{l=v_i}^{n} x_{il} \ge 1 \ \&$$

vi is the lowest available level for core i

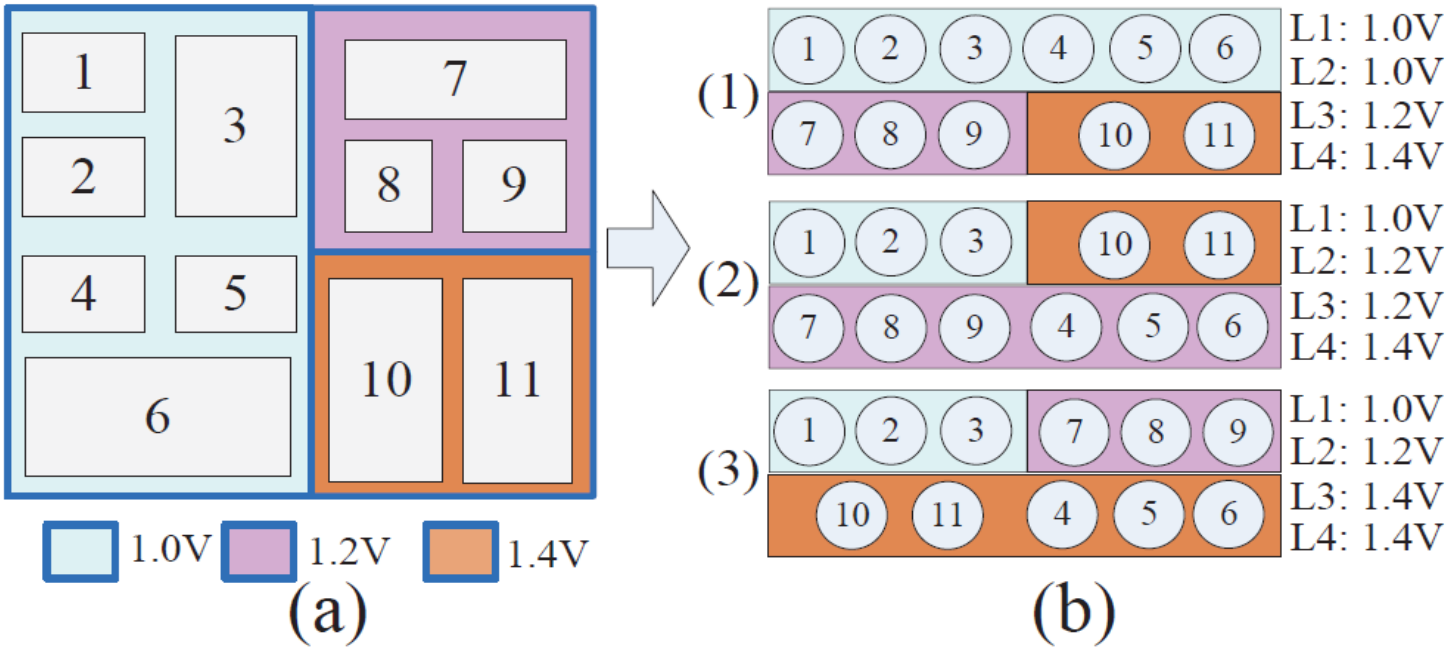
area-balanced constraint

$$\sum_{i=1}^{N} area_i \cdot x_{il} \le \frac{1}{n} \cdot Area + \xi \cdot Area$$

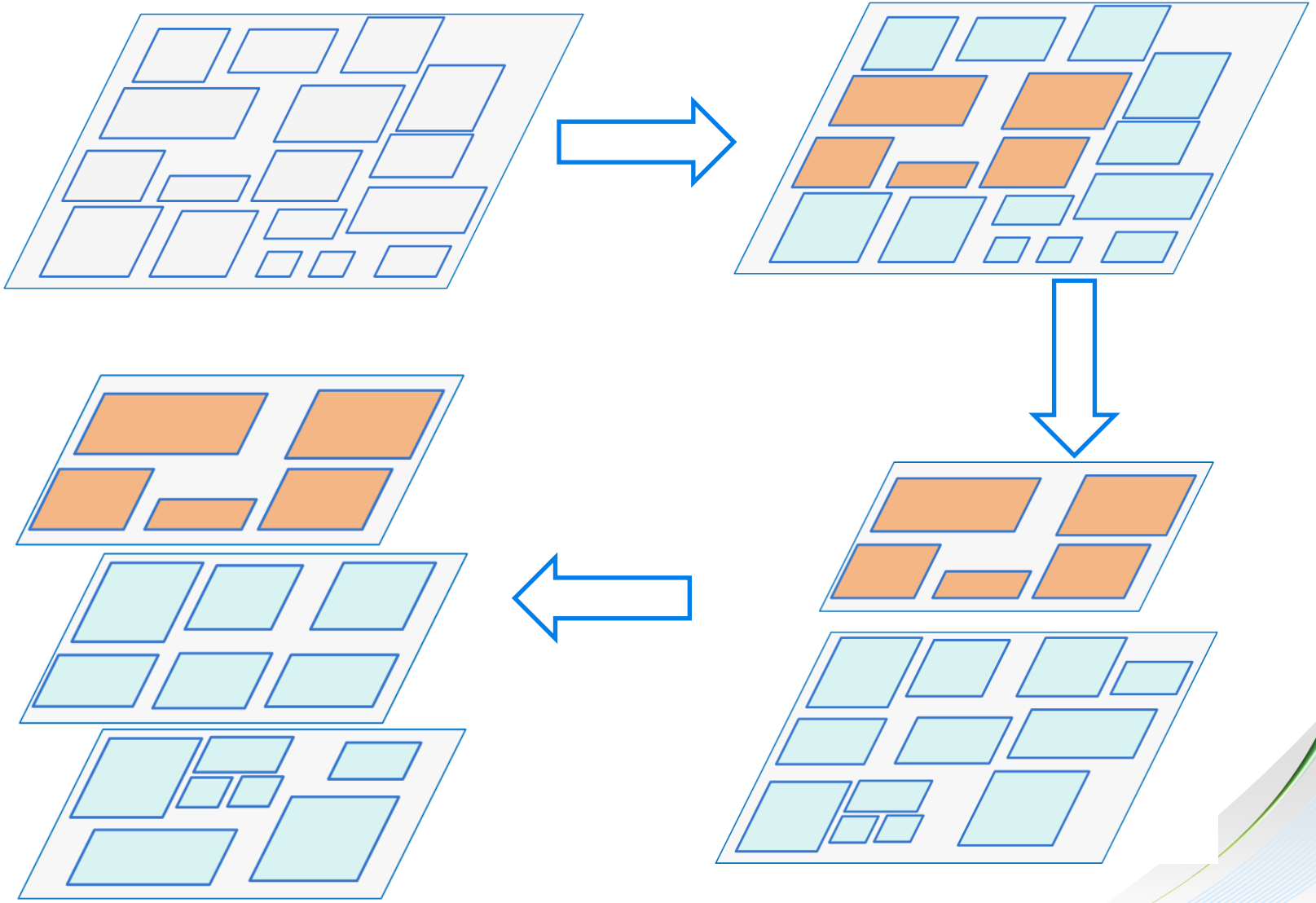
ξ is a slack variable for acceptable error on area balance and in this work, *ξ* is set to 0.01

The case of *m* < *n*

- m < n: one voltage on multi-layers
  - Which layers to share the same voltage?
  - First, *vlmap* candidates generation to



The case of $m < n$



The case of *m* > *n*

- m > n: more than one voltage island on each layer
  - Which voltages on each layer?
  - – Voltage assignment on 2D NoC
    - Mapping 3D cores onto 2D NoC
    - Do *m* voltage assignment on 2D NoC
    - Compare total cost of different combination
  - – Modified Core communication graph
    - Communication cost and connection cost to separate the cores in the same voltage island
  - – Area balanced partition

Variable Pruning for ILP

- As a result of area-balanced constraints, the ILP formulation is exact but time-consuming
  - It takes thousands of seconds to solve even small cases
- An ILP variable pruning method is proposed inspired by that
  - If core *i* connect few other cores or the communication cost generated by core *i* is small, then core *i* can be assigned to the lowest allowable voltage level

Variable Pruning for ILP

Algorithm 1 Variable Pruning for ILP

Require: N, m, Li, Com_{ij}, LAV_i;

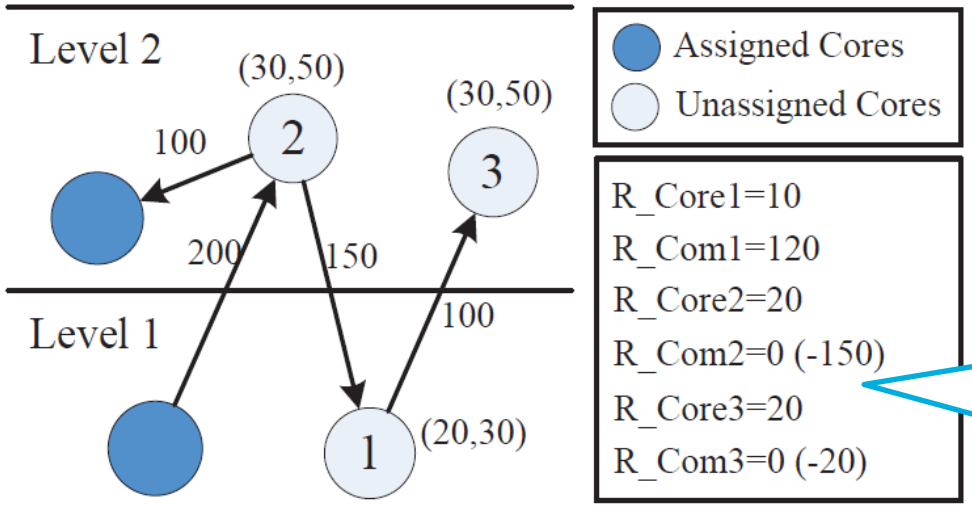
1: Sort cores according to lowest allowab
2: **for** each $i \in [1, N]$ **do**
3: **if** core i is assigned **then**
4: **continue**;
5: **end if**
6: $checkLargeCom()$;
7: $R\_coreCaculation(i)$;
8: $R\_comCaculation(i)$;

R_corei denotes the increased power of core *i from current voltage level to higher* level

...according to the lowest ...owable levels

R core and R com are calculated respectively for each core

R_comi denotes the potential communication power of core *i*



The cores in each group are inserted into each layer until the area of layer exceeds a ...tio is

After that the variables for the already assigned cores are updated and *R core and R com* are re-calculated.

21: **end while**
22: ILP solving of the rest unassigned cores;

For the rest unassigned cores, use ILP to solve them

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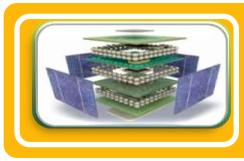
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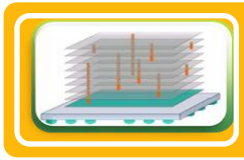
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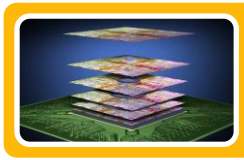
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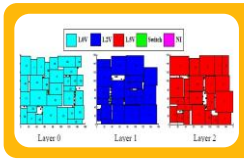
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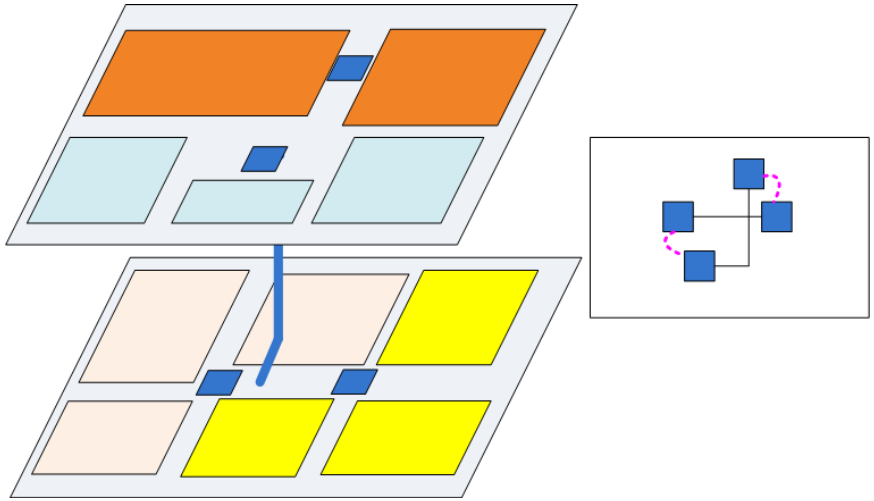
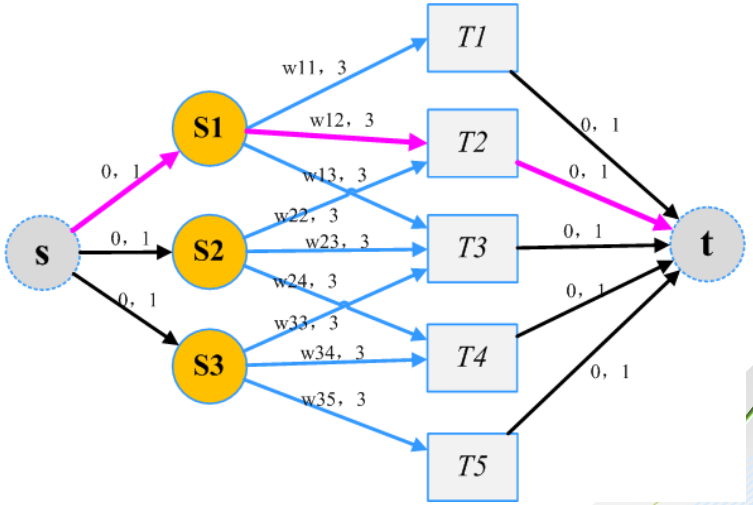
3D NoC Synthesis

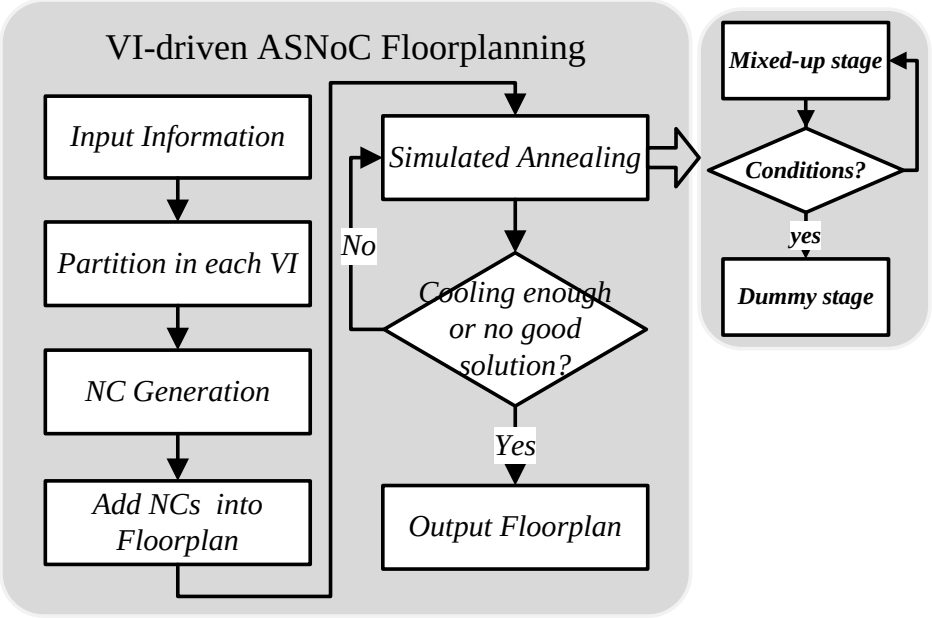
- 3D NoC is a 3D network including inner-layer networks and inter-layer interconnection
  - Inner-layer NoC synthesis [DAC'09]
  - Inter-layer TSV planning





Voltage Island Driven Floorplan

- Network components are integrated into floorplanning and the positions can be improved through floorplanning process



Two stage-disturbance is used to eliminate the redundancy in solution space

$$Cost_i = \alpha \cdot Area_i + \beta \cdot VIArea_i + \gamma \cdot Com_i + \lambda \cdot \sum_{j=0}^{i} Vcom_{ij}$$

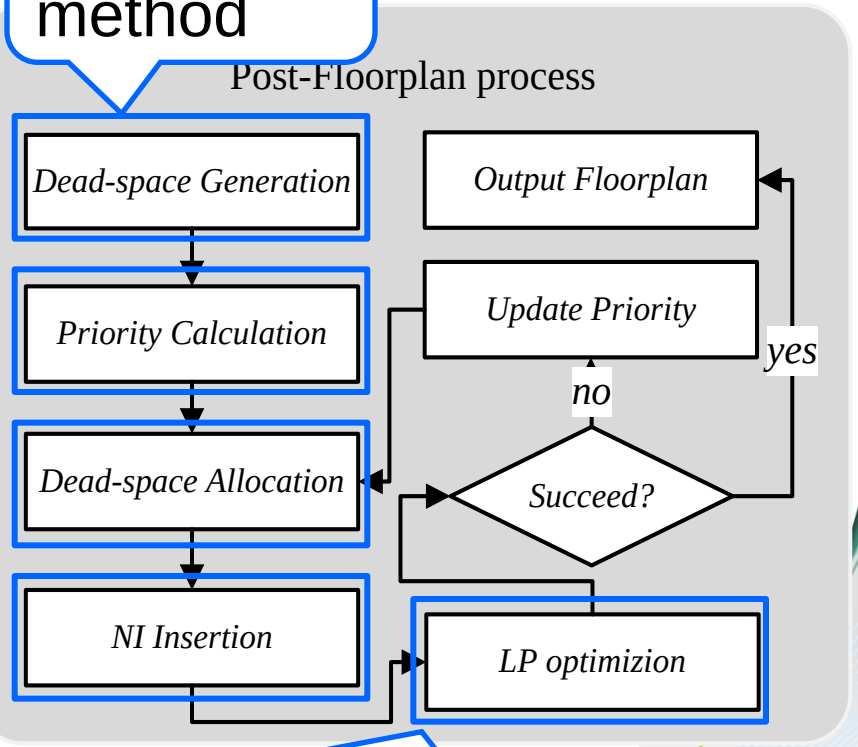
Post- Floorplan Processing

- A post-floorplan dead-space re-allocation and LP based optimization algorithm is proposed to further improve comm power.

$$comCost_{i,k} = \sum_{j=0}^{N} Com_{kj} * length_{ij} + \sum_{t=0}^{Ns} Com_{kt} * length_{it}$$

```
Function DS_Allocation:
Method:
orderDummyCoresByComs(); //order Switches by communication amount
For (i between 1 and Ns){ //Search for all dead-space for each switch
  orderDS(i); //order all dead-space by weighted wire length
  For (j between 1 and Nds) {
    if (enoughSpace(i, DSj)==True){//There is enough space for Switch i
      allocate(i, j); //Allocate core I to dead-space j
      updateSpace(j);//update the space by reduce the size of switch i
    }}
}
```

Line-scan method



Network flow based algorithm is used for NI insertion

Positions optimization

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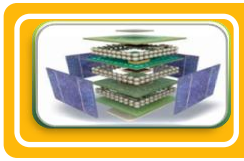
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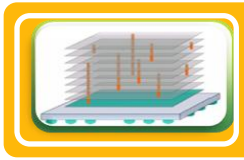
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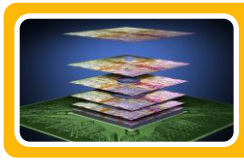
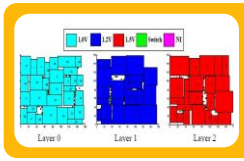

3D NoC Synthesis


Experimental Results


Conclusion

Effect of Layer Assignment Algorithm

Table 1: Results of MSV-driven Layer Assignment Algorithm

Benchmark	L#	V#	E#	ILP			Area Balanced Method			Heuristic ILP		
				Core Power	Inter-layer Com	Run time(s)	Core Power	Inter-layer Com	Run time(s)	Core Power	Inter-layer Com	Run time(s)
					44							13
					79							
					78							
					33							
					76							
					84							
					45							
												2
D_76	2	76	92	-	-				0.01	94.4	81.4	1.75
	3	76	92	-	-		149.7	111.4	0.01	104.1	138.6	63.0
	4	76	92				149.7	151.6	0.01			
	-	-	-	1	1	1	-	-	-	0.998	1.062	0.018
	-	-	-	-	-	-	1	1	1	0.664	1.098	-

Pure ILP solving without any strategy

Area balanced method for only vertical cost optimization

The proposed method with ILP variable pruning

- Compared to ILP formulation, the proposed algorithm can save time greatly by 98.2% with only 6% more power
- Compared to the partition method, the proposed method can improve core power by 33.6% with only 9.8% increase on communication power, which achieves good trade-off between core power and communication power.

Effect of NoC Synthesis

Table 2: Effect of post-floorplan global redistribution

Benchmark	L#	V#	F#	Inner Optimization			Inter Optimization			Global Optimization			
				Inter Power	Inner Power	Com Power	Inter Power	Inner Power	Com Power	Inter Power	Inner Power	Com Power	Run-time (s)
				30					7.15				5.02
				44					0.09				16
				40					7.15				44
				23					9.52				54
				38					2.10				74
				34					9.30				00
				42					5.18				82
				51					7.65				41
	4	52	61	79					5.38				14
D_76	2	76	92	60.					158.8				65.13
	3	76	92	139.4	93.91	233.3	72.08	103.2	175.2	39.77	105.1	144.9	60.36
	4	76	92	89.34	81.10	170.4	62.07	81.38	143.4	37.59	81.57	119.2	82.29
Ratio	-	-	-	1	1	1	0.642	1.038	0.831	0.392	1.047	0.709	-

Consider only horizontal communication optimization

Consider trade-off between horizontal and vertical communication

Global redistribution after floorplan

- Inter-layer communication can improve by about 35.8% with only 3.8% increase on inner-layer communication power, total power can be improved by 16.9%
- Global optimization can improve inter-layer communication by 60.8% and total power by 29.1%

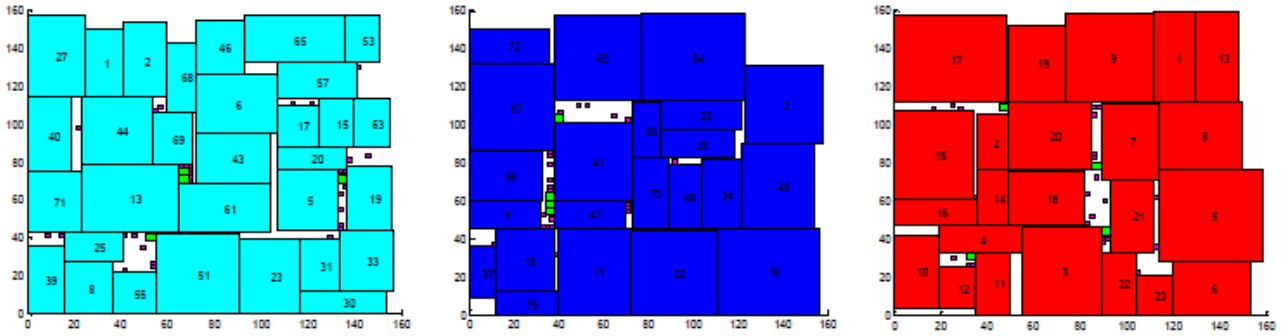
Effect of MSV-3DNoC

Table 3: Effect of MSV-3DNoC

Benchmark	L#	V#	E#	MSV-2DNoC			MSV-3DNoC			
				Core Power	Com Power	Dead Space	Core Power	Com Power	Dead Space	Run-time (s)
D_38_tvopd	2	38	46	46.2	95.96	14.39	47.3	54.12		44.7
	3	38	46		95.96	14.39	51.7	48.77		37.7
					96	14.39				
D_36					.4	11.99				
					.4	11.99				
					.4	11.99				
D_52					.8	19.56				
					.8	19.56				
	4	52	61	77.8	135.8	19.56				
D_76	2	76	92	92.4	264.1	23.83	94.4	139.1	23.83	65.1
	3	76	92	92.4	264.1	23.83	104.1	144.9	13.36	60.3
	4	76	92	92.4	264.1	23.83	101.8	119.2	18.65	82.2
Ratio			-	-	1	1	1	1.098	0.523	1.034	-

MSV-2D NoC in GLSVLSI'12

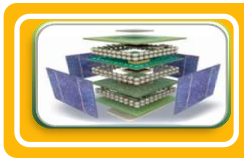
The proposed 3D-NoC

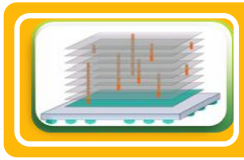


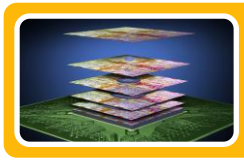
Layer 0 Layer 1 Layer 2

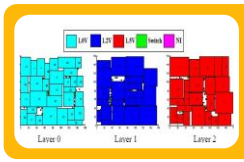
Floorplan for D_76

Outline


Introduction


MSV-driven Layer Assignment


3D NoC Synthesis


Experimental Results


Conclusion

Conclusion

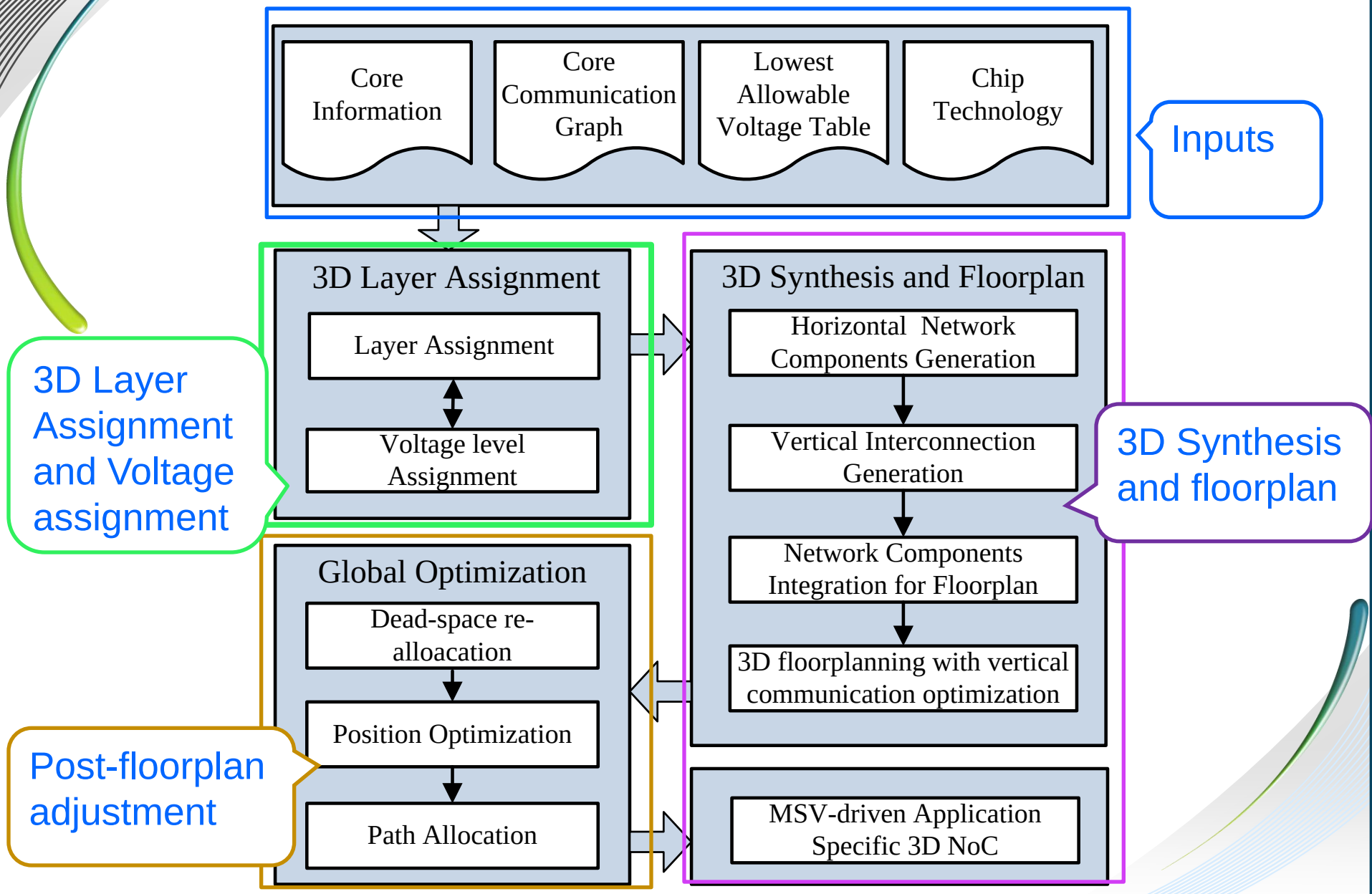
- In this paper, a MSV-driven framework for application-specific 3D NoC design is proposed.
- Through a unified modeling method for simultaneously layer assignment and voltage assignment, 3D NoC synthesis and 3D floorplanning algorithm, the total power can be optimized.
- Compared to MSV-driven 2D NoC, the proposed method can improve total chip power greatly

Thanks

Q&A

Email: wangkan09@mails.thu.edu.cn

Overall Design Flow



The case of *m*= *n*

$MLA\ (n, n)$

Total core power

Total communication cost

- Objective:

$$+ P_{com}$$

P_{vcom} — Vertical communication

P_{hcom} — Horizontal communication

power consumption of core *i* when assigned to layer *l*

Where

$$P_{core} = \sum_{l=1}^{n} \sum_{i=1}^{N} P_{il} \cdot x_{il}$$

If core *i* is assigned to layer *l*

Vertical cost including communication and voltage level conversion

$$P_{vcom} = Cost_{TSV} \cdot \sum_{i=1}^{N} \sum_{j=1}^{N} \sum_{l=1}^{m} \sum_{k=l+1}^{m} Com_{ij} \cdot v_{il} \cdot v_{jk}$$

communication amount between core *i* and core *j*

Constraints:

$$\sum_{l=1}^{n} x_{il} = 1 \ where \ x_{il} = 0 \ or \ 1, \forall 1 \le i \le N$$

Core *i* is assigned to one and only one layer

$$\sum_{l=0}^{v_i - 1} x_{il} = 0, \sum_{l=v_i}^{n} x_{il} \ge 1 \ \&$$

vi is the lowest available level for core i

area-balanced constraint

$$\sum_{i=1}^{N} area_i \cdot x_{il} \le \frac{1}{n} \cdot Area + \xi \cdot Area$$

ξ is a slack variable for acceptable error on area balance and in this work, *ξ* is set to 0.01

The case of *m*= *n*

$MLA\ (n, n)$

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Total communication cost

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Variable Pruning for ILP

Algorithm 1 Variable Pruning for ILP

Require: N, m, Li, Com_{ij}, LAV_i;

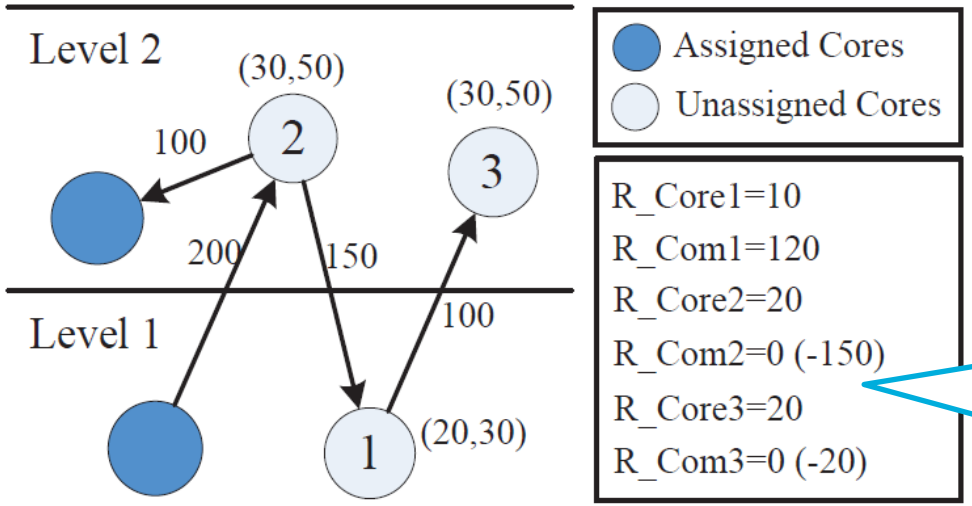
1: Sort cores according to lowest allowab
2: **for** each $i \in [1, N]$ **do**
3: **if** core i is assigned **then**
4: **continue**;
5: **end if**
6: $checkLargeCom()$;
7: $R\_coreCaculation(i)$;
8: $R\_comCaculation(i)$;

R_corei denotes the increased power of core *i from current voltage level to higher* level

...according to the lowest ...owable levels

R core and R com are calculated respectively for each core

R_comi denotes the potential communication power of core *i*



The cores in each group are inserted into each layer until the area of layer exceeds a ...tio is

After that the variables for the already assigned cores are updated and *R core and R com* are re-calculated.

21: **end while**
22: ILP solving of the rest unassigned cores;

For the rest unassigned cores, use ILP to solve them

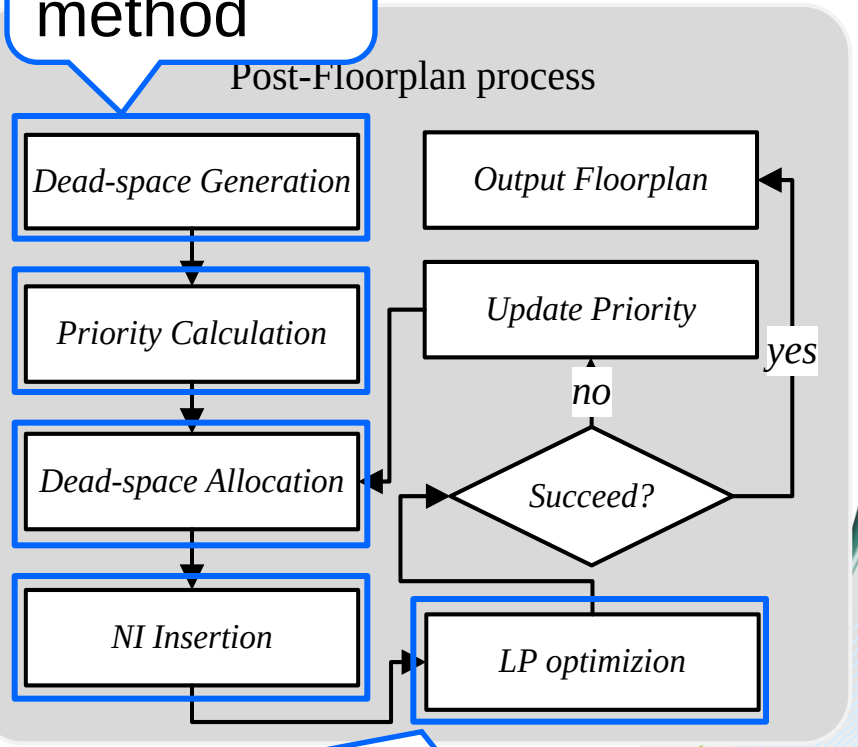
Post- Floorplan Processing

- A post-floorplan dead-space re-allocation and LP based optimization algorithm is proposed to further improve comm power.

$$comCost_{i,k} = \sum_{j=0}^{N} Com_{kj} * length_{ij} + \sum_{t=0}^{Ns} Com_{kt} * length_{it}$$

```
Function DS_Allocation:
Method:
orderDummyCoresByComs(); //order Switches by communication amount
For (i between 1 and Ns){ //Search for all dead-space for each switch
  orderDS(i); //order all dead-space by weighted wire length
  For (j between 1 and Nds) {
    if (enoughSpace(i, DSj)==True){//There is enough space for Switch i
      allocate(i, j); //Allocate core I to dead-space j
      updateSpace(j);//update the space by reduce the size of switch i
    }}
}
```

Line-scan method



Network flow based algorithm is used for NI insertion

Positions optimization

Experimental results

- Environment:
  - Workstation: 3.0 GHz CPU, 4GB memory
  - Tool: *hmetis* for partition *and lp_solve* for ILP and LP solving
  - Benchmark: *D_38_tvopd* is used from [6] and *D_36*, *D_52* and *D_76* are derived from *D_38_tvopd*
  - The power model of network components and communication is evaluated according to [ASPDAC'10]