A Novel Cell Placement Algorithm for Flexible TFT Circuit with Mechanical Strain and Temperature Consideration

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Presenter : Jiun-Li Lin

Outline

- Introduction
- Problem formulation
- Algorithm
- Experimental results
- Conclusion

Introduction (1/4)

Depth : 7.6 mm
Weight : 112 gram

Lightweight
&
Thin

Apple iPhone 5

Introduction (2/4)

Samsung bendable phone

Introduction (3/4)

Lightweight

Thin

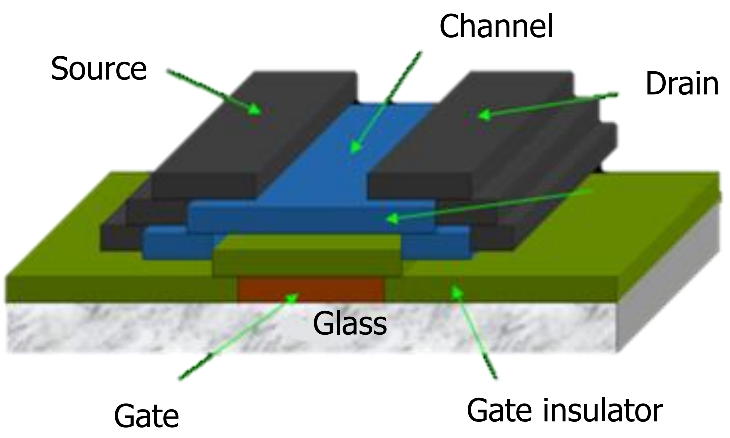
Bendable

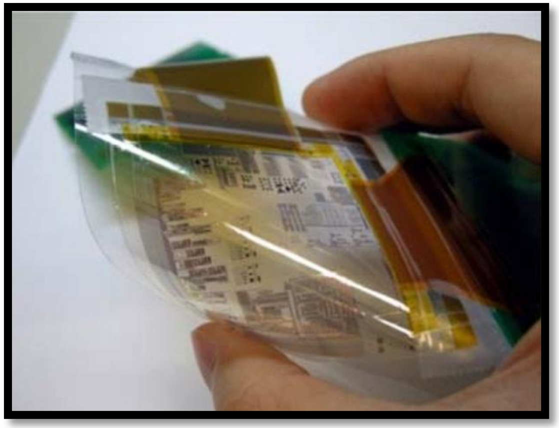
TFT

Portability + **Flexibility**

Introduction (4/4)

- Thin-film transistor (TFT)
- Flexible TFT technology has many advantages
  - Low manufacturing cost
  - Short manufacturing time
  - Light weight
  - Flexibility



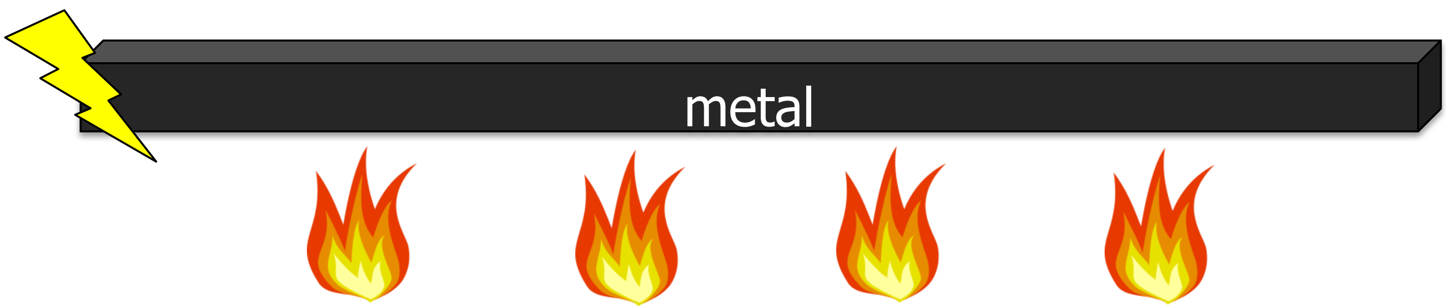


- Challenges
  - Mobility variation

Mobility

- Mobility determines how quickly an electron can move through metal or semiconductor

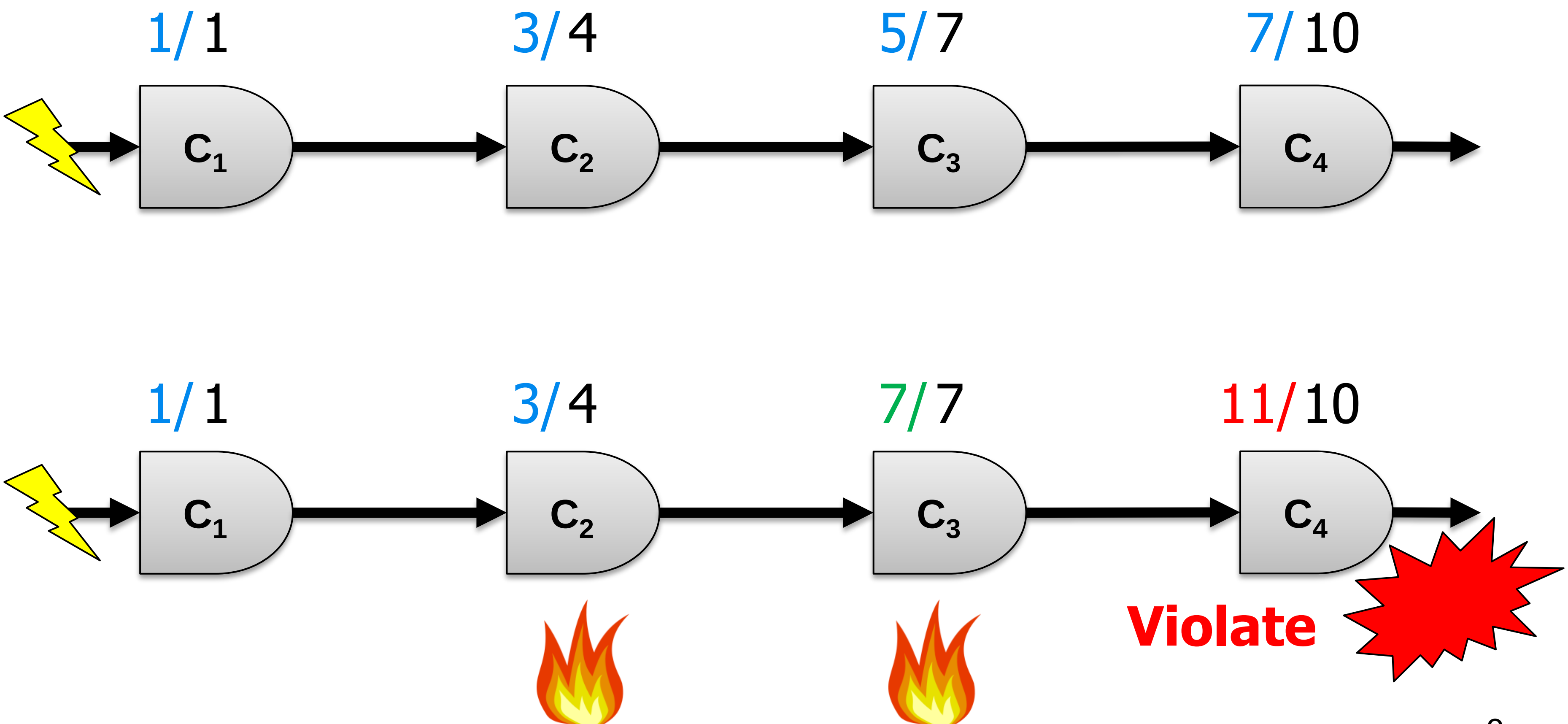
- Mobility may change under outside effects, called mobility variation, which makes a great impact on the cell delay



  - Mechanical strain
  - Temperature

Mobility Variation

- Mobility variation may leads to timing violations
  - Mechanical strain
  - Temperature

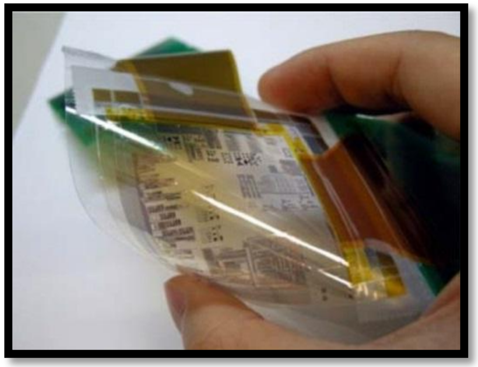


Mechanical Strain Effects

- Mobility variation under mechanical strain in different TFT technologies

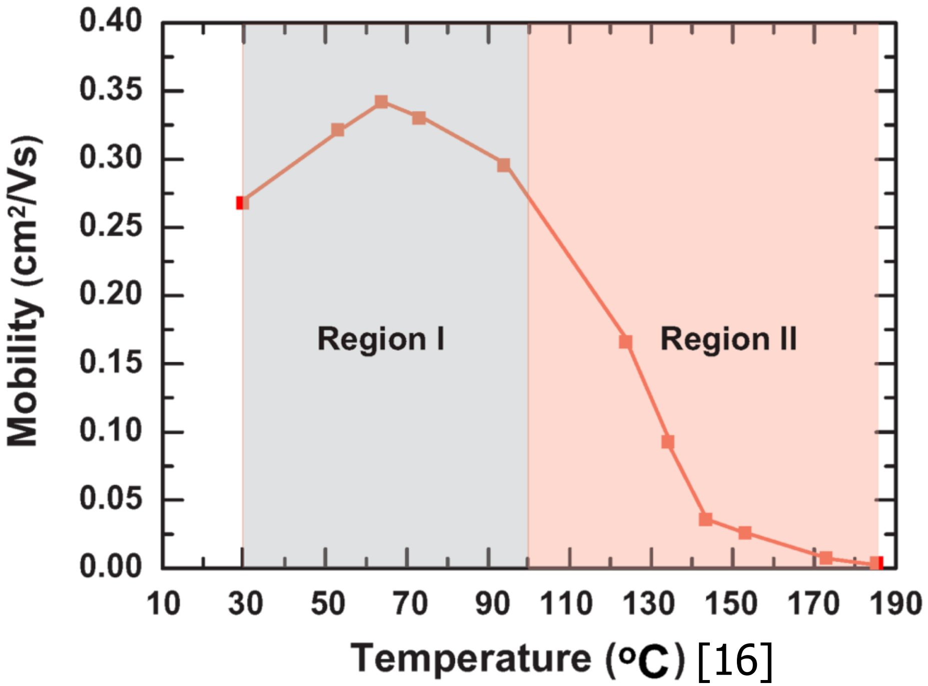
TFT technology	Compressive strain	Tensile strain
a-Si TFT	-26%	8%
organic TFT	20%	-30%
poly-Si TFT	44%	-44%
A-IGZO TFT	-2%	3%

- Separate cells which locate on critical paths



Temperature Effects

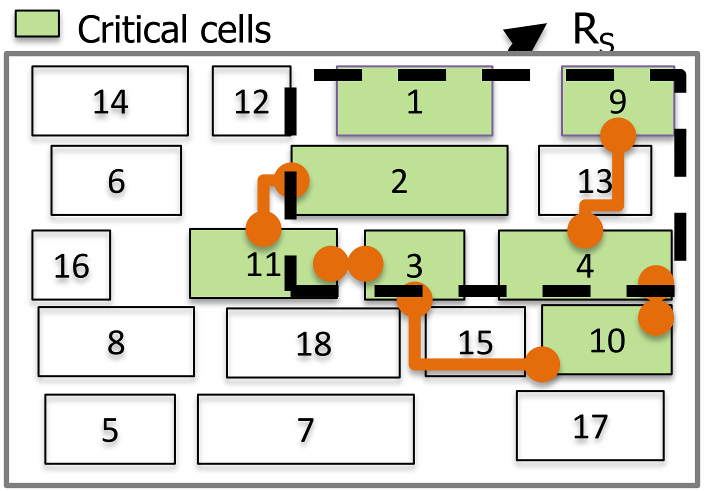
- Better mobility is obtained when temperature locates in Region I



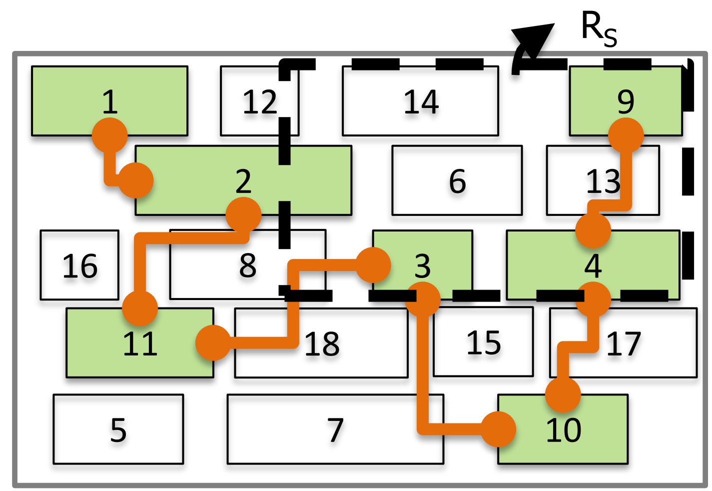
- To make the temperature close to Region I, hot cells are required to be adequately separated

[16]M. Zhu, G. Liang, T. Cui, and K. Varahramyan. Temperature and field dependent mobility in pentacene-based thin film transistors. Solid-State Electronics, 49(6):884–888, 2005

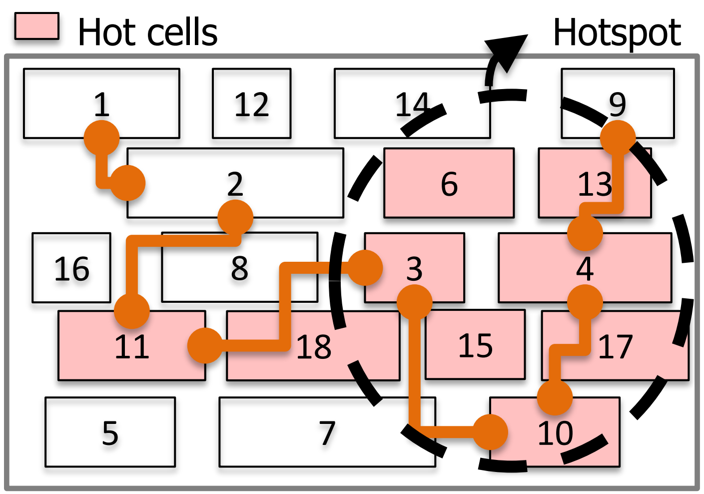
Placement Examples



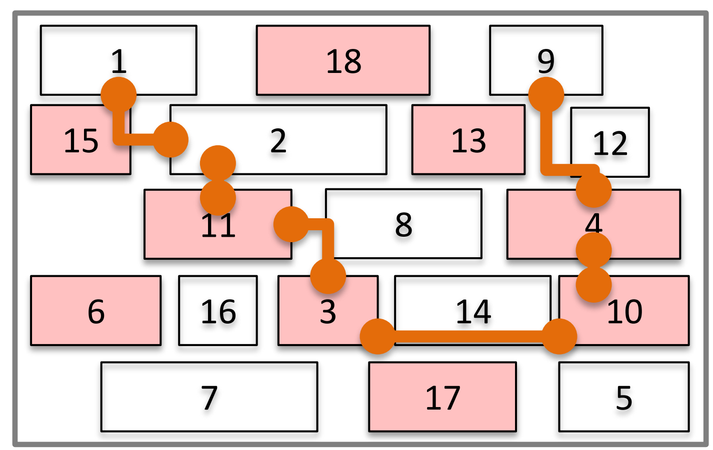
(a) Wirelength consideration only



(b) Mechanical strain consideration



(c) Mechanical strain consideration



(d) Both Mechanical strain and Temperature

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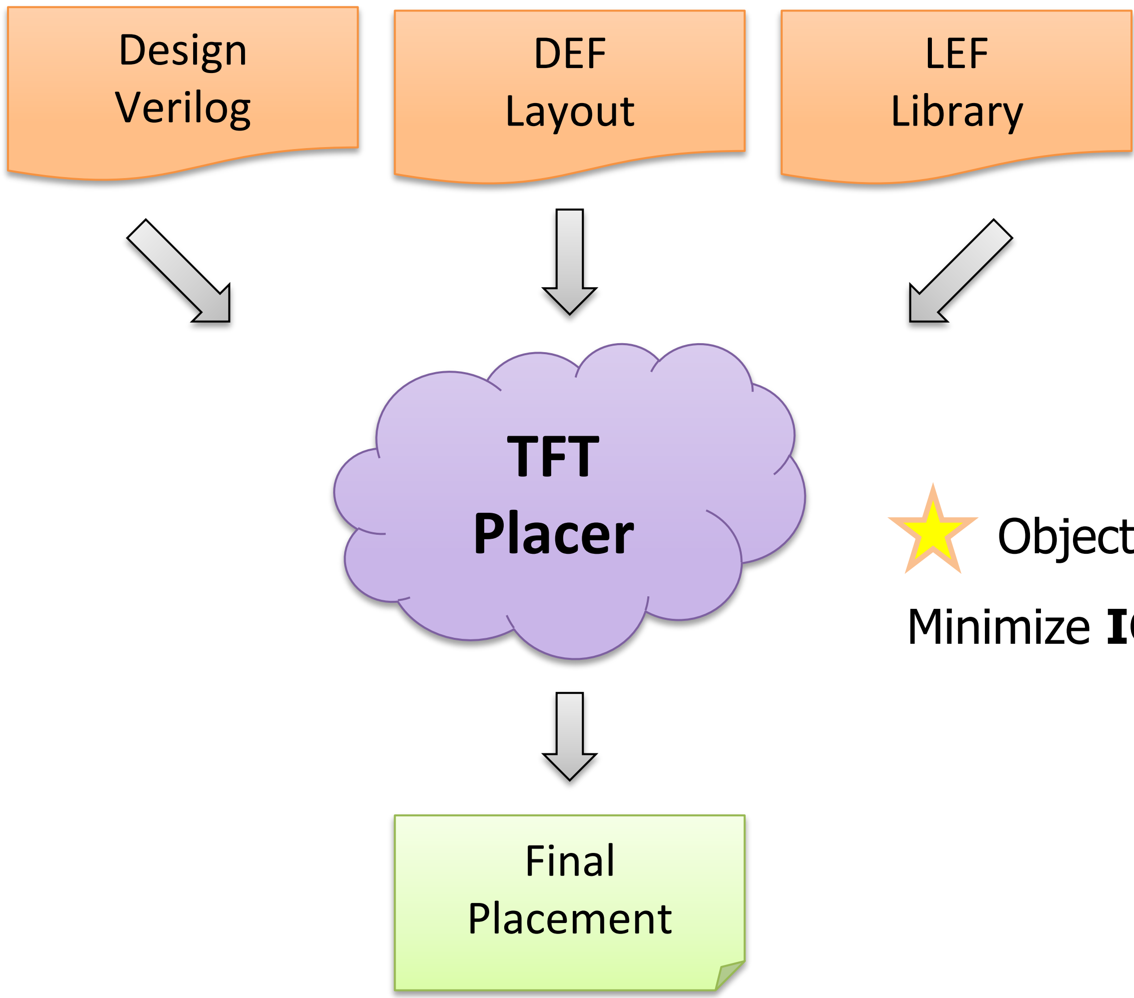
Problem Formulation



Objective

Minimize **ICPD**

What is ICPD

- Increase in critical path delay (ICPD)

$$ICPD = \frac{\mu_w - \mu_o}{\mu_o} \times 100\%$$

μ_w : the critical path delay in **working temperature** (by simulation) and with **mechanical strain**

μ_o : the critical path delay in **room temperature** (30℃) and with **no mechanical strain**

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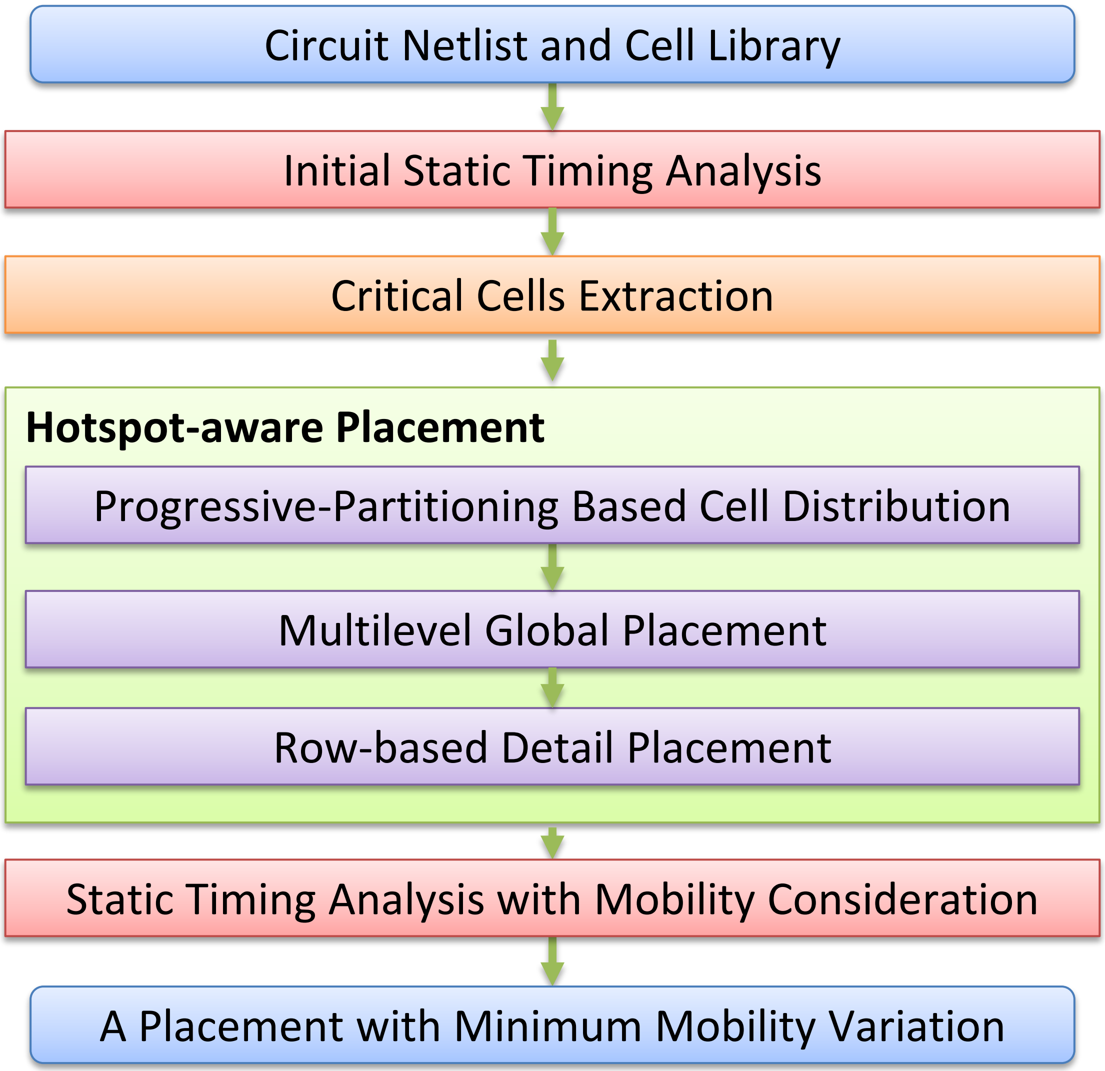
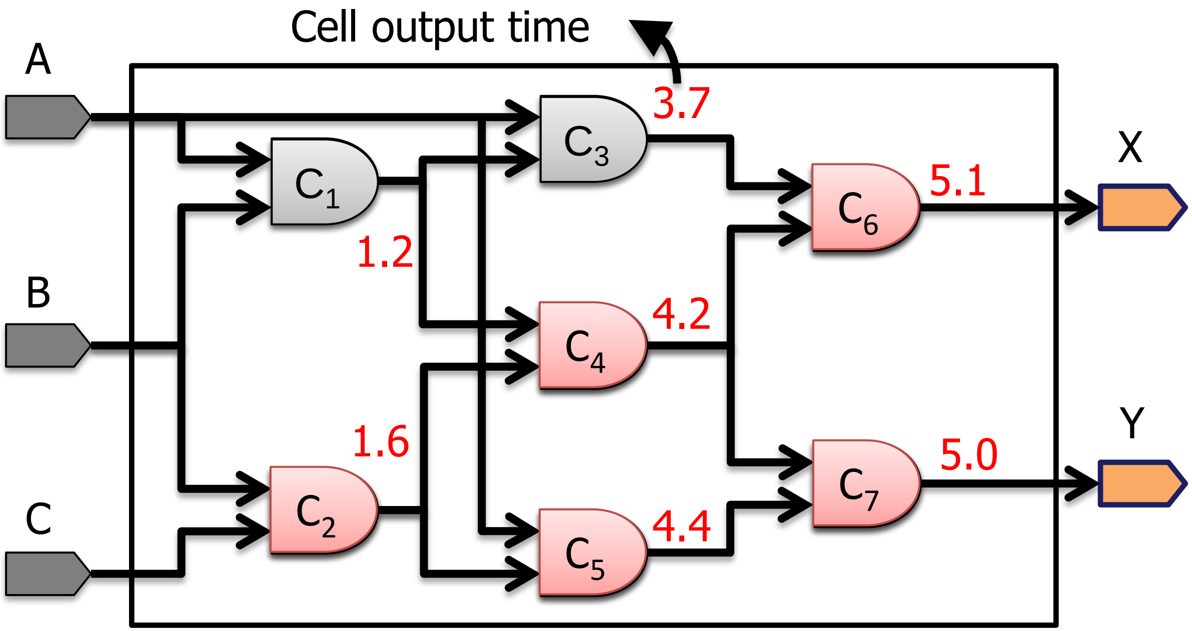
Algorithm Flow



Critical Cells Extraction

- In order to accurately catch the critical path under the impact of temperature, several circuit paths with largest path delay will be chosen as the critical paths



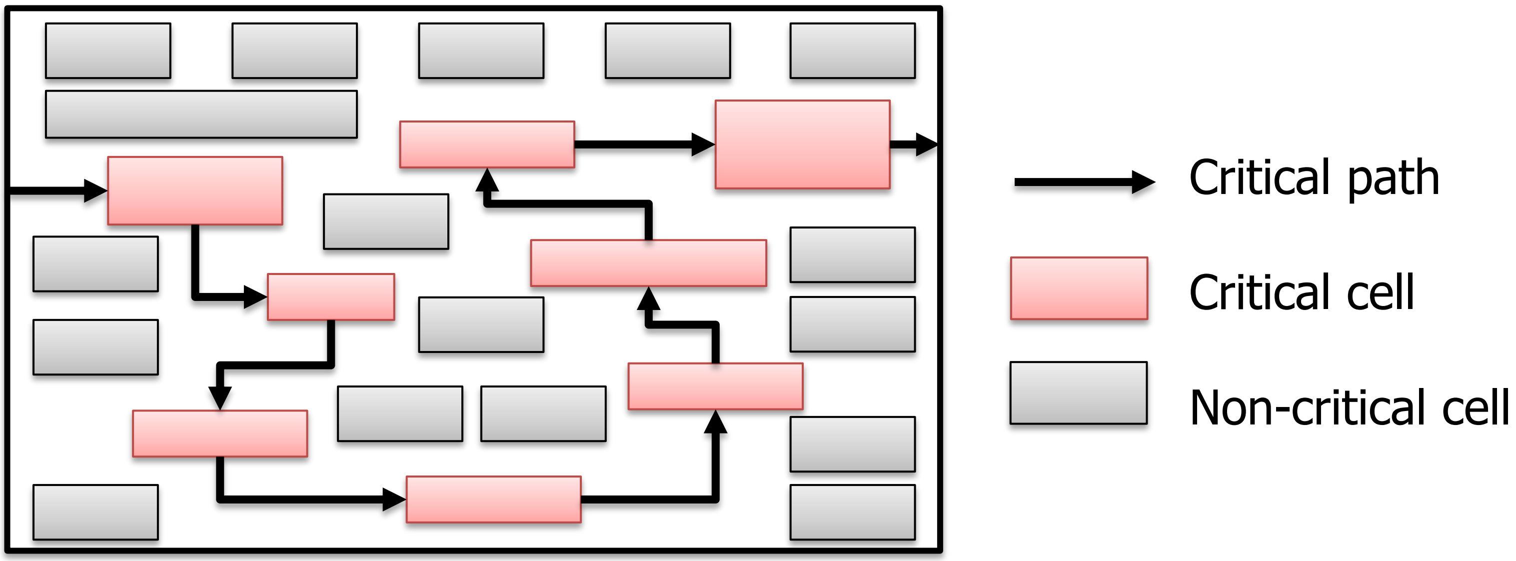
Critical path P_1: $C_2 \rightarrow C_4 \rightarrow C_6$

Critical path P_2: $C_2 \rightarrow C_5 \rightarrow C_7$

: Input pin : Cell : Output pin

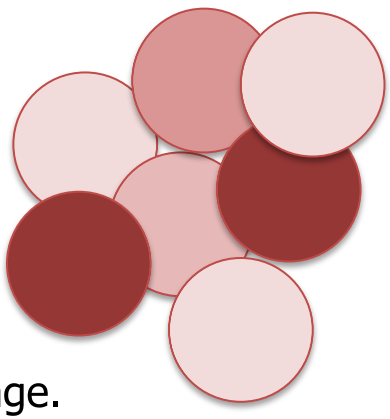
Progressive-Partitioning Based Cell Distribution

- Cells are classified into two categories
  - Critical cells
  - Non-critical cells
- Progressive-Partitioning Based Cell Distribution
  - Thermal-aware non-critical cells distribution
  - ILP-based critical cells distribution



Thermal-aware Non-critical Cell Distribution

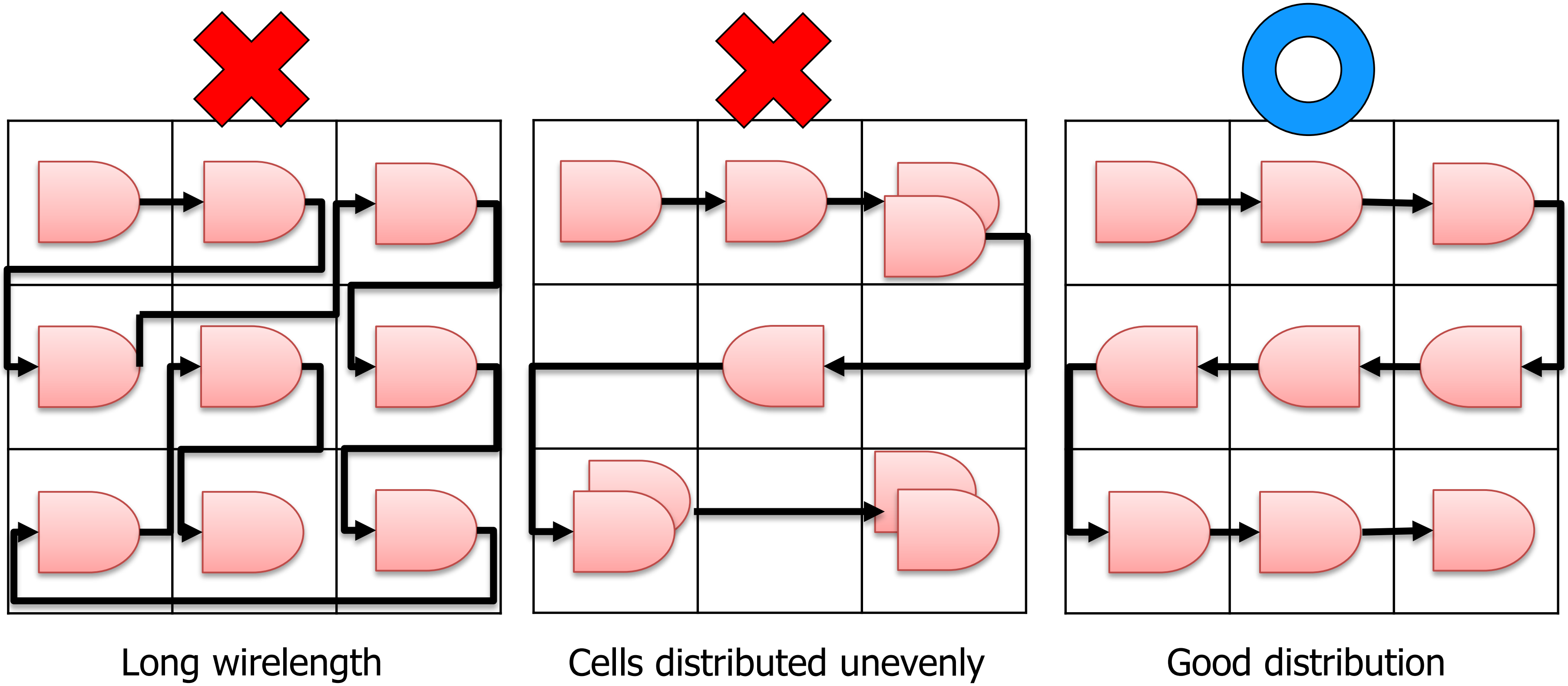
- Since heat has great impact on mobility, non-critical cells must be separated properly by ***power density*** (power per unit area)
- Cells must be distributed into bins meanwhile minimize the difference of total power density between bins
- A K-way graph partitioning method (hMetis [7]) is applied to distribute all non-critical cells to different groups while minimizing total wirelength and the chip temperature
- Power density as the weight



[7] G. Karypis and V. Kumar. hMETIS: A Hypergraph Partitioning Package. http://glaros.dtc.umn.edu/gkhome/metis/hmetis/download, 1999.

ILP-based Critical Cell Distribution

- For mobility and chip performance, critical cells need to
  - Separated evenly in all bins
  - Distributed while minimizing wirelength



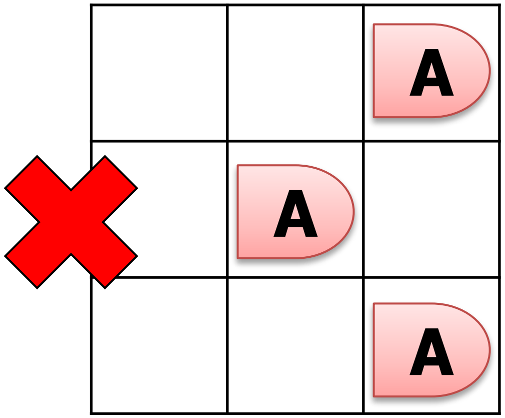
ILP Notations

P	a set of critical paths
C_i	a set of critical cells in critical path p_i , $p_i \in P$
c_{ij}	a critical cell j, $c_{ij} \in C_i$
NC	a set of non-critical cells
nc_i	a non-critical cell i
B	a set of bins of a chip
B^i_{max}	a constraint for maximum number of critical cells in a bin
x^k_{ij}	a 0-1 variable represents that a critical cell c_{ij} is assigned to bin b_k
y^k_i	a 0-1 constant represents that a non-critical cell nc_i is in bin b_k
z_{ijk}	a 0-1 constant represents the connection between c_{ij} and nc_k

ILP Formulation

- Objective function

$$Minimize: \sum_{i=1}^{|P|}\sum_{j=1}^{|Ci|}\sum_{k=1}^{|B|}\sum_{l=1}^{|NC|} z_{ijl} \times (x_{ij}^{k} \times y_{l}^{k})$$



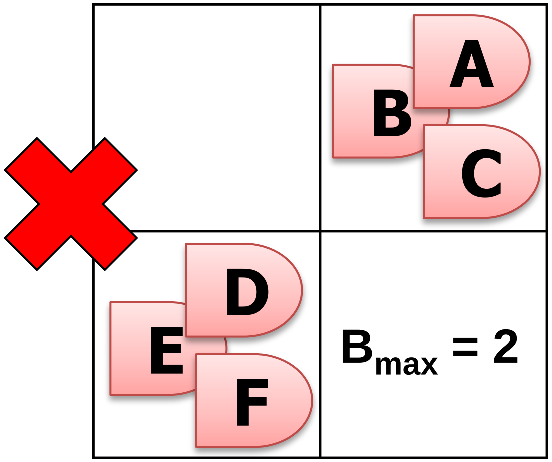
- Exclusivity constraint

$$\sum_{k=1}^{|B|} c^{k}{}_{ij} = 1, \forall c_{ij} \in C_i, p_i \in P$$

- Distribution constraint

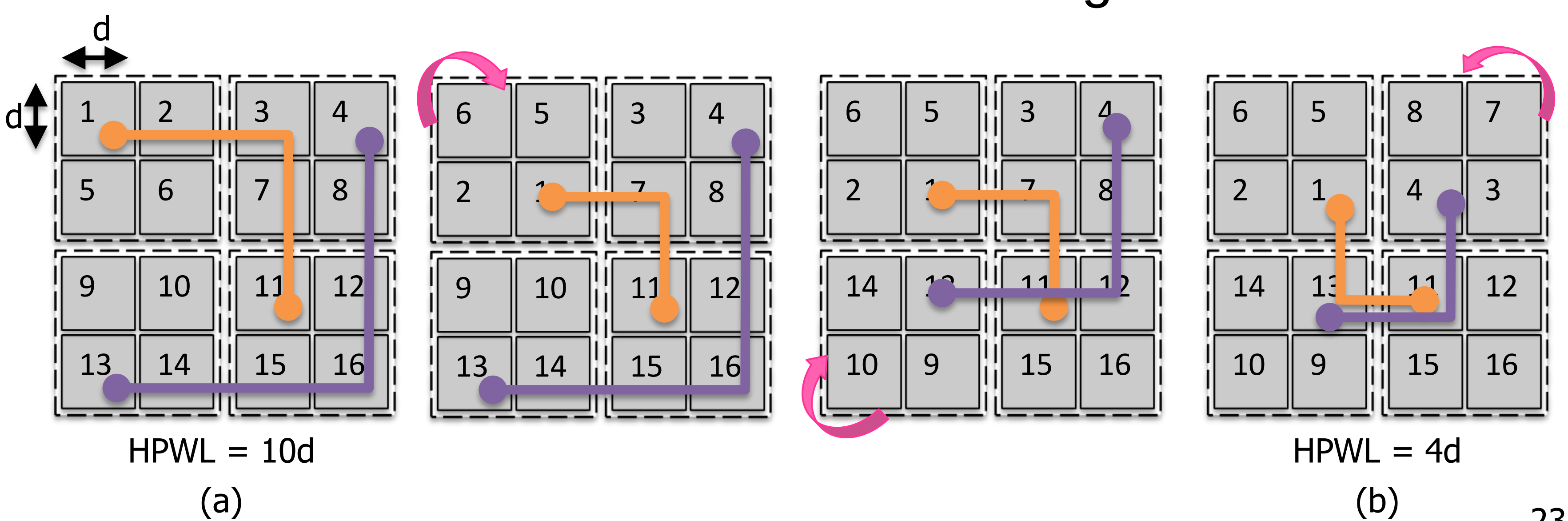
$$\sum_{j=1}^{|C_i|} c^{k}{}_{ij} < B^{i}{}_{\max}, \forall k \in B, c_{ij} \in C_i, p_i \in P$$

$$B^{i}{}_{\max} = \left\lceil \frac{|C_i|}{|B|} \right\rceil$$



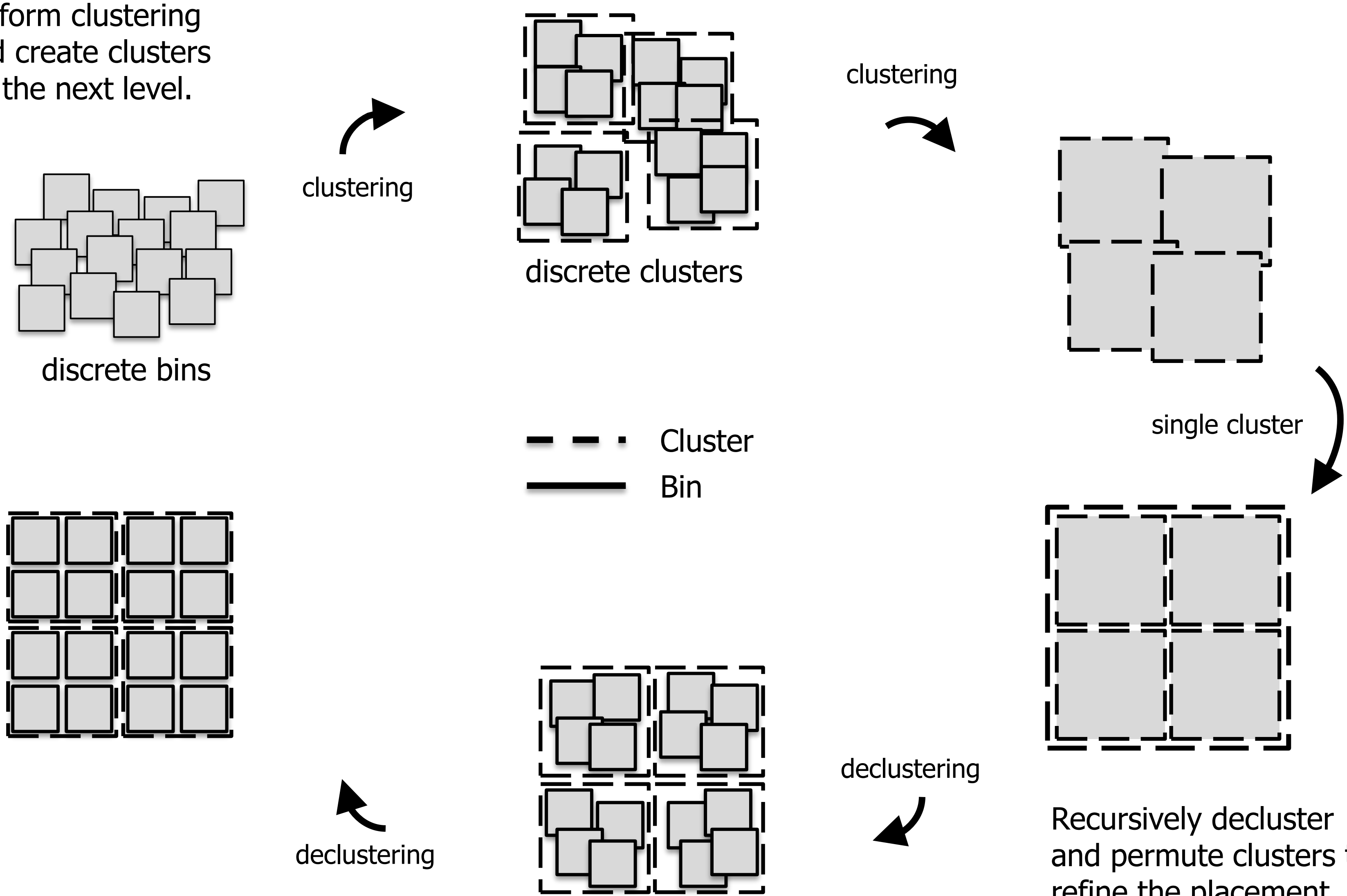
Multilevel Global Placement (1/2)

- At **clustering** stage, it will iteratively group a set of bins based on temperature and wirelength consideration
- At **declustering** stage, it will iteratively ungroup a set of clustered bins and enumerate all possible positions of all clustered bins to find the best bin placement
- Rotation methodology is applied when declustering which rotate each cluster to reduce the wirelength



Multilevel Global Placement (2/2)

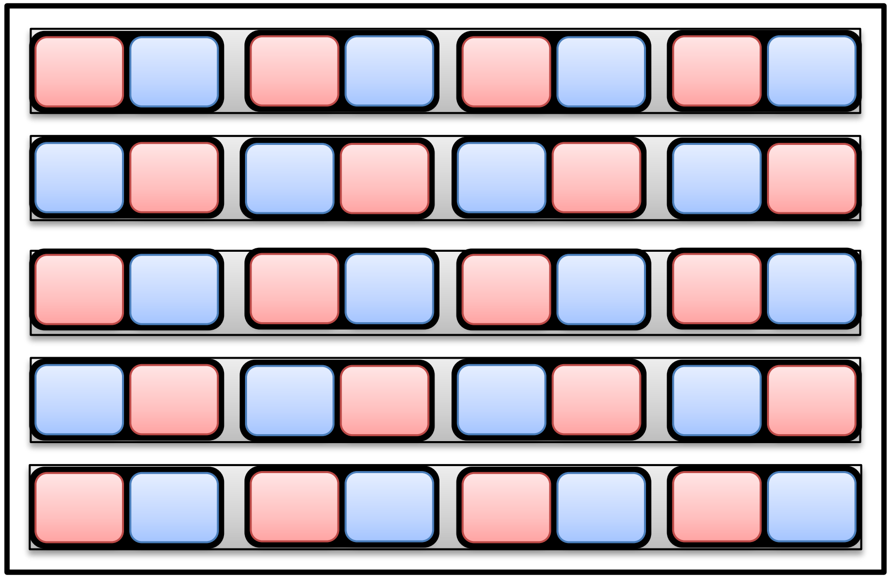
Perform clustering and create clusters for the next level.



Recursively decluster and permute clusters to refine the placement.

Row-based Detail Placement

- Partition all cells to different rows based on cell connectivity
- Cells in the same row are classified into hot cells and cool cells and group a hot cell and cool cell as a pair
- All possible pair orders inside a row and all possible row orders are enumerated



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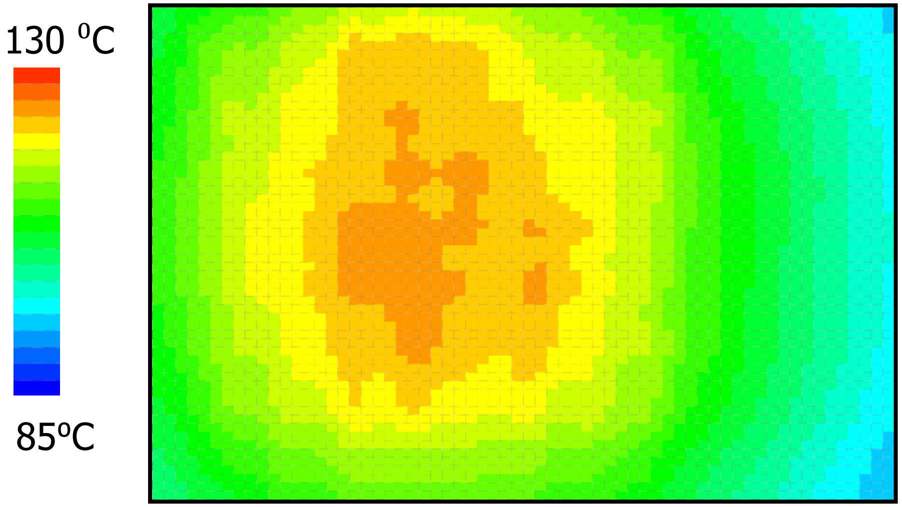
Experimental Results (1/2)

Circuit	[10]				This work			
	WL(10^8)	ICPD(%)	T_{max}(c)	Time(s)	WL(10^8)	ICPD(%)	T_{max}(c)	Time(s)
s1423	0.47	5.88	48.95	4.90	0.35	4.07	50.78	2.18
s5378	1.89	16.69	121.51	9.14	2.08	8.40	95.38	8.29
s9234	3.57	7.72	82.27	41.50	4.07	2.55	68.26	9.93
s15850	9.89	20.54	141.95	252.01	9.51	6.87	105.24	14.78
s35932	42.31	7.39	146.8	82.63	21.25	5.88	120.87	22.91
s38417	42.51	25.44	148.17	310.57	25.80	9.07	120.92	29.65
s38584	42.79	16.34	132.63	180.79	33.26	10.98	110.19	30.30
Norm.	1.30	2.14	1.21	6.45	1.00	1.00	1.00	1.00

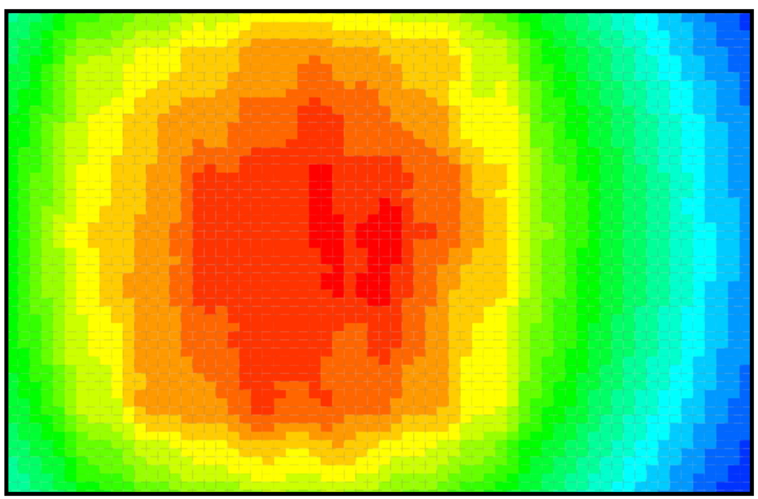
*T_{max} is the maximum chip temperature

[10] W.-H. Liu, E.-H. Ma, W.-E. Wei, and J. C.-M. Li. Placement optimization of flexible TFT digital circuits. IEEE Design Test of Computers, 28(6):24–31, November 2011.

Experimental Results (2/2)



(a) Ours



(b) [10]

Largest case : s38584

WL(10^8)	ICPD(%)	T_{max}(c)	Time(s)
33.26	10.98	110.19	30.30

WL(10^8)	ICPD(%)	T_{max}(c)	Time(s)
42.79	16.34	132.63	180.79

[10] W.-H. Liu, E.-H. Ma, W.-E. Wei, and J. C.-M. Li. Placement optimization of flexible TFT digital circuits. IEEE Design Test of Computers, 28(6):24–31, November 2011.

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Conclusion

- In this paper :
  - The impact of temperature on mobility variation have been demonstrated and derive new problem formulation for flexible TFT
  - A novel cell placement flow and algorithms to minimize the mobility variation caused by the change of both mechanical strain and temperature while minimizing total wirelength is proposed
  - Experimental results have demonstrated that the proposed algorithms can reduce the ICPD without routing overhead


Thank You!