# Manycore Processor for Video Mining Applications



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- Next-Gen Embedded Systems : Requires more performance(100's GOPS~ 1 POPS)
- Power Consumption : Already reached upper limit (~W)



<Expectations on Many-Core>

Ref: NDEO Technology Roadmap 2009, I-48p, Fig. 1-6

Energy-Efficient Computing goes to Heterogeneous & Manycore

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## **SMYLEvideo:** Application Domain Specific **TOPS:** Heterogeneous Manycore for Computer Vision

"ML and 3D Object Recognition on Image Stream"

Computer Vision (CW) = EYE (sensor) + CEREBRUM (decision)



- Conceptually: Machine Learning (ML) ≒ Functional Configuration
- High Perf. Requirement: More than 1 TOPS
- Inherent Parallelism: More than 99% of processing
- Several types of Proc.: Huge cost with Hardwires Implementation
  - Resolutions: VGA, XGA, SGGA, FHD, 2K, 4K, etc.
  - Algorithms: SIFT, Optical Flow, Ransac, Viola & Jones, Model based Recognitions, etc.

Multi-Medium Streams (MPEG-2, MPEG-4, H.264, etc.)

Key requirement is High Performance with Flexibility

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> Others:

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# What is Video Mining System





# Parallelisms in Algorithms for Video Mining

Application	Objective	Algorithm	Parallel	ism
Video Analysis	Prediction of Motion Vector	Optical Flow	Line	
	Specific feature detection and extraction	SIFT <sup>*1</sup>	Data Partitioning	
	Detection of human, and tracking	Cascaded Haar Like	Pixel Level	
	Line detection for field separation	Huff	Line	
	Elimination of error from continuous frames	Ransac <sup>*2</sup>	Sample Data	00
Human Search	Face detection from several angles	Vector Face Detection	Pixel Blocks	
	Extraction of features on faces	Model Based Face Detection	Task Level	$\overset{\sim}{\sim}$
	Specific feature detection and extraction	SIFT	Data Partitioning	
Video Editing	Segment Extraction	Graph based Segmentation	Grid Level	
	Detection of Motion Vector	Block Matching	Line	

\*1 SIFT: Scale-Invariant Feature Transform

\*2 Ransac Random Sample Consensus

Many type of pallarelisms are inherent in algorithms for Video Mining



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- Real-Time Processing : 1TOPS~
- Scalability :
- Programmability :
- Flexibility :

- 10fps, 20fps, 30fps
- **Software Based Implementation** 
  - **OpenCV (Computer Vision)**
  - SIFT, Optical Flow, Ransac, Viola & Jones, Model based Recognitions, SVM, etc.
- Low Power : ~1.5W
- Low Clock Frequency : ~100MHz





# System Level Architecture of SMYLEvideo

Local Memory

Stream

IN

**Data Parallel** 

**Data Paralle** (SIMD)

time

Core can keep

**Processing of** 

Kernel

Stream

OUT

Kernel

Stream

OUT

#### **Distributed Processing with KPN** Local Memory **Non-Shared Memory Processes** Zero-Overhead Message Passing Mechanism Kahn Process Network **Combination of Parallelisms** Distributed Parallel Processing (Task, Pipeline) Task-A Data Parallelism (High-Level, Instruction Level) Task Parallel Task-B **Stream Processing (Core)** Task-C Kernel Task-D Stream-In (Read Message) **Combination of Data & Task Parallel** Stream-Out (Write Message) Stream Stream Stream IN. IN IN **Optimization of Core** Support Stream Processing : background Stream Kernel Kernel Kernel Complex Inst : Reduction of Kernel cycle \_ **FIFO** support mechanism \_ Stream Stream Reduction of energy for instruction / data supply OUT OUT Distributed Processing, ZOMP, Task Parallel, Stream Processing, ASIP TOPS Systems Corp. www.topscom.co.jp



# **SMYLEvideo : Basic Architecture**





# Partitioning **OpenCL vs. Distributed Processing**

- **OpenCL** (CPU centric) \*
  - **Bottleneck** 
    - Processing on Host  $\geq$
    - Increasing communication with Host

- \*\* **Distributed Processing** 
  - **Scalability**
  - Can combine with Data Parallel Processing





## **Software Partitioning** Sequential to Distributed Processing



Investigation has done on Many Algorithms ; Viola & Jones, SVM, SIFT, etc. TOPS Systems Corp. www.topscom.co.jp



# Approach for Energy-Efficient Computing

- Goal : High-Performance & Low-Power Programmable Accelerator (Energy-Efficient, Low Cost, Flexible, Scalable)
- Approach : Low Clock Frequency



#### High Performance @ Low Clock Frequency drives Low Power TOPS Systems Corp. www.topscom.co.jp



# Approach to reduce clock frequency with Architecture-Algorithm Co-Design





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# **Stream Processing Core**

MPSoC'10

### Hide overhead of Stream-In and Stream-Out





### Inter-Core FIFO : Register Bank Sharing MPSoC'10

Reduction of Memory Access Bandwidth and its Energy





# **Reduction of memory traffic**

### Path for Message Passing



Significant Reduction of Memory Trafifc : more than 30% TOPS Systems Corp. www.topscom.co.jp

## ZOMP TOPS Zero-Overhead Message Passing Mechanism

 Remove cycles and memory access for checking FIFO counts and synchronization



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# Memory Access reduction by Distributed Stream Processing

- Memory Centric Processing
  - Each core works data on External Memory
  - Integration of processors and memories
- Distributed Stream Processing
  - Core to Core Stream passing
    - On-Chip memory
    - Register Sharing





# Frame based vs. Block based Processing



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# Frame based vs. Block based Processing

	Frame based Processing	Block based Processing	
Global Memory Usage	22Mbytes	3.1Mbytes	
Cluster Local Memory Usage	0.15Mbytes	0.8Mbytes	
Recognition Latency	167mSec(5.1frame)	100mSec(3frame)	





Memory Usage : 1/7, Memory Bandwidth Requirement : 1/5TOPS Systems Corp.www.topscom.co.jp



# **SMYLEvideo Configuration**





- Manycore will play a crucial role in extending the roadmap for enabling the next generation SoCs required for "Video Mining" one of Computer Vision systems.
- Zero-Overhead Message Passing Mechanism (ZOMP) can efficiently increases the system performance and scalability of Manycore processors.
- Block based distributed processing drastically reduces memory access bandwidth and increases room for higher performance on Manycore processors.
- SMYLEvideo provides scalability in performance and functionality with its clustered architecture.



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