An Adaptive Current-Threshold Determination for IDDQ Testing Based on Bayesian Process Parameter Estimation

Michihiro Shintani and Takashi Sato

Kyoto University, Japan

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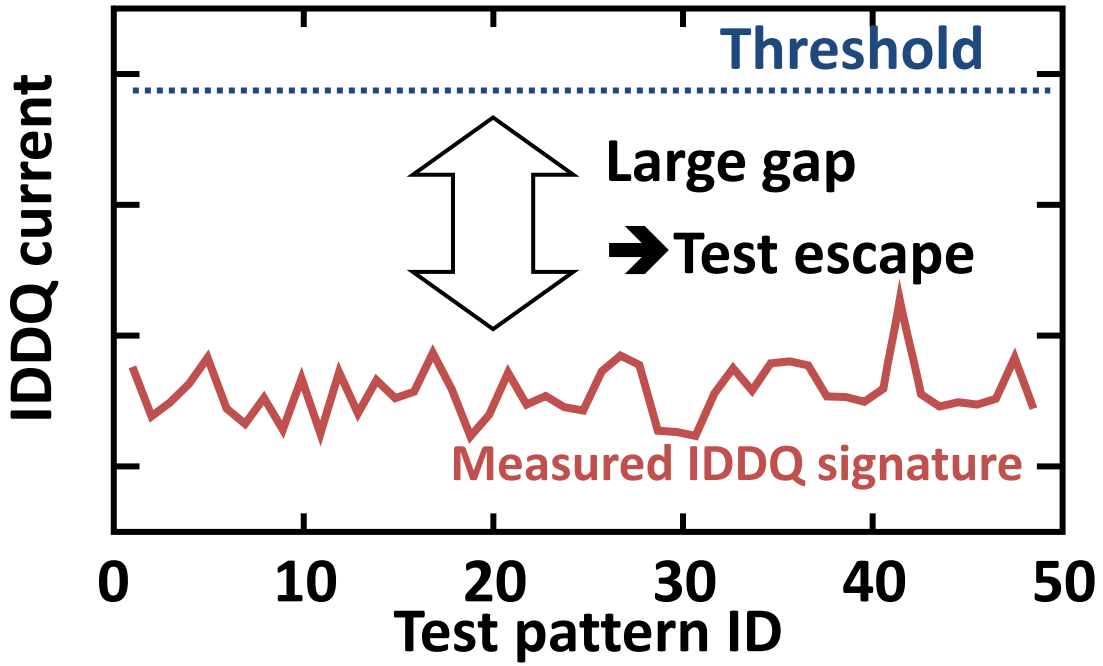
Contents

- Background and objective
- IDDQ testing pass/fail threshold determination
  - Two concepts
  - Four steps for realization
- Experimental results
- Conclusion

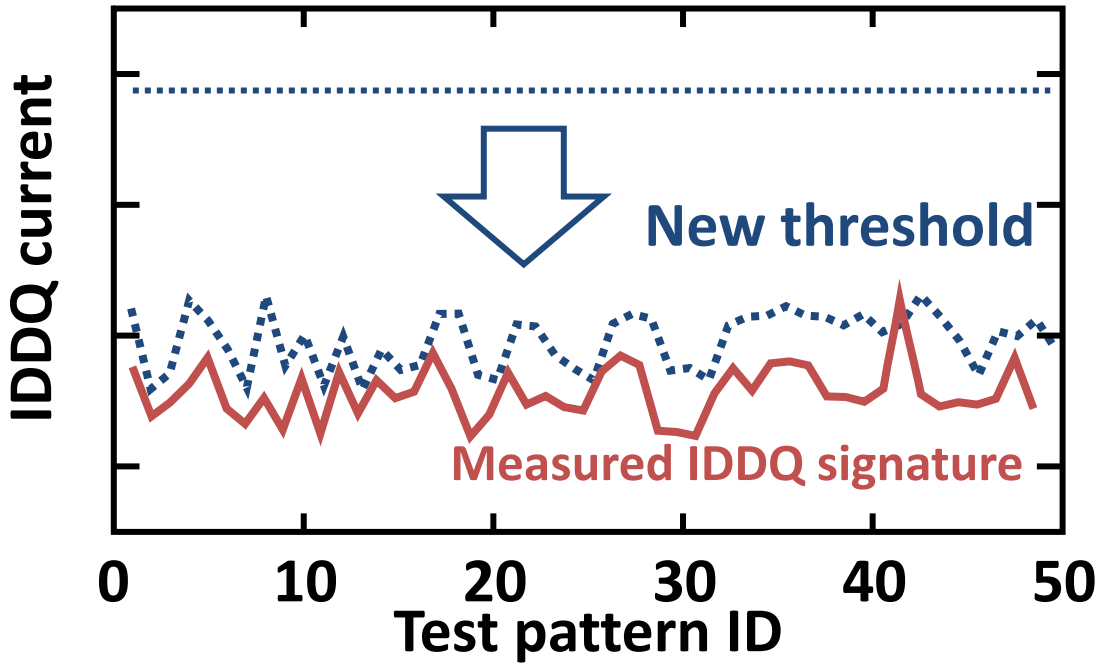
IDDQ testing in advanced process

- Increasing relative process variation
- Setting pass/fail threshold for IDDQ testing has become difficult
  - Inappropriate threshold results in yield loss and test escape



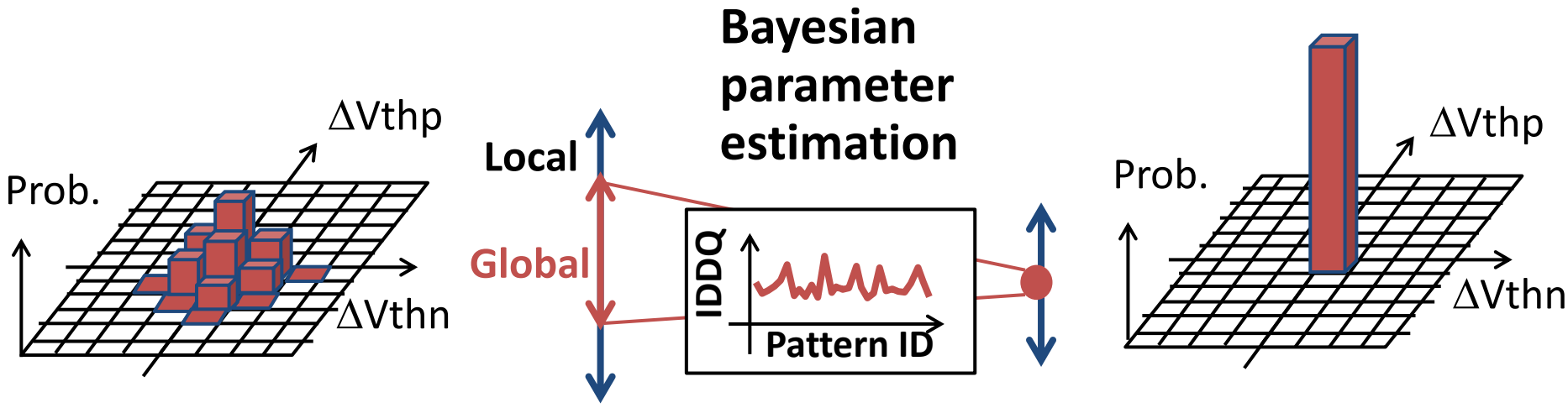
Objective of our work

- Propose a novel IDDQ threshold determination
- Obtain per-chip, tighter pass/fail thresholds for more accurate IDDQ testing
- Achieve low yield loss and test escape

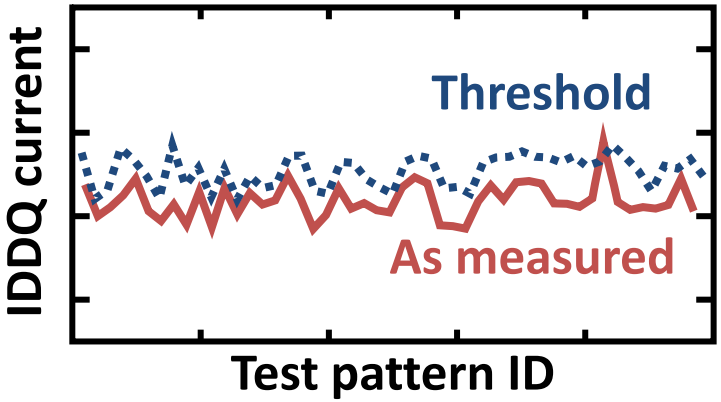


Key concept 1: two stage approach

1) Estimate global parameter of a chip using IDDQ signature based on Bayes' theorem[Shintani, VTS'12]



2) Determine thresholds for each chip based on the estimated global parameters



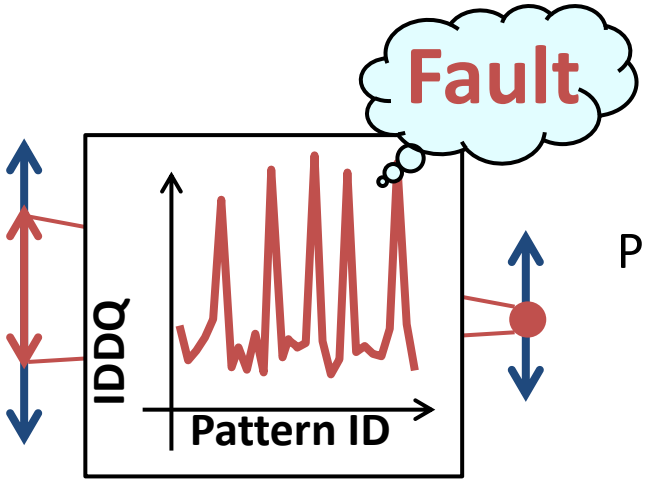
Issue of key concept 1

- When a chip has faults…,

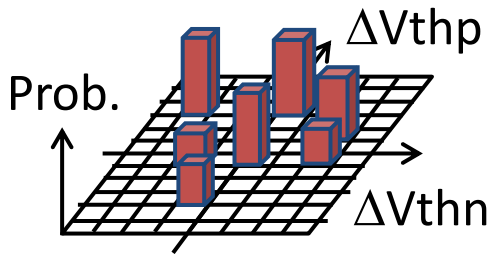
➔Global parameter estimation will be degraded

➔Also current-threshold determination will be degraded

Parameter estimation by using faulty signature

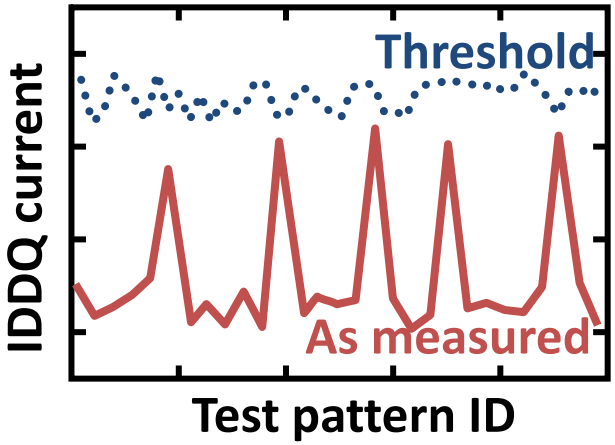


Wrong parameter estimation



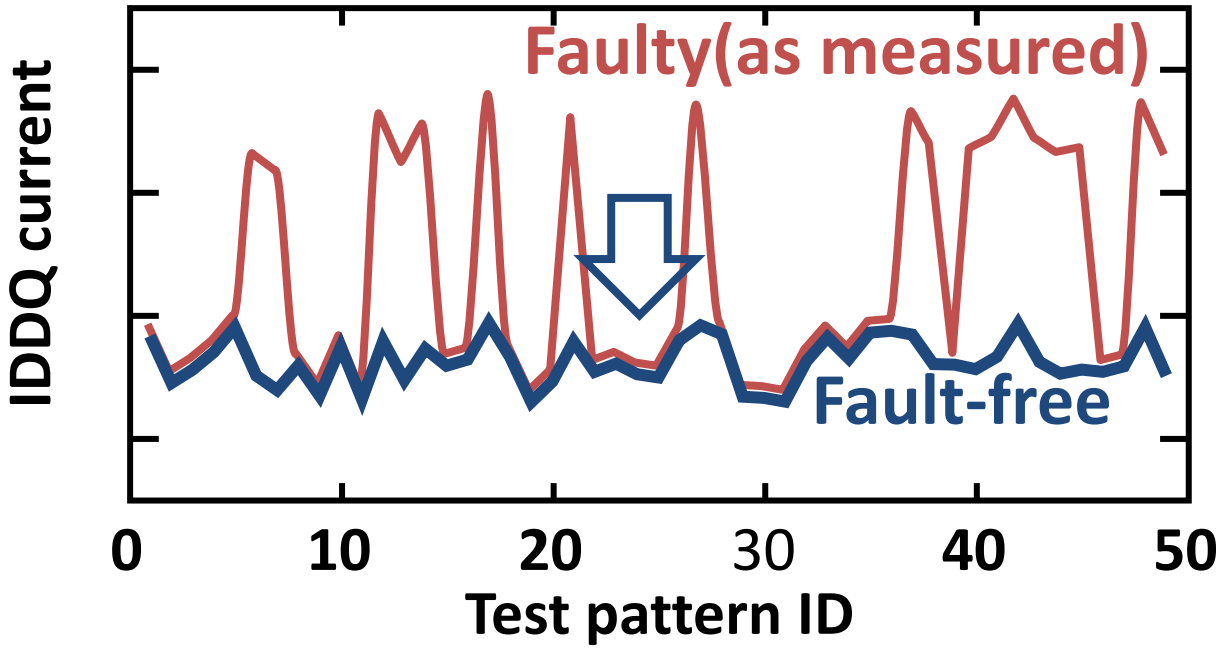
Wrong threshold determination

➔***Yield loss*** and ***test escape***



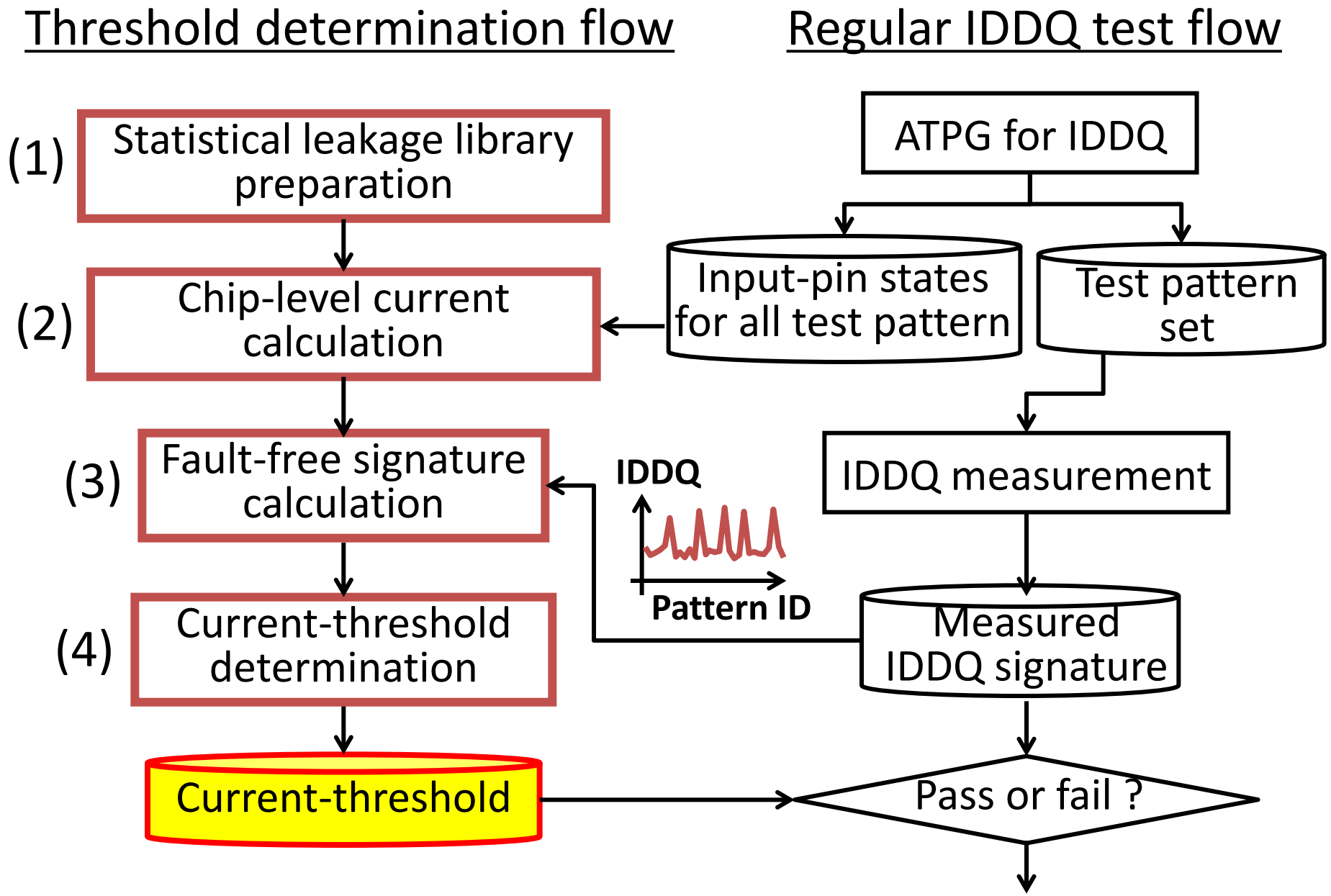
Key concept 2: fault-free signature calculation

- For the accurate threshold determination, calculate a FF (fault-free) signature through **simulated annealing**



- Then, estimate global parameter using the FF signature

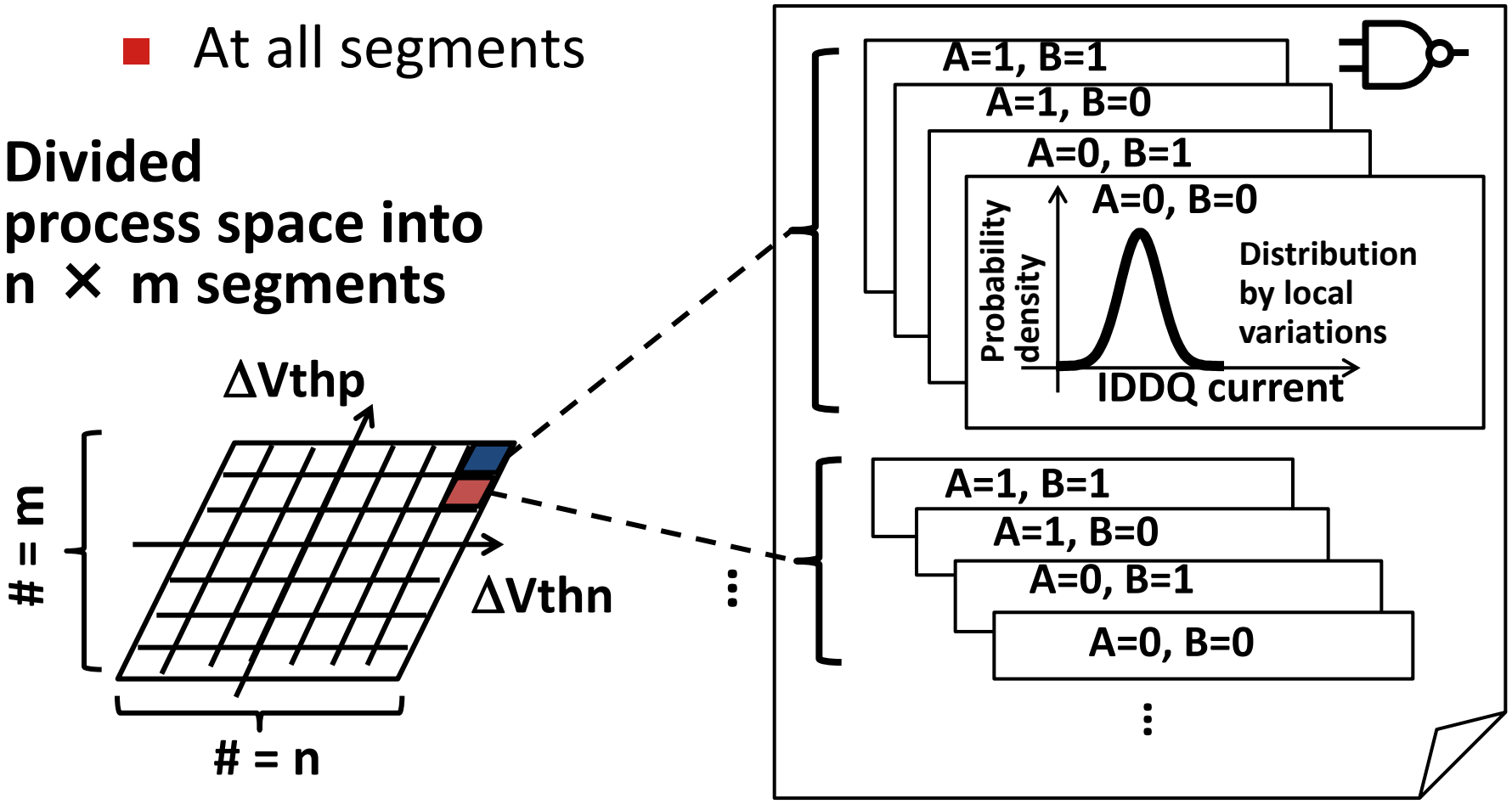
Proposed flow



(1) Statistical leakage library preparation

- Calculate statistical leakage distribution
  - For all standard cells
  - For all input states
  - At all segments

Divided process space into n × m segments

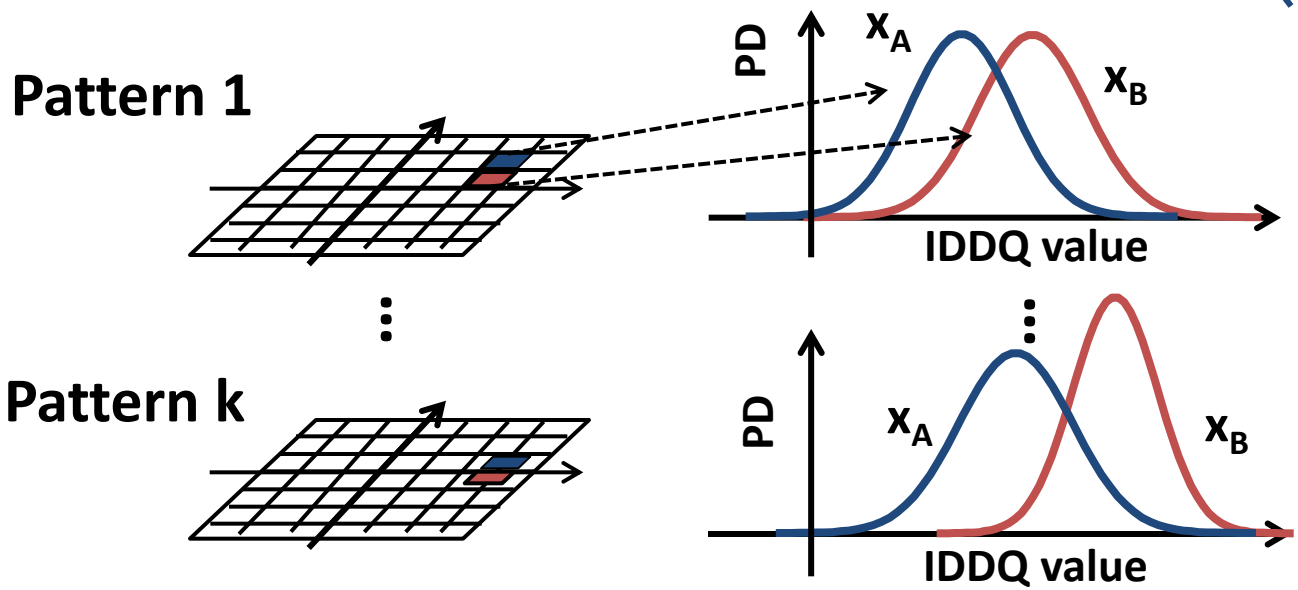


(2) Chip-level current calculation

- Calculate statistical leakage distribution of total leakage using the leakage library
  - For all test patterns
  - At all segments
- Chip-level leakage = $\sum$ (leakage of cells)

Statistical leakage lib.

Input-pin states for all test pattern



(3) Fault-free signature calculation (1/2)[10]

- Calculate Fault-sensitization vector (FSV) and a fault size in simulated annealing
  - Element of FSV = [0 (if non-sensitized)
    1 (if sensitized)

  - Fault size = $IDDQ_{Ave\_FSV=1}$ − $IDDQ_{Ave\_FSV=0}$

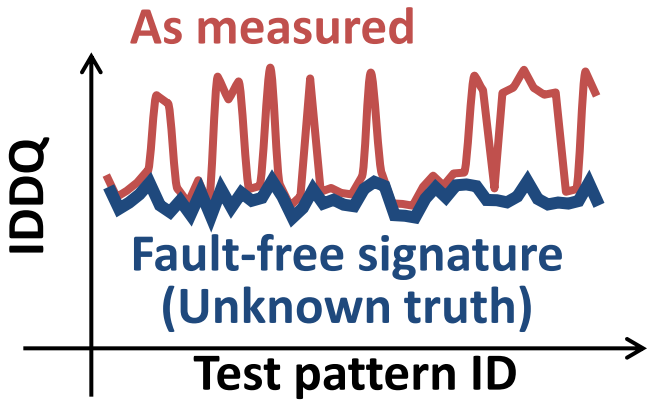
➔ FF current = measured IDDQ current – fault size

(3) Fault-free signature calculation (2/2)

- In simulated annealing:
  1) Generate FSV randomly and calculate FF signature
  2) Estimate global parameter using the FF signature through Bayesian parameter estimation
  3) Evaluate cost function: convergence of estimation

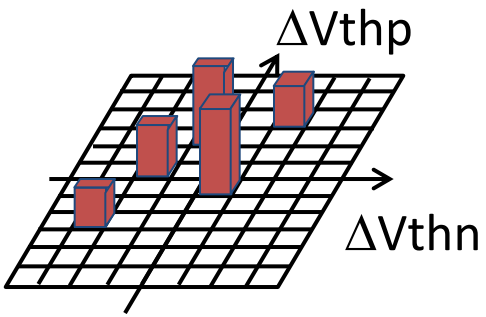
FSV

```
0 0 0 0 0 0 1 0 1 1 1 1 0 1
0 0 0 0 0 0 1 0 1 1 0 1 0 0
0 0 0 0 0 0 1 0 0 1 0 1 0 0
...
```



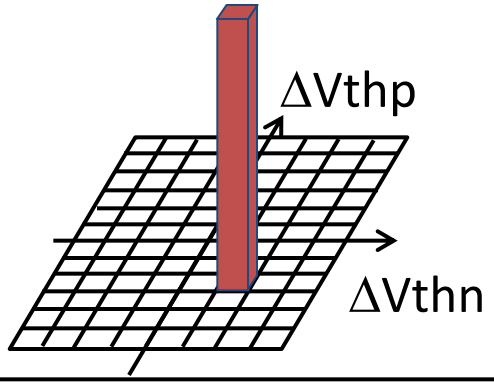
When FSV is wrong

The estimation fails to converge



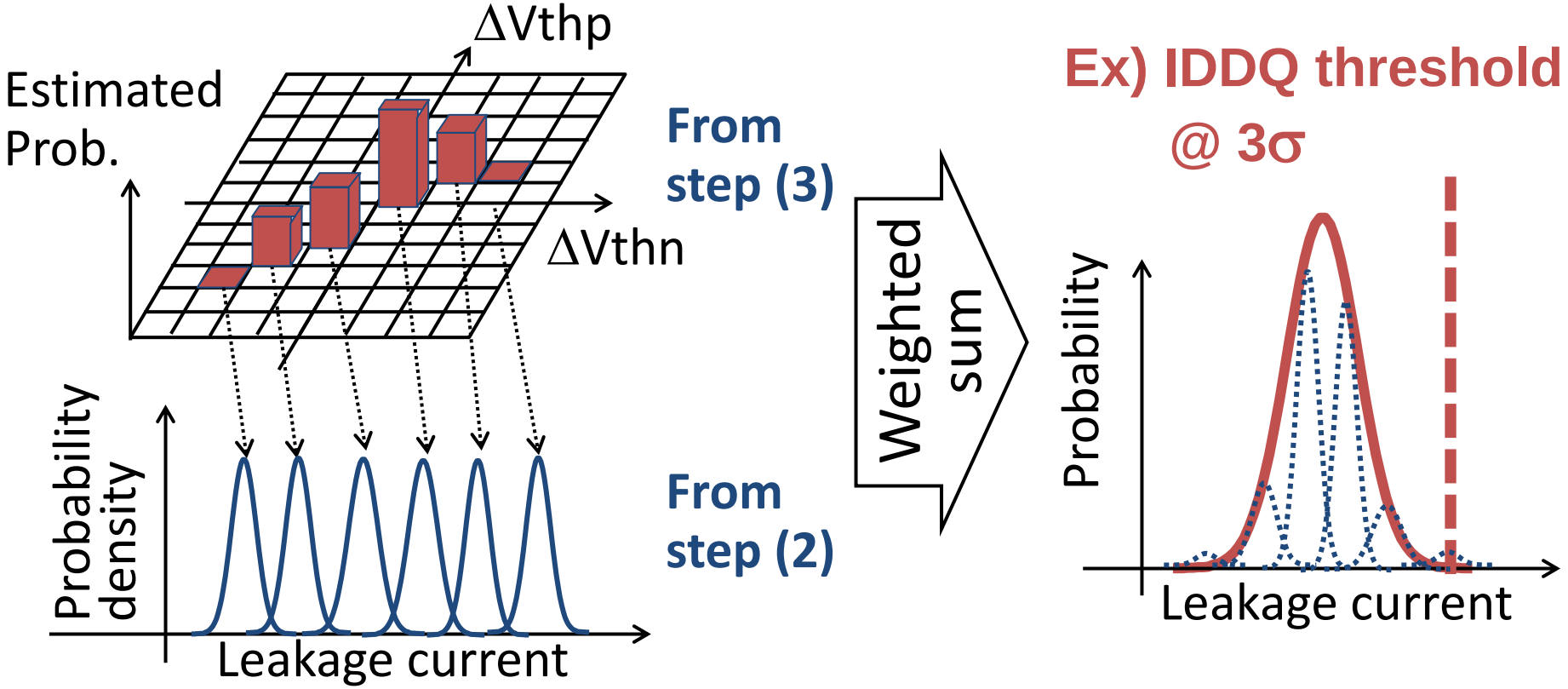
When FSV is correct

The estimation converges quickly



(4) Current-threshold determination

- Calculate statistical leakage current distribution considering global and local variations by a weighted sum
- Determine current-threshold



Simulation setup (1/3)

- On an assumed virtual wafer, evaluate test accuracy with changing pass/fail threshold from 1σ to 9σ

- Analyze
  - Yield loss and test escape
  - Result of fault-free signature calculation
  - Relationship between current-threshold and measured IDDQ signature
  - Detected leakage fault size

Simulation setup (2/3)

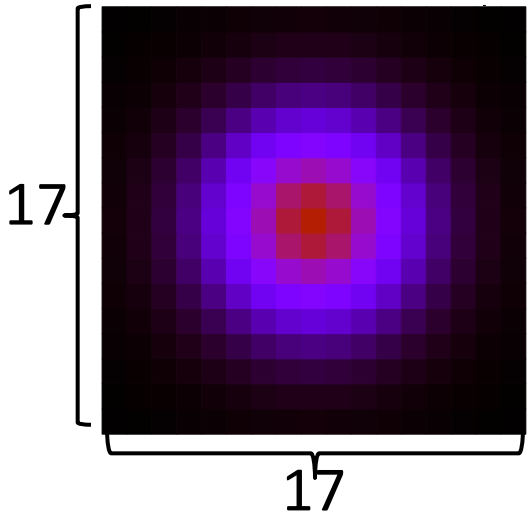
- Target circuit
  - ISCAS'89 benchmark circuit: s38584
  - Test pattern set
    - Pseudo stuck-at model
    - # of test patterns: 49
    - Test coverage: 100%
- Library set
  - 65nm commercial library
  - Global & local variation
    - Threshold voltages of pMOS and nMOS

    ΔVthn, ΔVthp

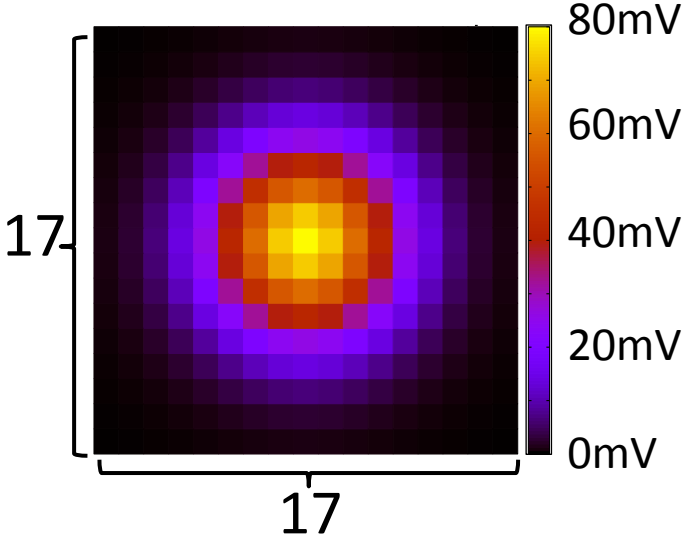
Simulation setup (3/3)

- 17x17(=289) chips on the wafer
- Yield 80%: 231 good chips, 58 bad chips
  - Single stuck-at fault is randomly inserted
  - Leakage fault size (μA) follows: $0.6 \exp(-0.6\lambda)$
- Distributions on the wafer

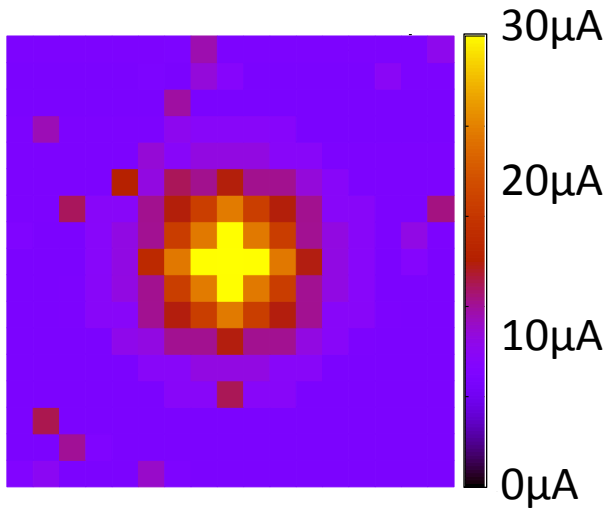
ΔVthn



ΔVthp

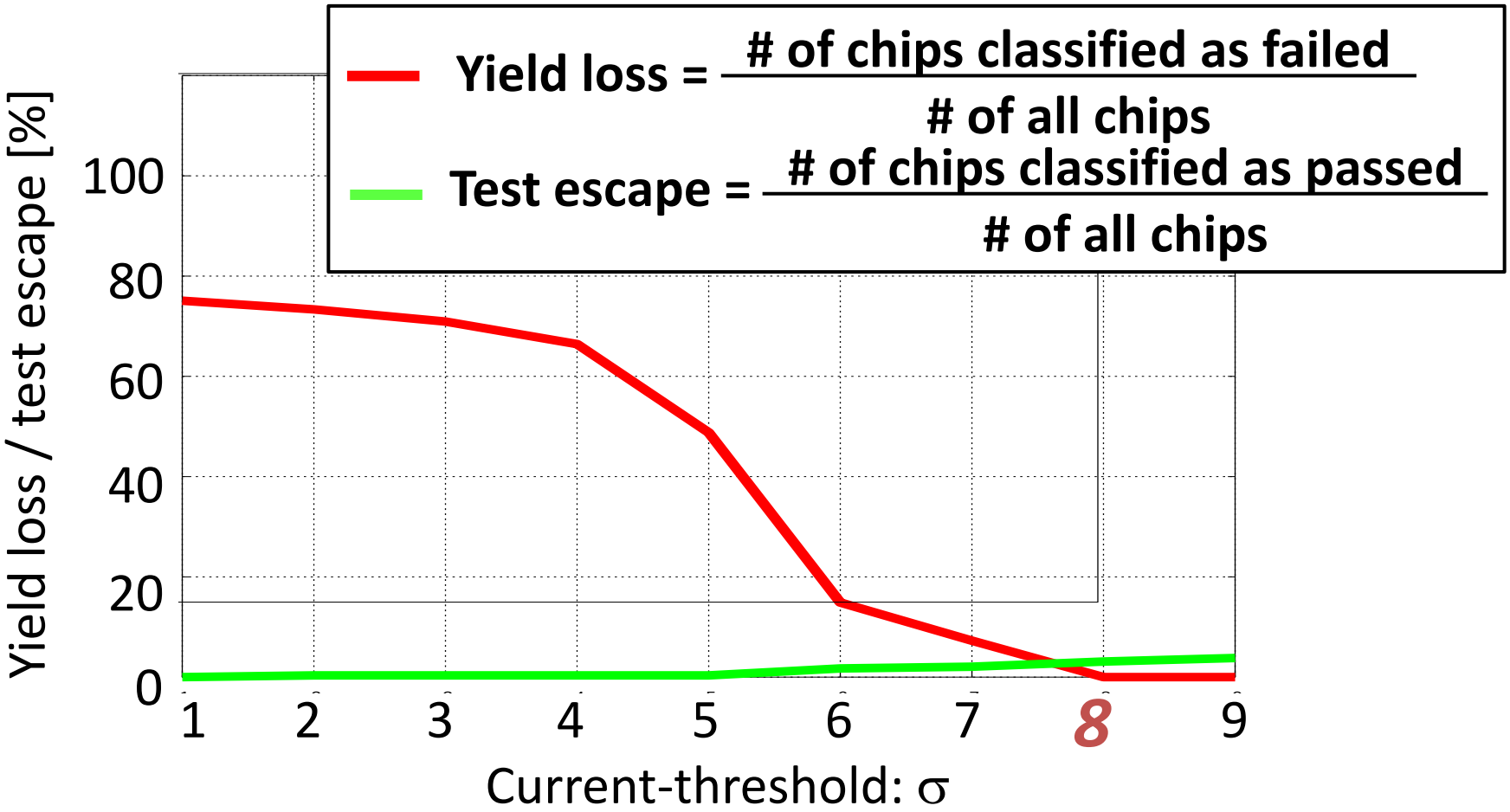


IDDQ currents distribution for 1st test pattern



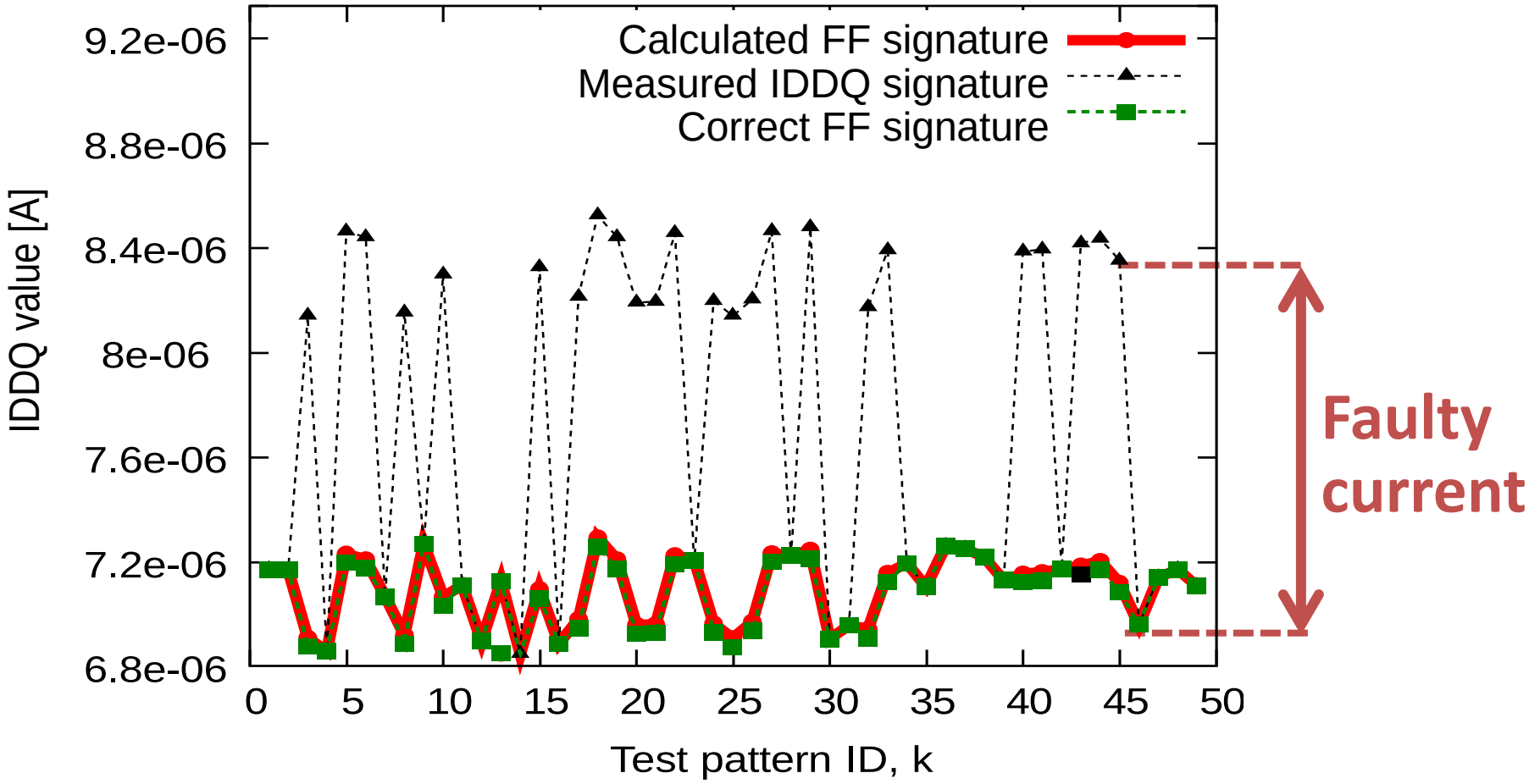
Result of test accuracy

- Best performance is achieved at **8σ**
  - Lowest yield loss and test escape
  - Yield loss: **0%**, test escape: **3%**



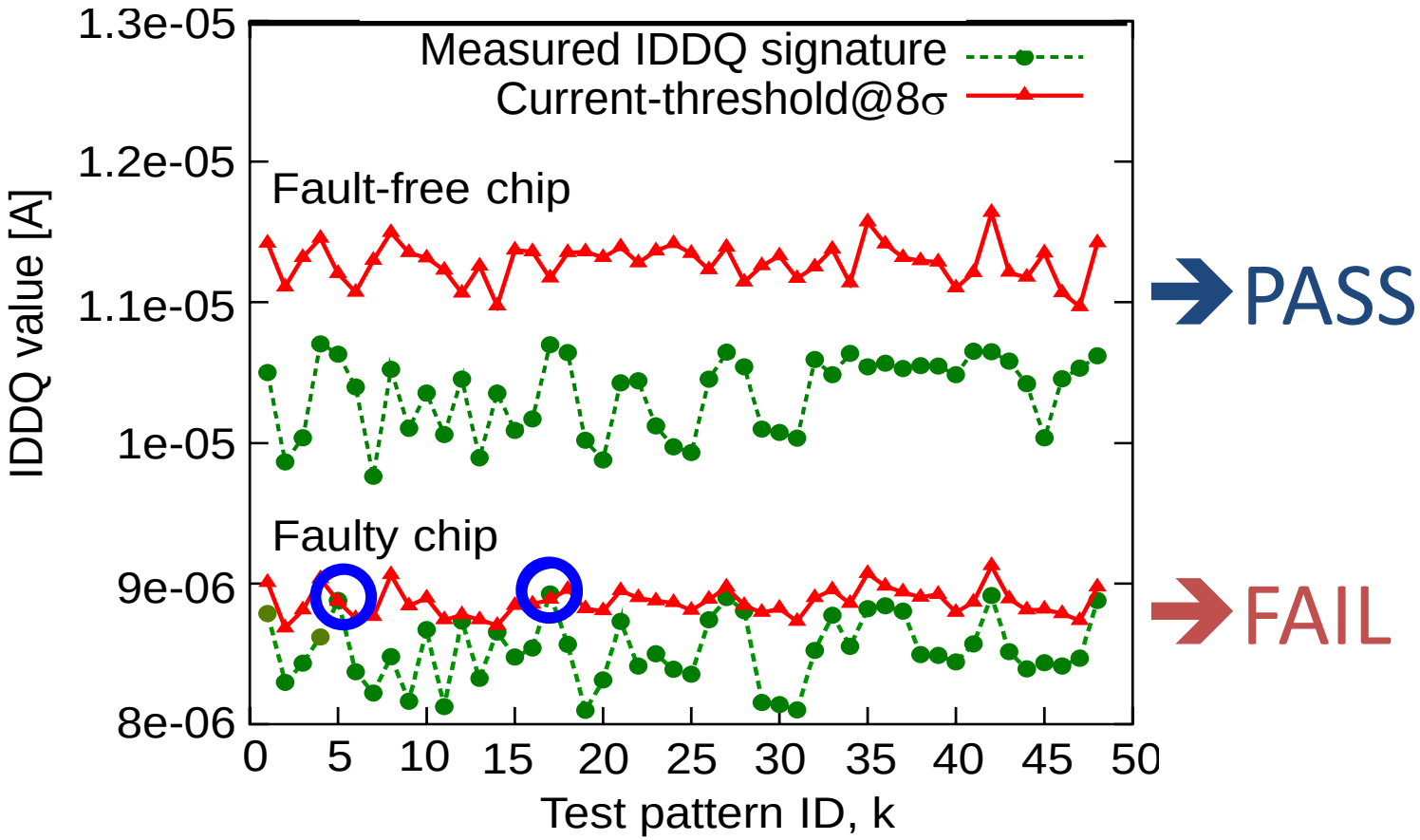
Example of fault-free signature calculation

- Faults are completely identified
- Completely coincident with correct FF signature



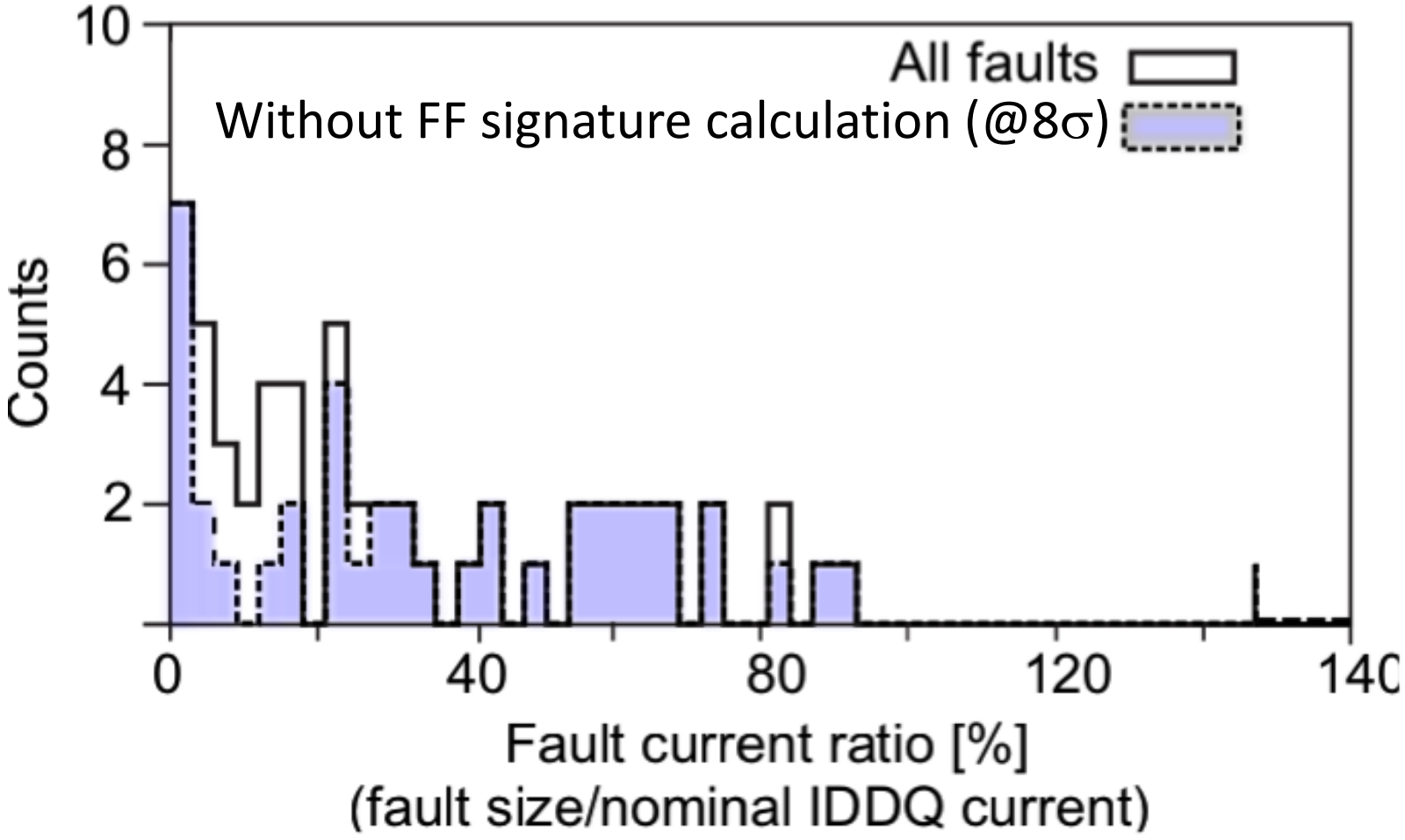
Examples of current-threshold

- Chips are successfully classified
- Our technique can applicable to the case:
  - Fault-free > faulty



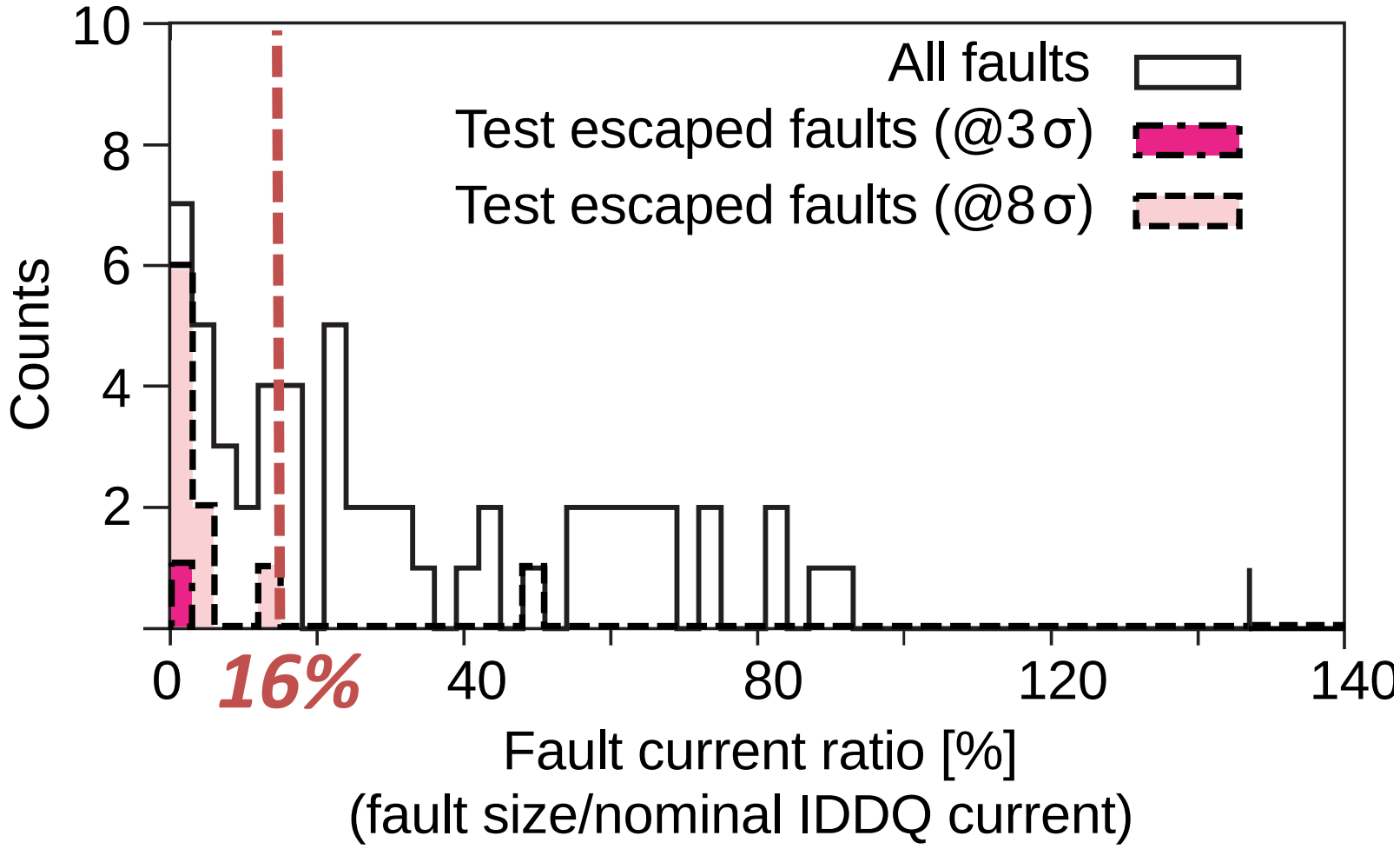
Histogram of escaped size w/o FF signature

- Without fault-free signature calculation, almost all faults can not be detected



Histogram of escaped size with FF signature

- Detect faults whose size, down to **16%** of the nominal IDDQ current



Conclusion

- Propose a novel IDDQ testing pass/fail threshold determination
  - Based on Bayesian global parameter estimation using IDDQ signature
  - Calculate fault-free signature
- Experimental results show:
  - Calculate the fault-free signature correctly
  - Achieve best performance at 8σ
    - Yield loss: 0%, test escape: 3%
  - Detect small leakage defect
    - 16% of nominal leakage at 8σ

- Thank you for your attention