Block-level Designs of Die-to-Wafer Bonded 3D ICs and Their Design Quality Tradeoffs

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Near Future 3D ICs

• Wafer-to-wafer bonding is a low cost process, but it requires that all dies have the same size

• In several cases, die-to-wafer bonding is more practical than wafer-to-wafer bonding and still low-cost
  – Memory + logic stacking
  – Logic-to-logic stacking when dies are from different companies
  – Designs with IP blocks that enforce different size of dies in the stack

• In near future, block-level designs are likely to be early 3D ICs on the market because the methodology allows the reuse of optimized IP blocks
TSV position is an important design factor that limits the quality of 3D ICs in terms of:
- Performance: area, wirelength, delay, and power
- Reliability: temperature and mechanical stress

No previous work has studied the quality trade-offs between different styles of block-level layout of die-to-wafer bonded 3D ICs in a holistic manner.
Problem Statement (I)

• A 2-tier 3D IC is focused in this work

• Both dies are facing down
  – Compatibility with popular flip-chip packaging
  – Heat sink attached on back side of the top die for good cooling

• Bottom die has larger footprint than top die
  – Large area available for C4 bumps for good power delivery
• Redistribution layer (RDL)
  – Necessary if some TSVs in bottom die are outside the footprint of top die
  – Not needed if all TSVs in bottom die are inside the footprint of the top die
• Layout of the top die is fixed

• Study three different design styles of the bottom die
  – TSV-farm: dense array of TSVs in the middle of bottom die (no need for RDL)
  – TSV-distributed: arrays of TSVs distributed across bottom die
  – TSV-whitespace: TSVs inserted in whitespace nearby connecting pins
Design Flow

• **Partitioning:**
  – Use same partition in all design styles for fair comparison

• **Floorplanning:**
  – Preplace TSVs (TSV-farm and TSV-distributed)
  – Postplace TSVs (TSV-whitespace)

• **Timing optimization:**
  – Set timing constraints of each die according to [Y.-J. Lee, 3DIC 2010]
  – Insert buffers to meet the constraints of each die separately

• **Routing**
  – Routing on each die
  – RDL routing (TSV-distributed and TSV-whitespace)
• Area and wirelength are directly obtained from the layout of both bottom and top dies
• Delay and power are analyzed using the following flow:

Diagram:
- Top-Die DEF/GDSII
- Bottom-Die DEF/GDSII
- SoC Encounter
- Top-Level Verilog
- Bottom-Die Verilog
- Design Switching Activity
- Top-Die Parasitic RC
- Bottom-Die Parasitic RC
- Top-Level TSV RC
- PrimeTime PX
- Timing and Power of 3D ICs
• Temperature is analyzed using the following flow:
Evaluation – Reliability Metrics
Temperature (II)

- Adhesive
- Bulk Si (30 μm)
- STI
- Active
- Poly
- M1
- TSV M1 Landing Pad
- M5

Thermal Cell Width

- TSV (5 μm)

Device Contact = 5.56%
Poly = 8.33%
TSV = 11.11%
Dielectric = 75%
Baseline TSV stress model from FEA simulation

- Model realistic TSV structures: TSV, liner, landing pad
- Obtain stress tensor from simulation result
- Convert to Cartesian coordinate

\[ S_{xyz} = \begin{bmatrix}
\cos \theta & -\sin \theta & 0 \\
\sin \theta & \cos \theta & 0 \\
0 & 0 & 1 \\
\end{bmatrix} \begin{bmatrix}
\sigma_{rr} & \sigma_{r\theta} & \sigma_{rz} \\
\sigma_{\theta r} & \sigma_{\theta\theta} & \sigma_{\theta z} \\
\sigma_{z r} & \sigma_{z\theta} & \sigma_{zz} \\
\end{bmatrix} \begin{bmatrix}
\cos \theta & \sin \theta & 0 \\
-\sin \theta & \cos \theta & 0 \\
0 & 0 & 1 \\
\end{bmatrix} \]

Stress tensor from FEA simulation
Full-chip stress and reliability analysis using linear superposition

- TSV1, TSV2, and TSV3 affect P
- TSV4 doesn’t affect P
• A reconfigurable computing array obtained from OpenCores

<table>
<thead>
<tr>
<th></th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total #gates</td>
<td>1,363,536</td>
</tr>
<tr>
<td>#Interblock nets</td>
<td>1,853</td>
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<tr>
<td>#TSVs</td>
<td>312</td>
</tr>
<tr>
<td>Total #blocks</td>
<td>95</td>
</tr>
<tr>
<td>#Blocks on top die</td>
<td>26</td>
</tr>
<tr>
<td>#Blocks on bottom die</td>
<td>69</td>
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</tbody>
</table>
Experiments

- **Baseline designs**
  - TSV size: 10 μm
  - TSV pitch: 30 μm

- **Small TSV (Small TSV size)**
  - TSV size: 5 μm
  - TSV pitch: 30 μm

- **Dense TSV (Small TSV size + narrow TSV pitch)**
  - TSV size: 5 μm
  - TSV pitch: 15 μm
Baseline – Layout in TSV-farm Style

Bottom Die

Top Die

- TSV Farm
- Bonding Pads (Top Metal)
Baseline – Layout in TSV-distributed Style

**Bottom Die**

- A TSV Array

**RDL**

- Bonding Pads (to top die)
- Bonding Pads (to bottom die)
Baseline – Layout in TSV-whitespace Style

Most TSVs are in whitespace
Baseline – Wirelength, Delay, and Buffers

Distributed TSV arrays interfere floorplan

RDL = extra wirelength

Extra buffers are needed

Still slow
Baseline – Power, Temperature, and Stress

Slow = Low power

Distributed TSV arrays help reduce max temp.

High stress in small area
Baseline – Temperature Map of Bottom Die

- TSV-farm
  - Hot spot far from TSV farm

- TSV-distributed
  - Only few TSVs nearby hot spot

- TSV-whitespace
Baseline – Stress Map of Bottom Die

TSV-farm

TSV-distributed

TSV-whitespace

Zoom up these areas

TSV stress impacts area nearby the TSV
Baseline – Stress Map of Bottom Die (Zoom-up)

- **TSV-farm**: Stress from nearby TSVs adds up.
- **TSV-distributed**: Areas impacted by TSV stress do not overlap much.
Small TSV – Wirelength, Delay, and Buffers

- Same WL
- Little faster (smaller TSV RC)
- About same # buffers

Bar chart showing wirelength (WL), delay, and buffer comparisons between Base and Small TSV types.
Small TSV – Power, Temperature, and Stress

Possible to narrow TSV pitch & footprint
Smaller area under stress impact
Little more power  Same temp.  Much lower stress
Dense TSV – Wirelength, Delay, and Buffers

**Little shorter WL**

**Litter faster**

**Lower # buffers**

Bar chart showing comparison of B2B WL, RDL WL, LPD (Opt), and # Buffers for different TSV configurations (farm, dist, white) in Base, Small, and Dense scenarios.
Dense TSV – Power and Temperature

- Little more power
- About same temp.
### Dense TSV – Stress

Stress is back to original values in even smaller area under stress impact.

<table>
<thead>
<tr>
<th>TSV-farm</th>
<th>TSV-dist</th>
<th>TSV-white</th>
<th>TSV-farm</th>
<th>TSV-dist</th>
<th>TSV-white</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base</td>
<td>Base</td>
<td>Base</td>
<td>Base</td>
<td>Base</td>
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</tr>
<tr>
<td>Small</td>
<td>Small</td>
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<tr>
<td>Dense</td>
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- **Ave S (s>10)**
- **Area (s>10)**
• A circuit is manually designed in three different styles to study trade-offs of the quality of the layouts

• TSV-farm style
  – Shortest wirelength and best timing
  – Highest average stress, but smallest impacted area

• TSV-distributed style
  – Longest wirelength (TSVs interfere placement)
  – Lowest temperature (TSVs help reduce temperature)
Thank you

Questions?