Stacked Signal TSV for Thermal Dissipation in Global Routing for 3D IC

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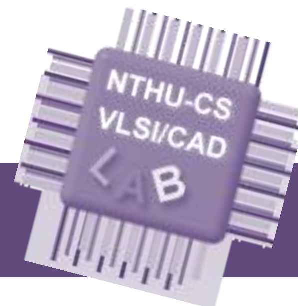

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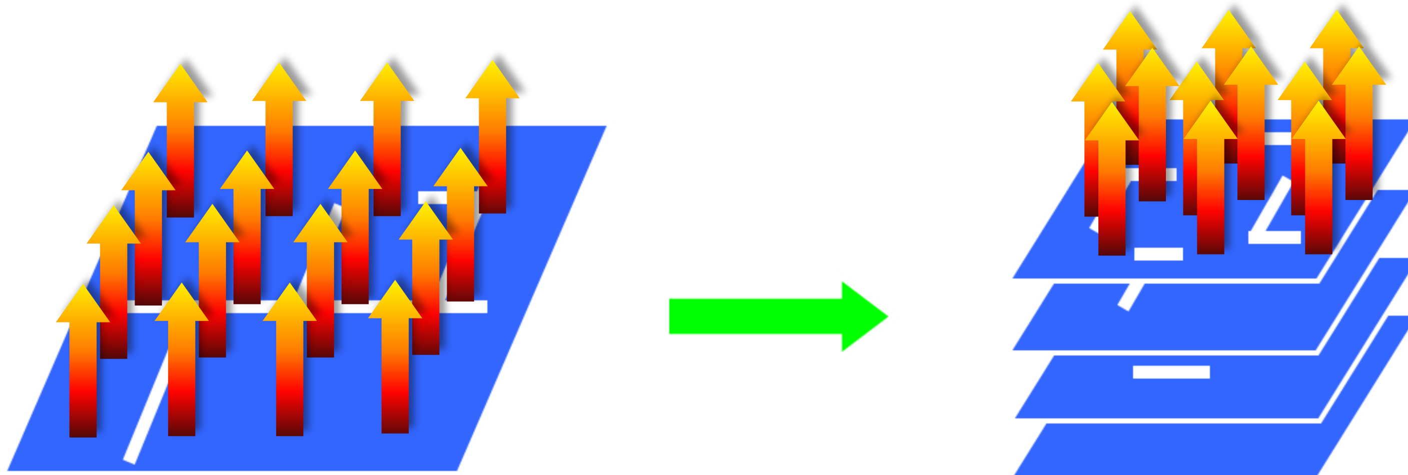
Outline

- Introduction
- Motivation
- Stacked-TSV Assignment & Relocation
- Experimental Results
- Conclusions

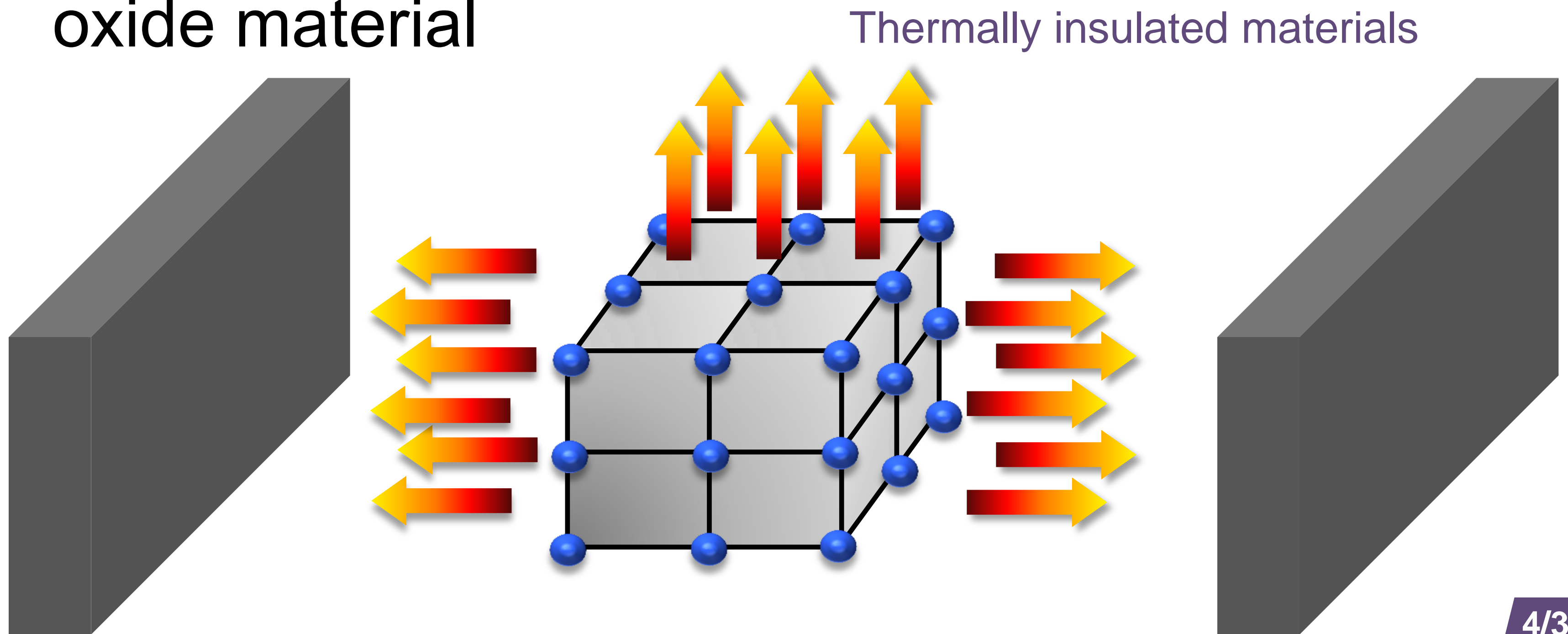
3D IC

- 3D IC reduces the interconnect delay and integrates heterogeneous components
- High power density and lower thermal conductivity produce critical thermal issue



Heat Dissipation in 3D IC

- The heat dissipation in vertical direction is the critical issue in 3D IC
- Thermal conductivity of Si is much better than oxide material



Related Work

- Thermal via insertion method
  - Zhang at el. “Temperature-aware routing in 3D ICs”, *ASP-DAC’06*
  - Cong and Zhang “Thermal via placement in 3D ICs”, *ISPD’05*
  - Goplen and Sapatnekar “Placement of thermal vias in 3D ICs using various thermal objectives”, *TCAD’06*
  - Wang et al. “Rethinking thermal via planning with timing-power-temperature dependence for 3D ICs”, *ASP-DAC’11*

Extra via overhead

- Thermal aware routing and placement
  - Pathak and Lim “Performance and thermal-aware Steiner routing for 3-D stacked ICs”, *TCAD’09*
  - Cong et al. “Thermal-Aware Cell and Through-Silicon-Via Co-Placement for 3D ICs”, *DAC’11*
  - Chen et al. “A new design architecture for power network in 3D ICs”, *DATE’11*

Without fully utilization of stacked signal TSV

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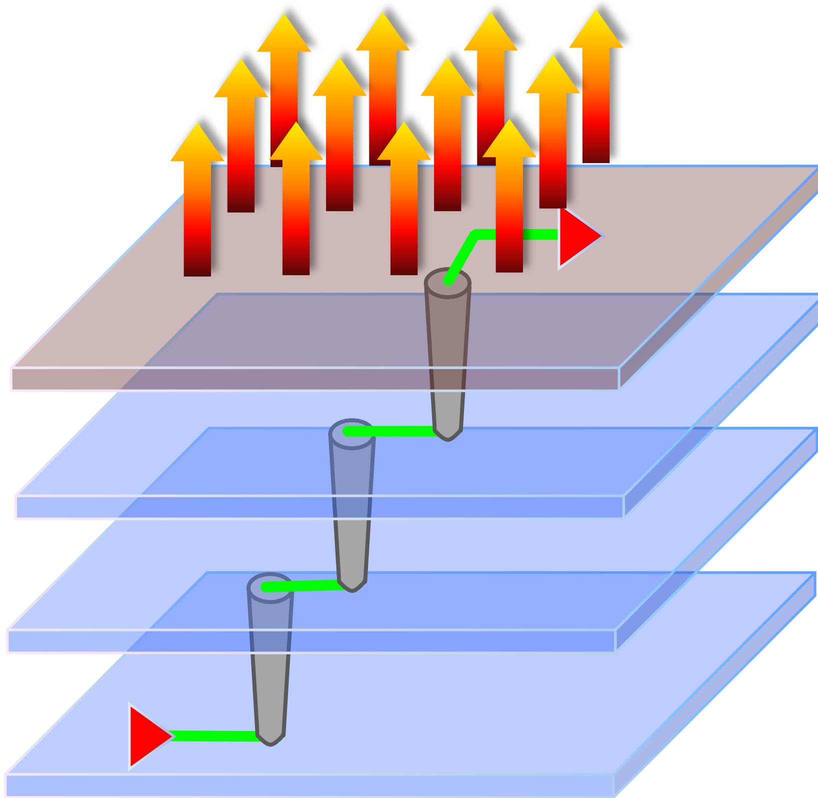
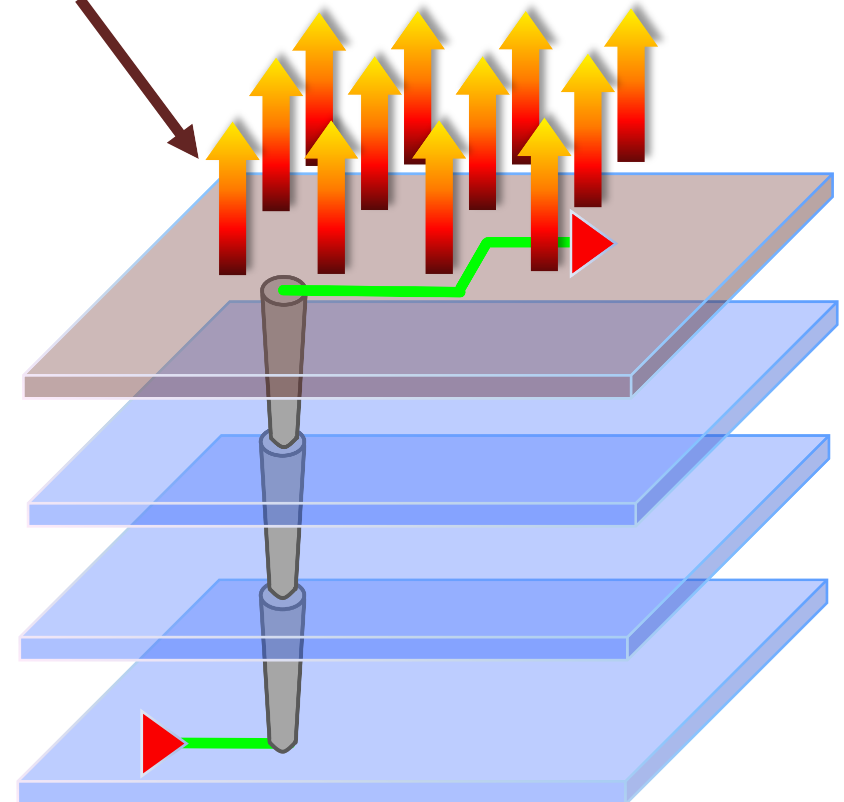
Non-stacked TSV vs. Stacked Signal TSV

Non-stacked signal TSVs

Stacked signal TSVs





Heat sink layer

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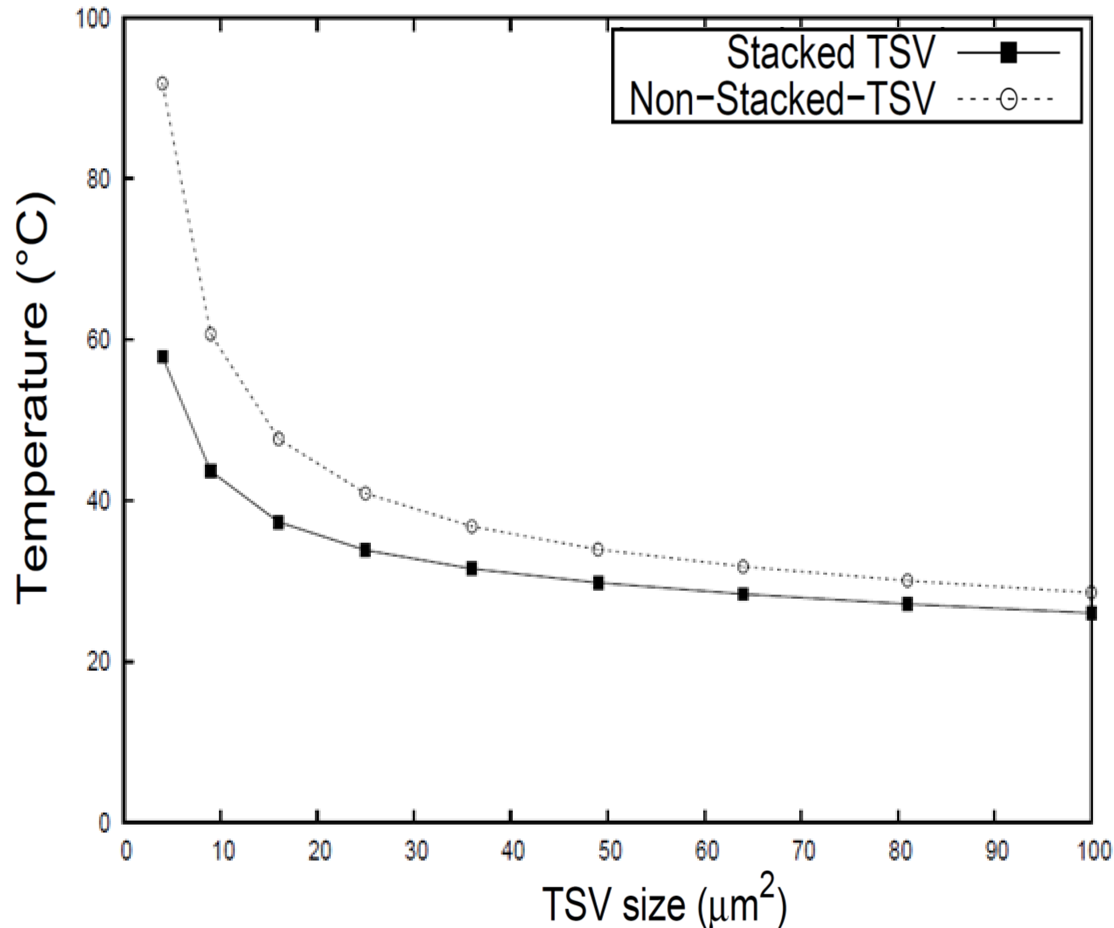
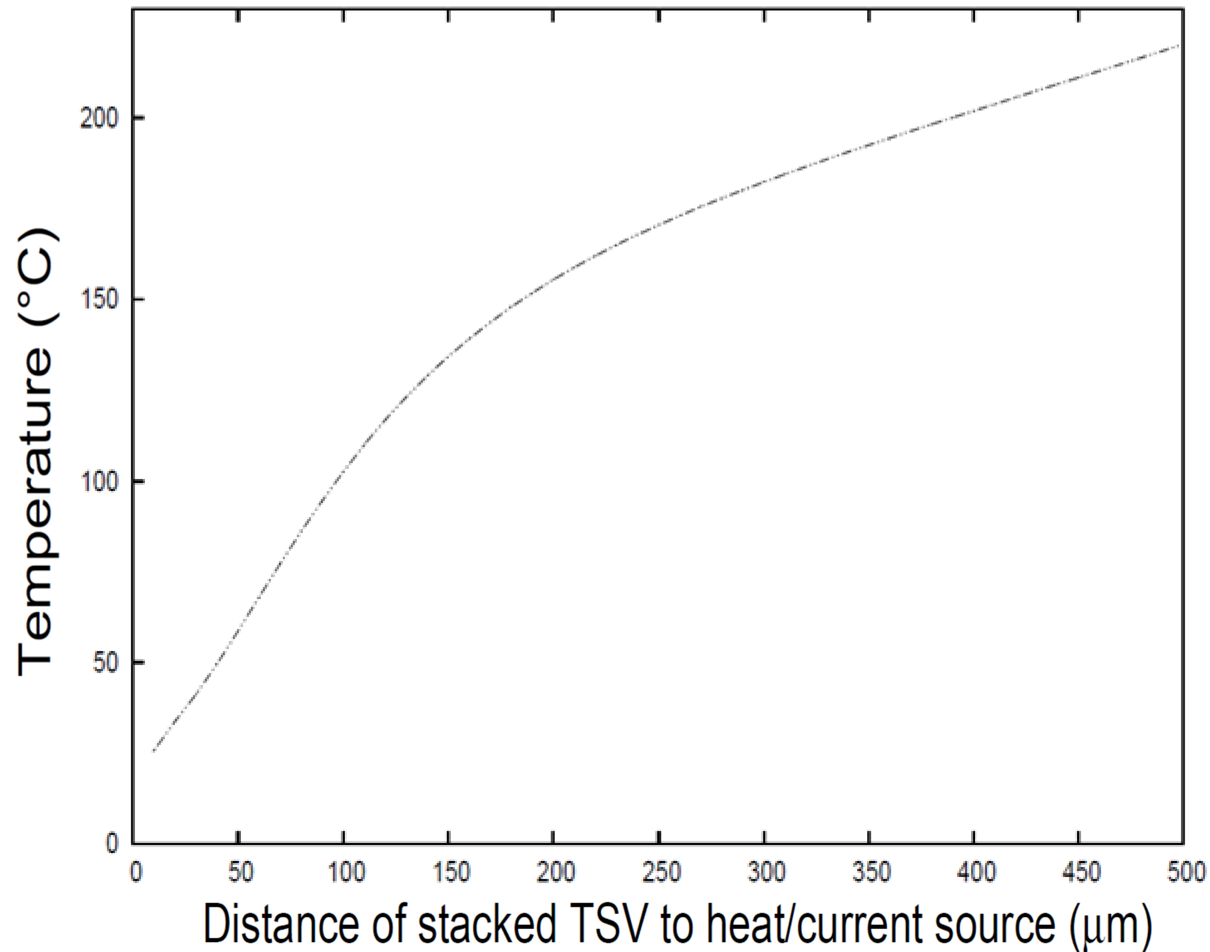
Temperature Comparison of Stacked TSV and Non-stacked TSV

- Stacked TSV has better thermal dissipation



Temperature vs. Distance of Stacked TSV



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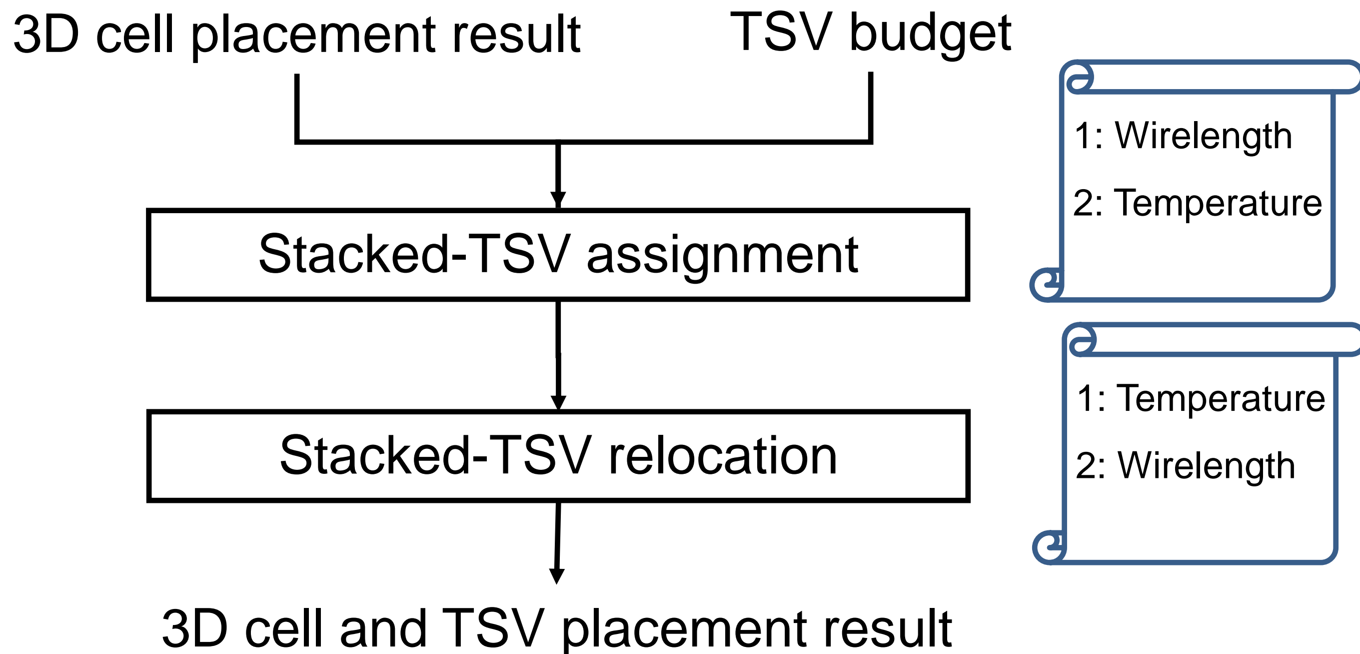
Problem Definition

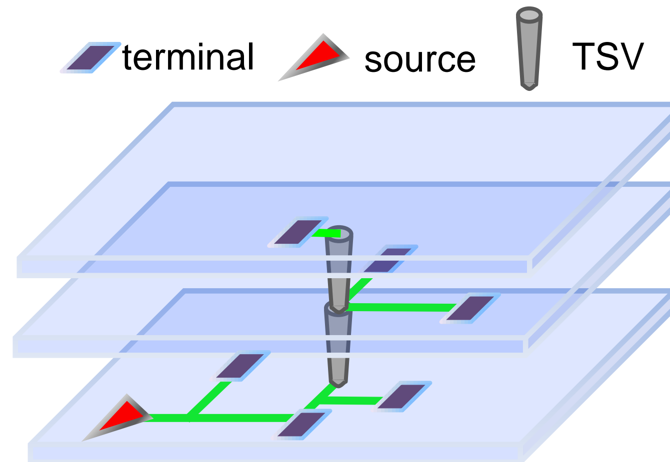
- Input:
  - 3D cell placement result
  - TSV budget
- Output:
  - 3D cell and TSV placement result
- Objective:
  - Wirelength
  - Temperature

Overall Flow

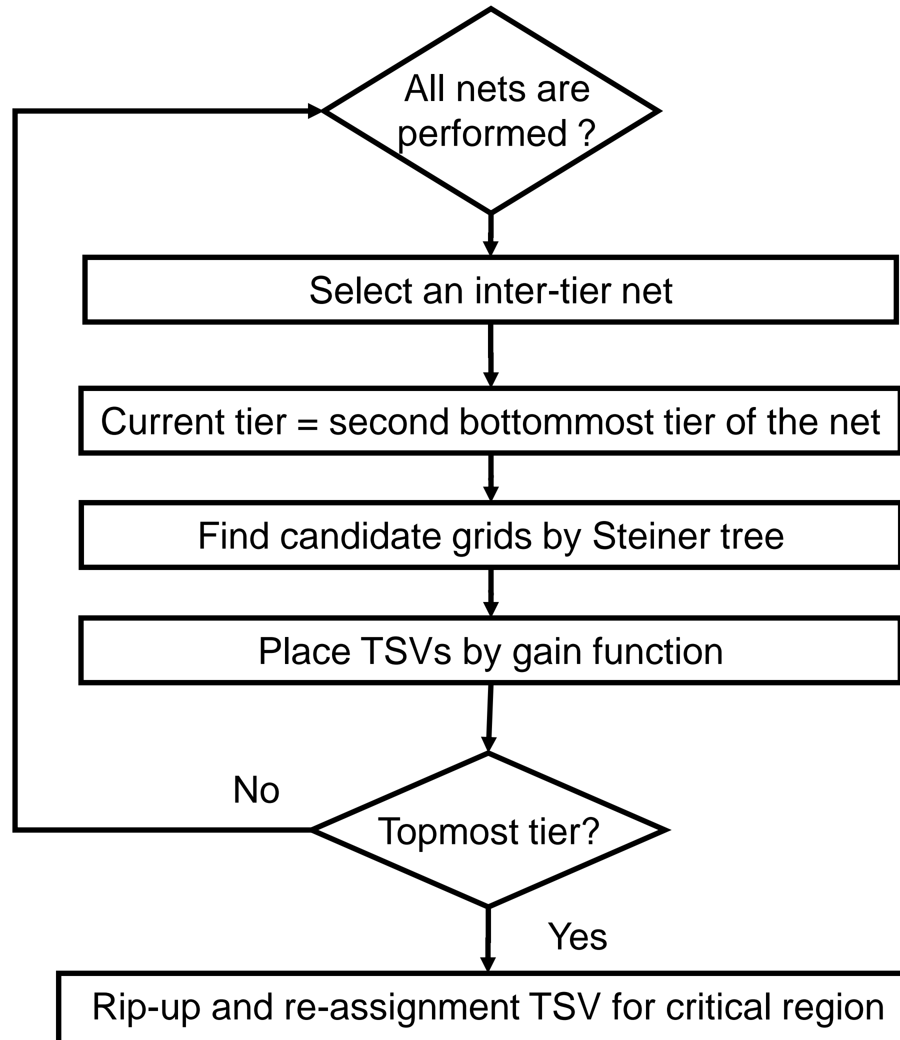


Stacked-TSV Assignment Stage

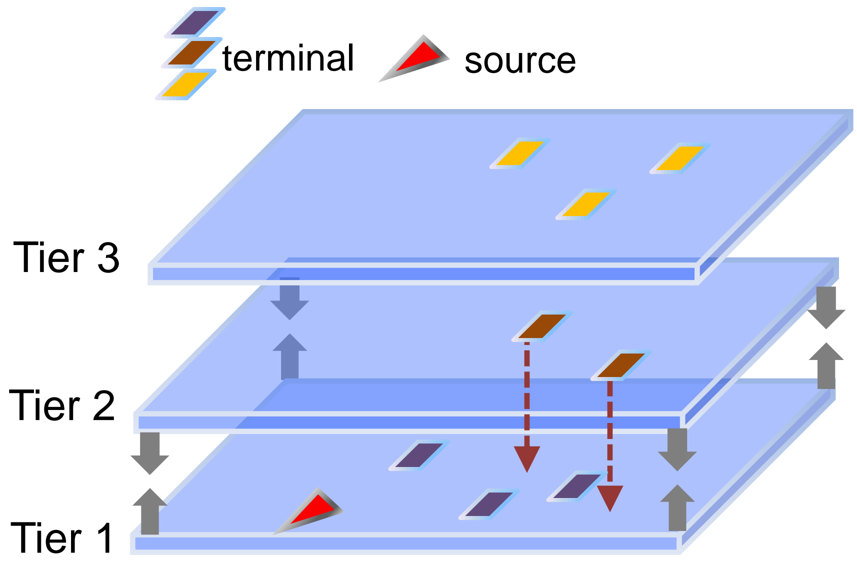
- Assign TSV within bounding boxes for each inter-tier net ➔no wirelength overhead
- Place as many stacked signal TSVs as possible ➔reduce temperature



Stacked TSV Assignment Flow



Find Candidate Grids by Steiner Tree



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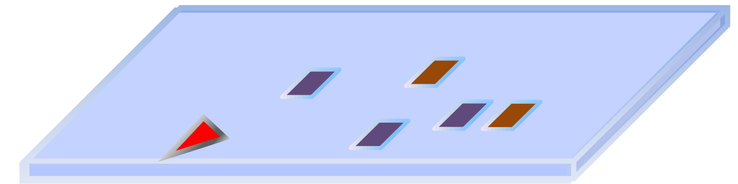
Map adjacent tier sinks to 2D plane



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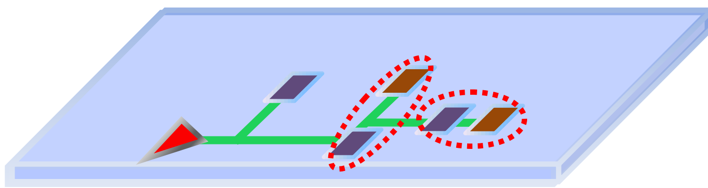
Construct 2D Steiner tree



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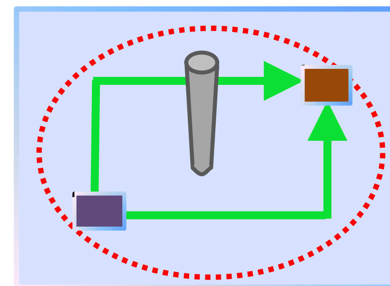
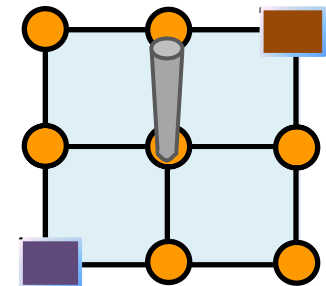
Aerial view



Grid view

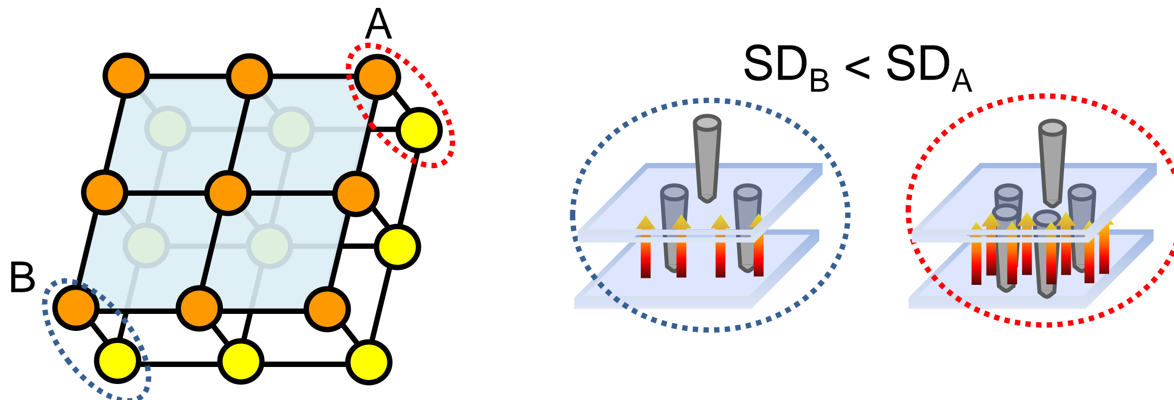


Gain Function for Candidate Grids

- Select the TSV location by a gain function
  - Grid with larger gain value is selected to place signal TSV

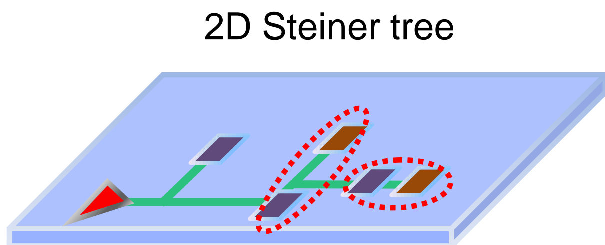
$$Gain_{i,j,k} = SD_{i,j} \times \frac{\sum_{k=1}^{n} PowDensity_{i,j,k}}{TSVNum_{i,j,k}}$$

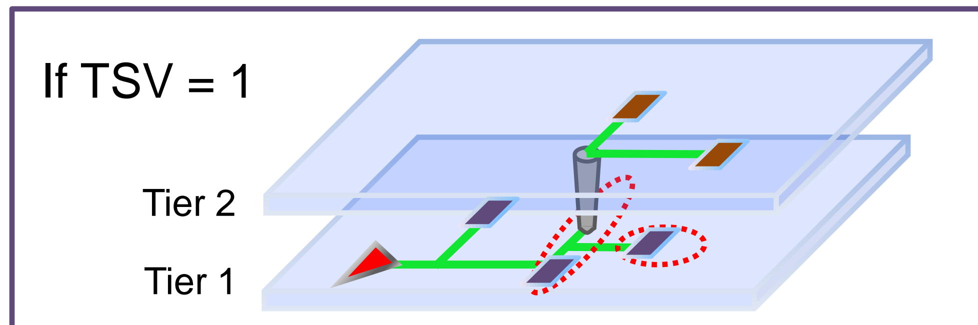
$PowDensity_{i,j,k}$	Power density in grid (i,j,k)
$TSVNum_{i,j,k}$	Number of signal TSVs in grid(i,j,k)
$SD_{i,j}$	Stacking degree in grid (i,j)

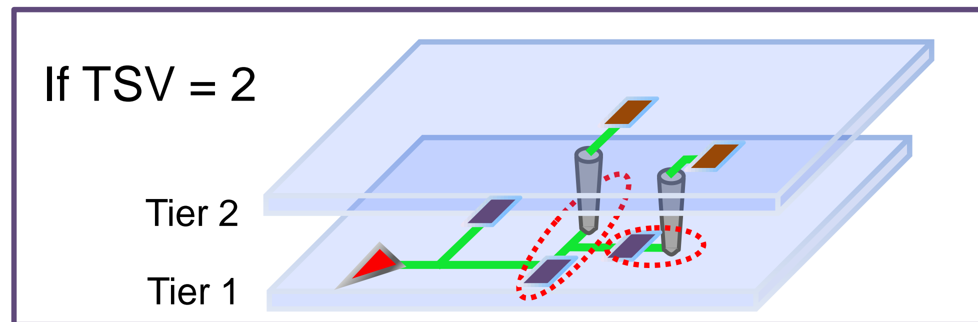


Signal TSV Placement

- For the given TSV budget *N*, we select *N* candidate grids which have largest gain values

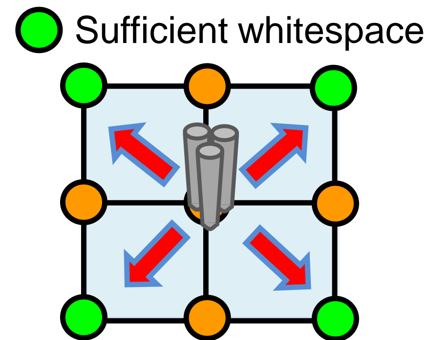




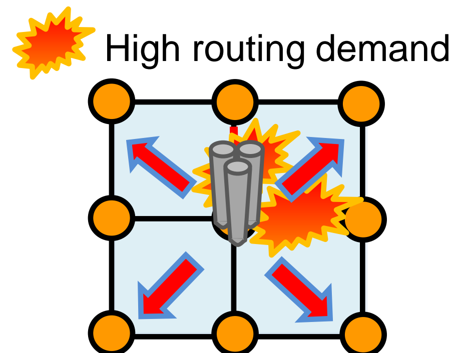


Rip-up and Re-assignment TSV for Critical Region

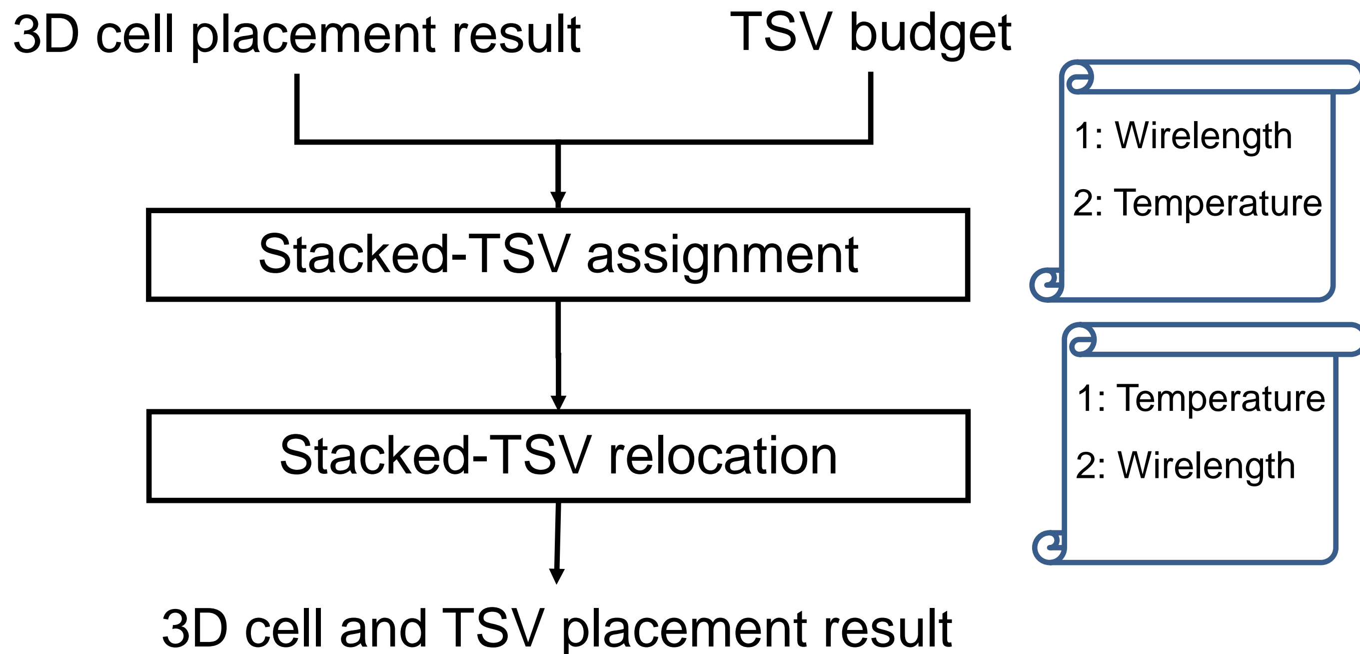
- Re-assign TSVs in overflow grids to nearby grids that have whitespace



- Re-assign TSVs in congested grids to nearby low routing demands grids

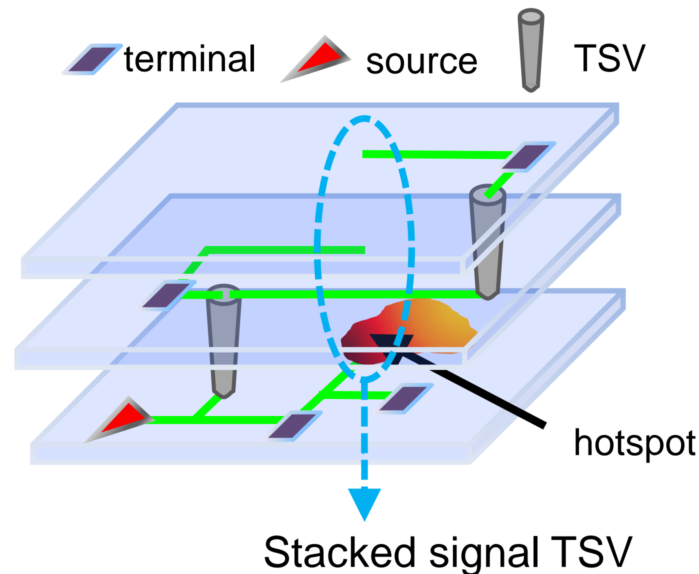


Overall Flow



Stacked-TSV Relocation Stage

- Not all hotspot grids are near the candidate grids in bounding boxes
- Relocate stacked signal TSV to the hotspot grid outside the bounding boxes with minimum wiring overhead



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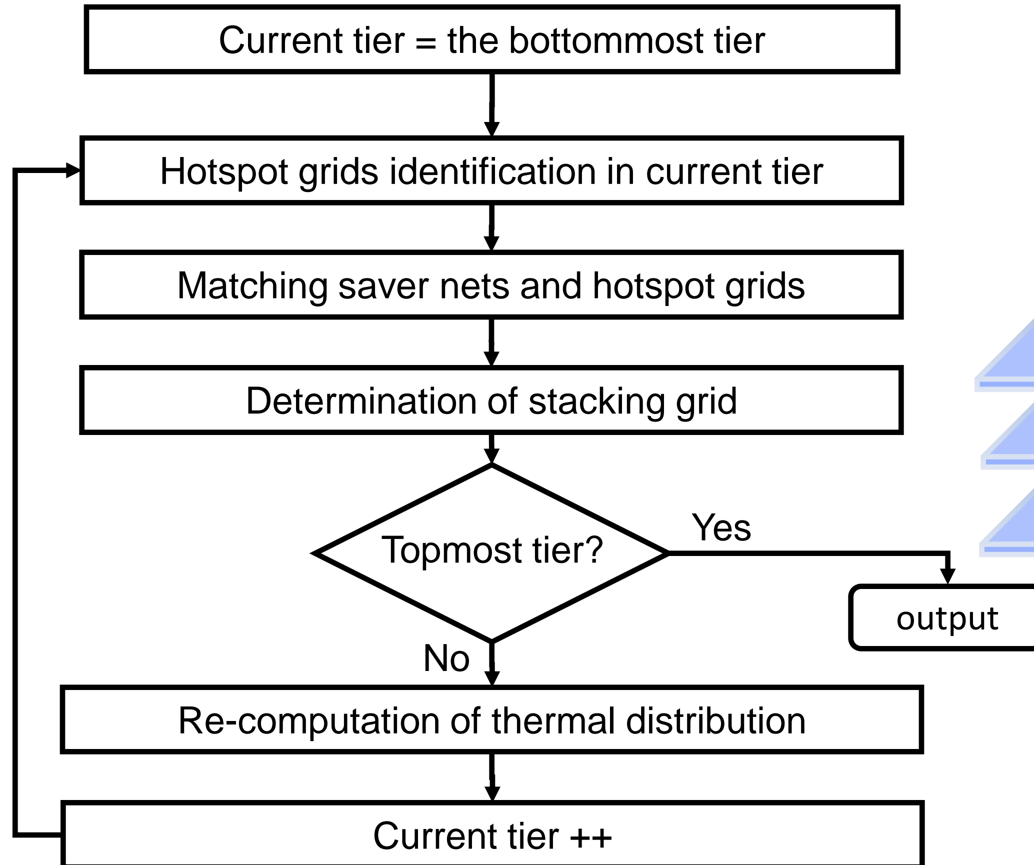
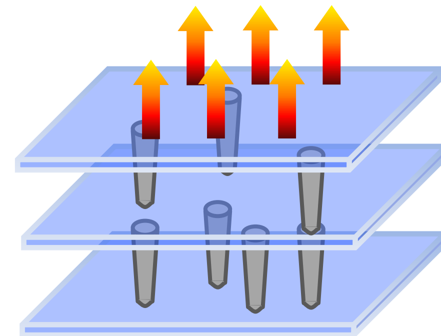
Stacked TSV Relocation Flow



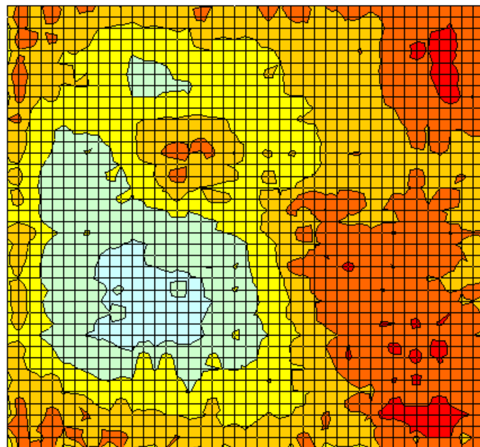


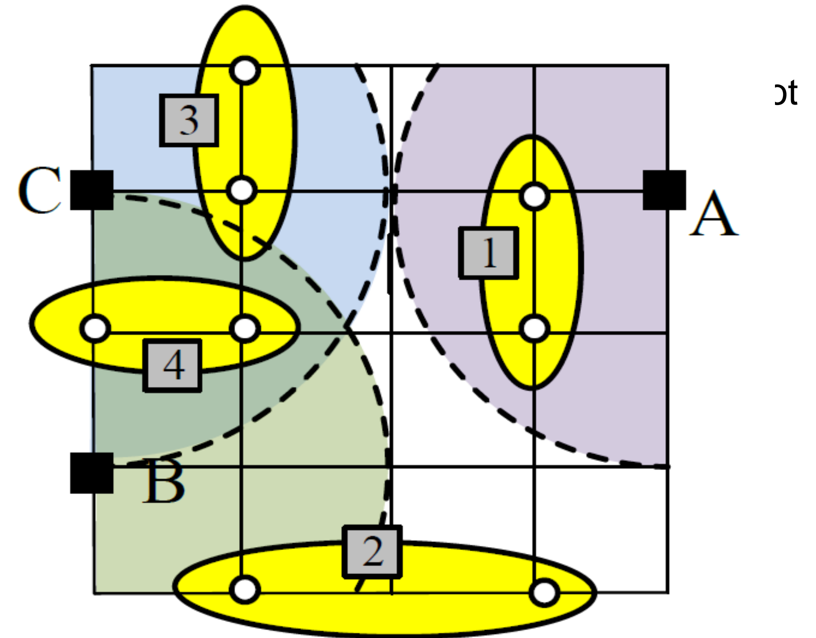
Explore Saver Nets

10 % highest

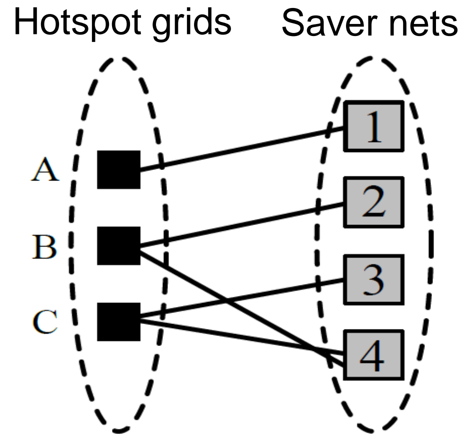
$$ThermalCri_{i,j,k} = \frac{\sum_{k=1}^{n} PowDensity_{i,j,k}}{TSVNum_{i,j,k}}$$

Critical hotspot identification



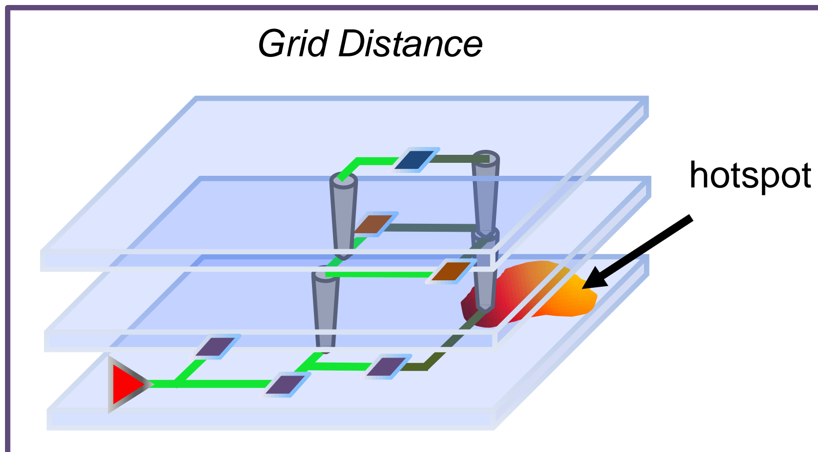


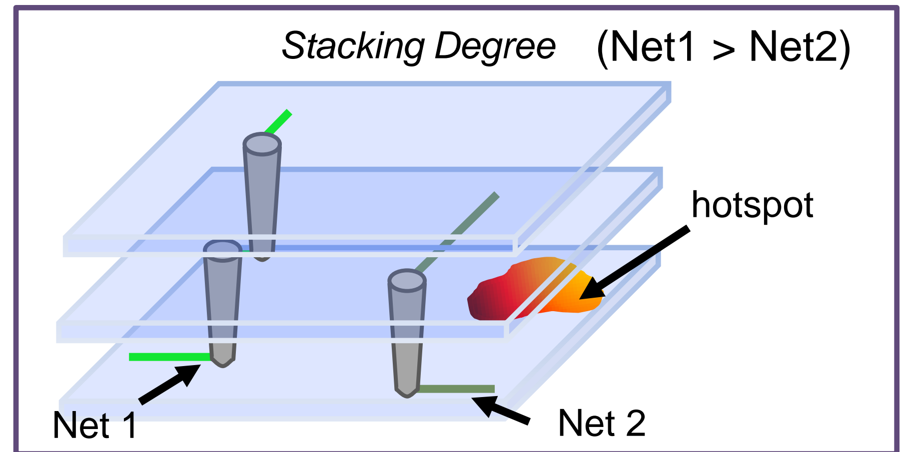
Select Pairs of Nets and Grids



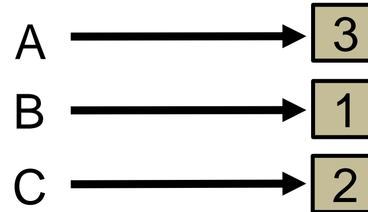
$$EdgeCost(g,n) = GridDist - StackingDegree$$

(wirelength overhead) (heat dissipation ability)



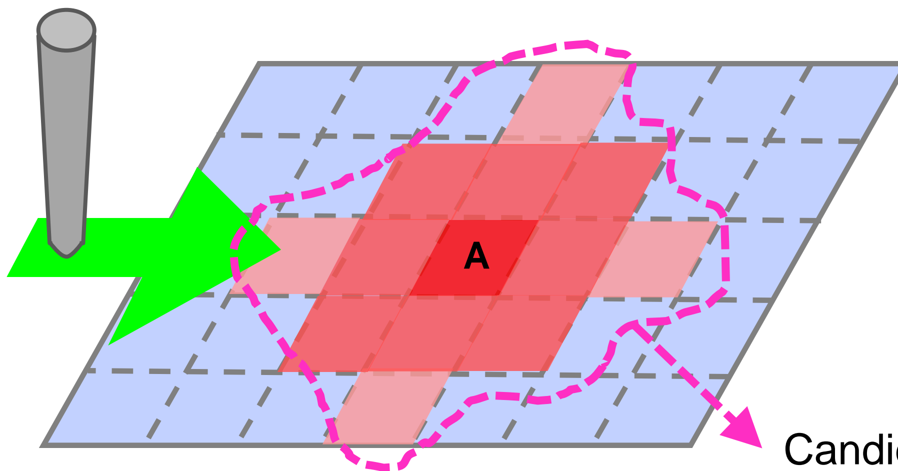


Place Stacked TSV by Gain Function



$$Gain_{i,\,j} = DSST_{i,\,j} + \sum_{k=1}^{n} Power_{i,\,j,\,k} + \sum_{k=1}^{n} TSV_{i,\,j,\,k} + \sum_{k=b}^{t} WSDens_{i,\,j,\,k} + \sum_{k=b}^{t} WL_{i,\,j,\,k}$$

	Thermal	Wirelength
DSST	✓	
Power	✓	
TSV	✓	
WSDens		✓
WL		✓



Candidate target grid

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Experimental Environment

- Benchmarks are from reference work [5]
- 3D placement results produced by a partitioning-driven placement for 3D IC [5]
- Use FLUTE [19] to estimate global routing wirelength
- The topmost layer of chip and ambient temperature set to 25 ℃

Key Parameters

Wafer thickness	50 um	6670 (um * K/W)
TSV size	25 um^2	2500 (um * K/W)
Interposer thickness	100 um	$3*10^6$ (um * K/W)
Low-K thickness	2 um	10^6 (um * K/W)
SiO2 of TSV thickness	0.2 um	10^6 (um * K/W)
Power dissipation	$1 \sim 10^7$ W/cm^2	

Experimental Results

- Baseline result [5]
- Thermal-TSV insertion method [1]

	baseline [5]					thermal-TSV insertion method [1]		
ckt	*TSV*	*S.TSV*	*Tmax*($^\circ C$)	*Tavg*($^\circ C$)	wire(μm)	*TSV*	*Tmax*	*Tavg*
ckt1	3495	101	168.6	155.7	3.46e+06	4580	129.4	120.6
ckt2	21146	566	91.5	86.3	9.21e+06	23748	84.3	81.4
ckt3	46621	1215	91.4	84.6	2.53e+07	53549	87.3	82.3
ckt4	33560	545	110.5	99.2	2.55e+07	39562	94.9	88.2
ckt5	22498	1548	147.0	133.3	1.60e+07	31116	122.9	116.5
Ratio	1	1	1	1	1	1.23	0.83	0.87

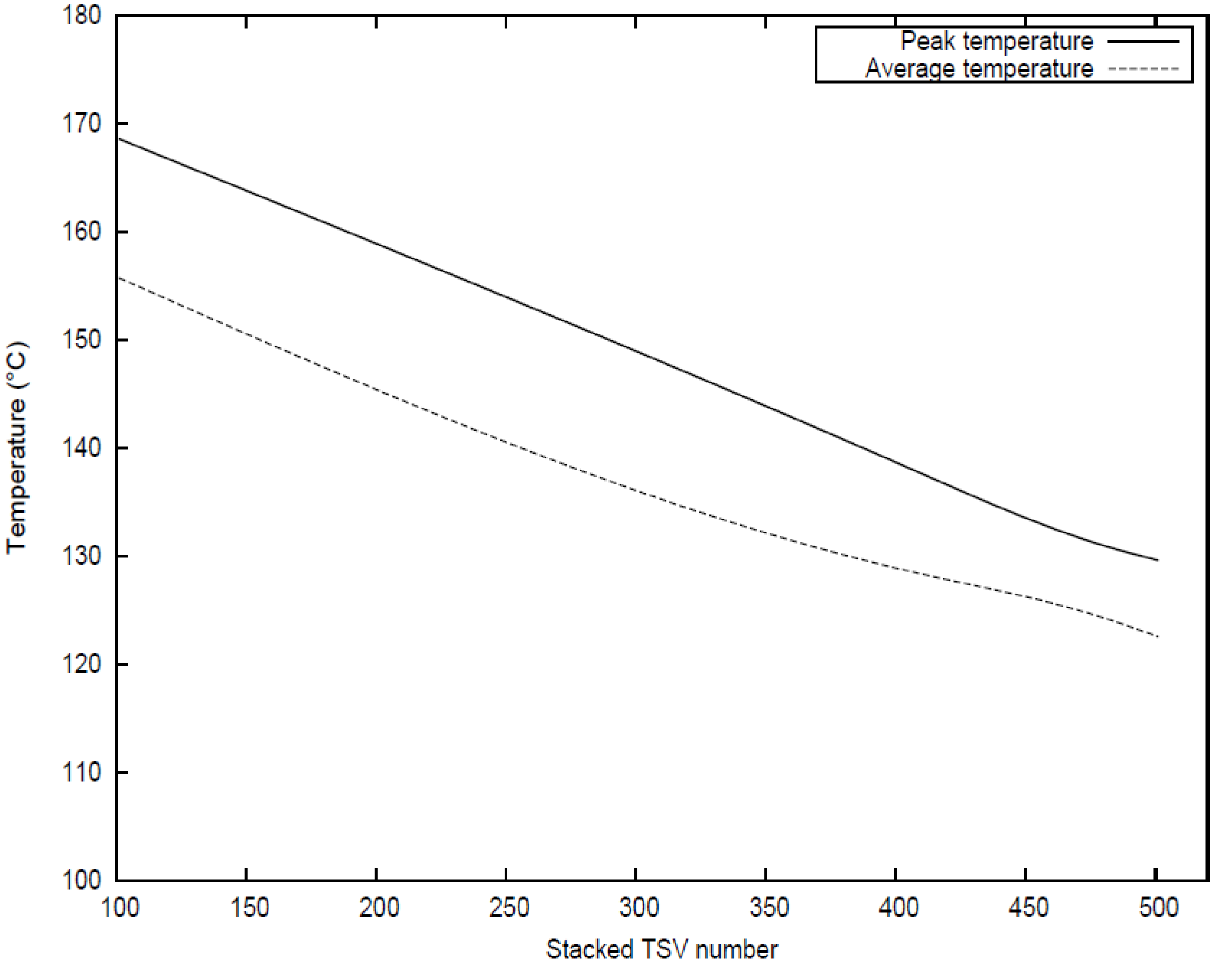
ours				
TSV	*S.TSV*	*Tmax*	*Tavg*	wire
3495	501	129.1	122.0	3.59e+06
21146	2513	84.3	81.5	9.65e+06
46621	5068	86.0	82.5	2.51e+07
33560	2723	93.4	86.0	2.70e+07
22498	2163	123.0	116.2	1.68e+07
1	2.99	0.83	0.87	1.04

Routing Congestion Results

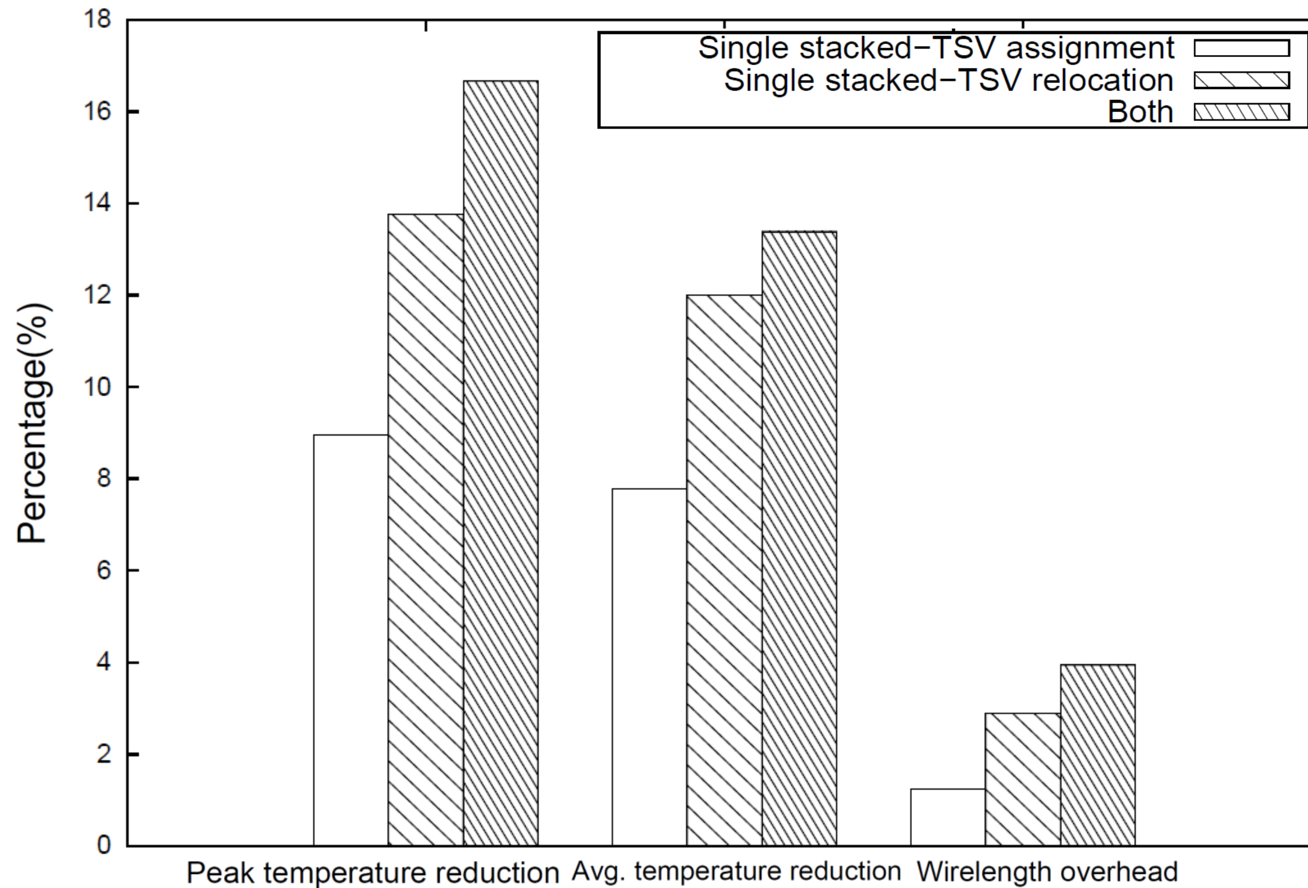
- 3D Elmore delay model [11] is used to estimate maximum delay value

	Congestion				Delay
	baseline		ours		
ckt	$AvgR_d$	$MaxR_d$	$AvgR_d$	$MaxR_d$	$Delay_{ratio}$
ckt1	35.5	119.5	36.7	110.5	1.00
ckt2	37.1	138.5	38.53	124	1.02
ckt3	51.7	185	50.81	181	1.07
ckt4	49.4	236.5	52.2	213.5	1.06
ckt5	28.85	131	30.1	97.5	1.00
Ratio	1	1	1.03	0.89	1.03

Stacked TSVs vs. Temperature in ckt1



Analysis of Each Step



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Conclusions

- An algorithm is proposed to construct stacked signal-TSVs for heat dissipation
- The experimental results show that our algorithm has 17% temperature reduction with 4% wiring overhead

Thank You