Stable Backward Reachability Correction for PLL Verification with Consideration of Environmental Noise Induced Jitter

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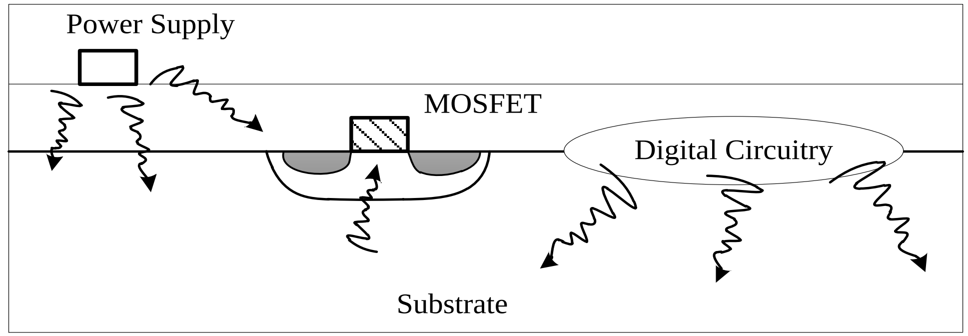
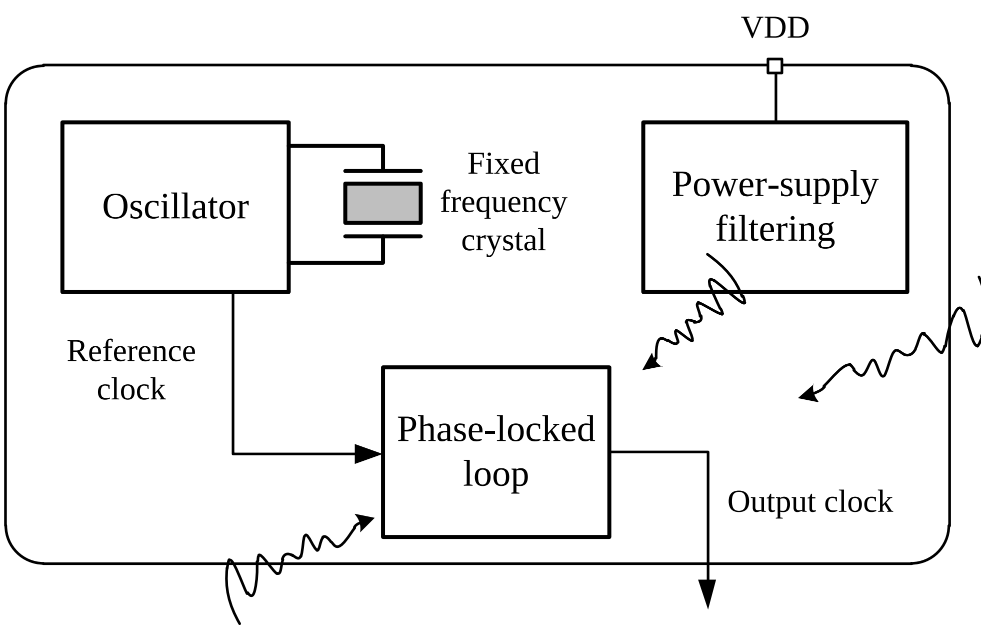
Outline

- PLL phase deviation by jitter
- Reachability analysis
- Backward reachability correction
- Experimental results
- Summary

PLL and Noise Injected Perturbation

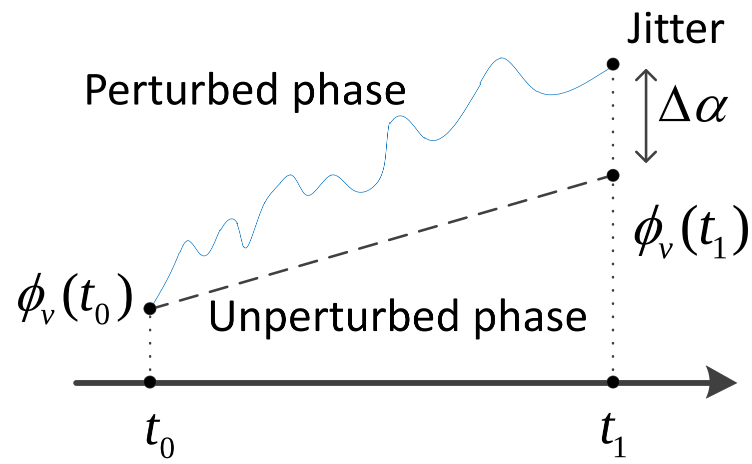
- Injected noise through substrate or power-supply



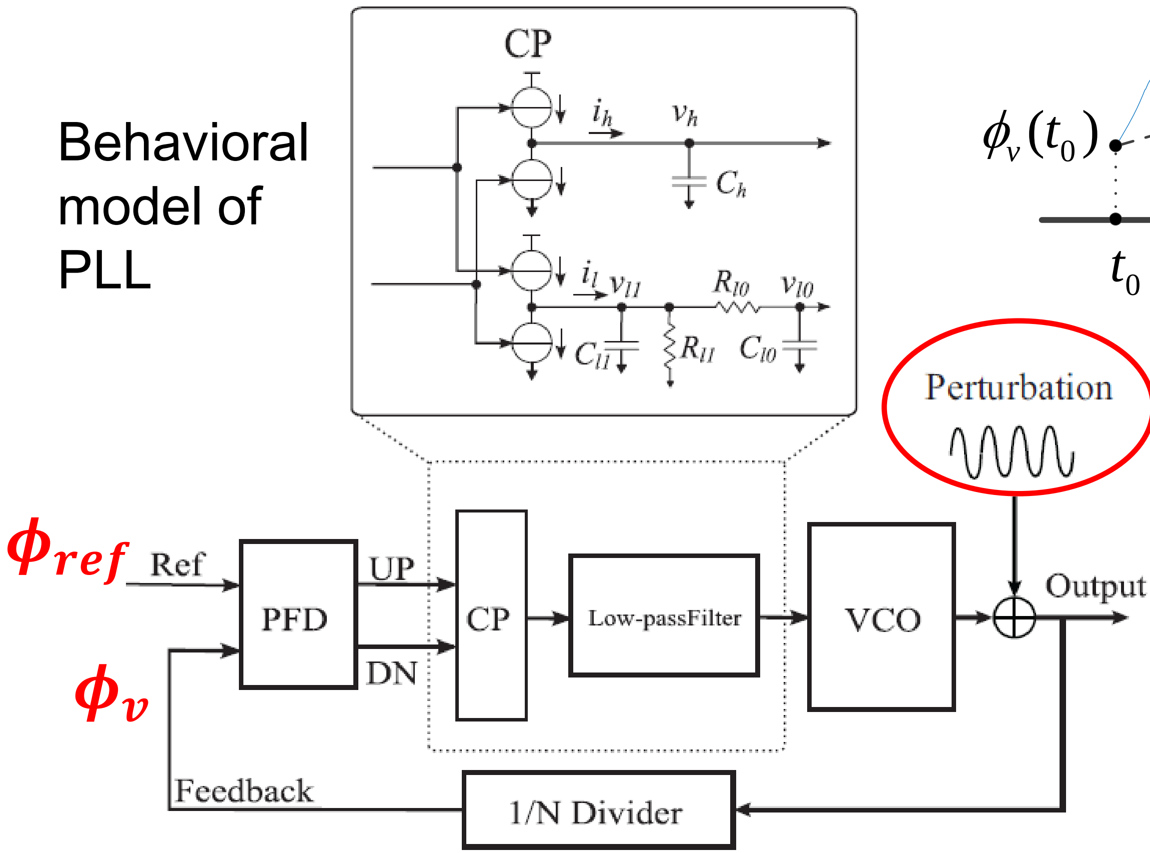


- Perturbation coupled to PLL

Induced Phase Deviation and Jitter



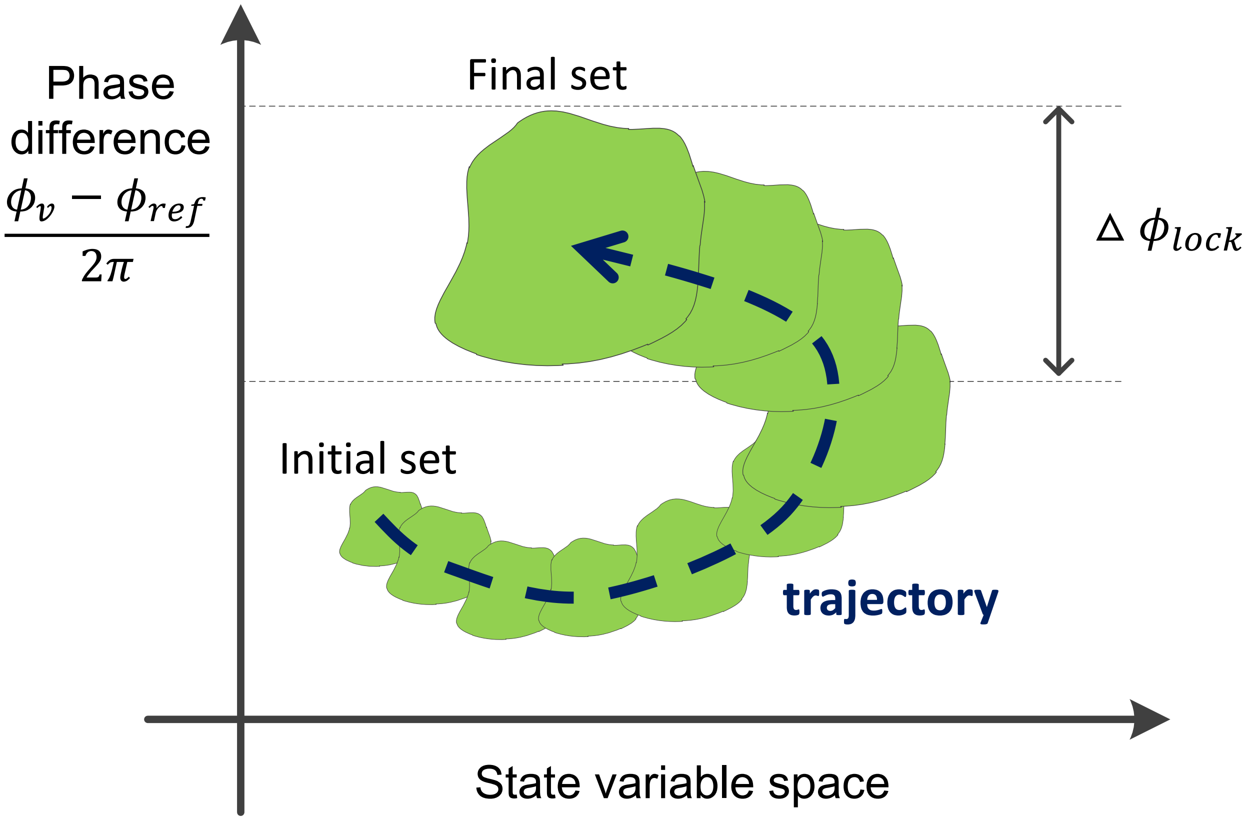
Behavioral model of PLL



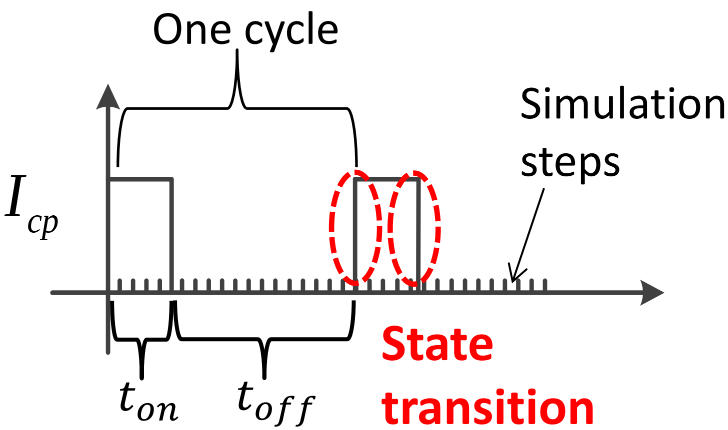
$$\phi_{lock} \coloneqq \phi_v - \phi_{ref} \in \textit{locking bound}$$

Reachability Analysis for PLL Verification

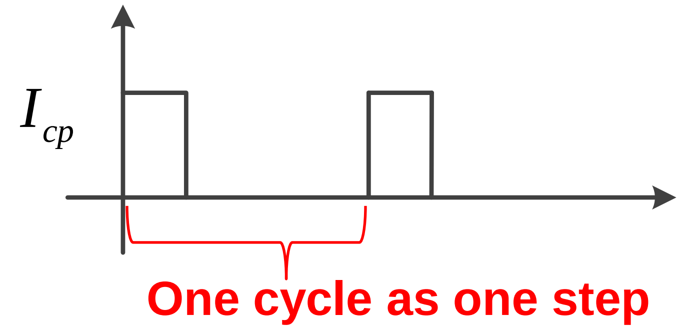
- Reachability analysis has been deployed to exam locking range after system settles down.



Previous Work



Challenge:
To capture state transitions of CP
⇨ Simulation step is tiny
⇨ Too many steps



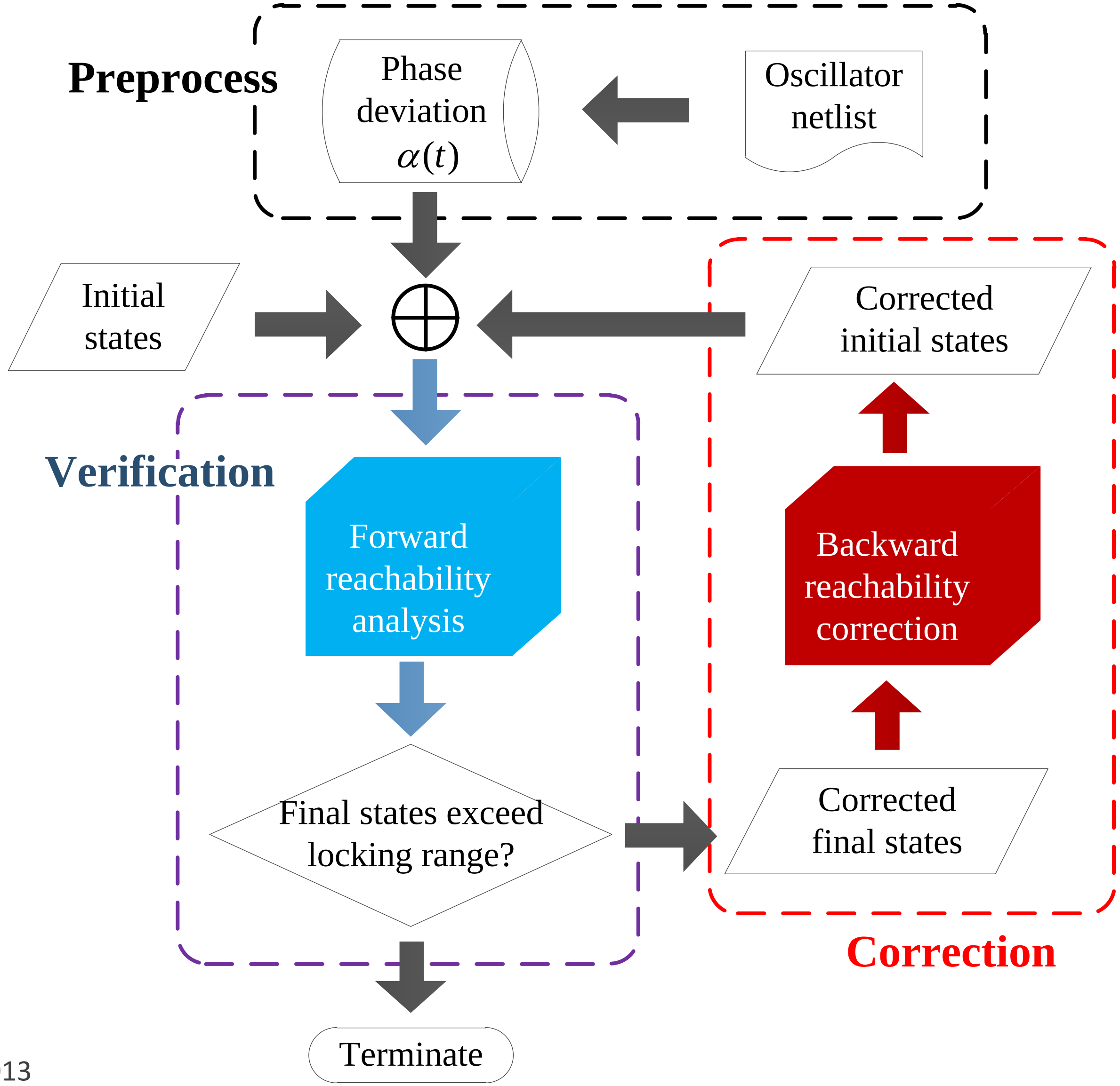
Continuization [1]:

- Responses to different inputs to CP in a cycle are calculated simultaneously
- No need of explicit simulation of state transitions

- Pro
  - Less calculation
- Con
  - No jitter induced phase deviation considered
  - No correction if verification failed

[1] M. Althoff and et.al. *ICCAD*, 2011.

Reachability based PLL Jitter Verification and Correction Flow



Nonlinear Phase Noise Model by PPV

Perturbed system: $\boxed{\dot{x} = f(x)} + b(t)$

Noiseless system

Injected perturbation

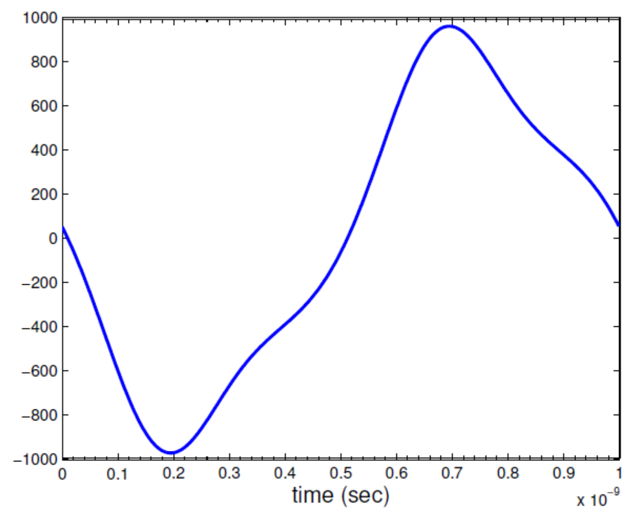
Perturbed solution: $x(t) = x_{pss}(t + \boxed{\alpha(t)})$

Accumulated phase deviation

$$\dot{\alpha}(t) = v(t)^T\big(t + \alpha(t)\big) \cdot b(t)$$

Perturbation Projection Vector (PPV) [2]

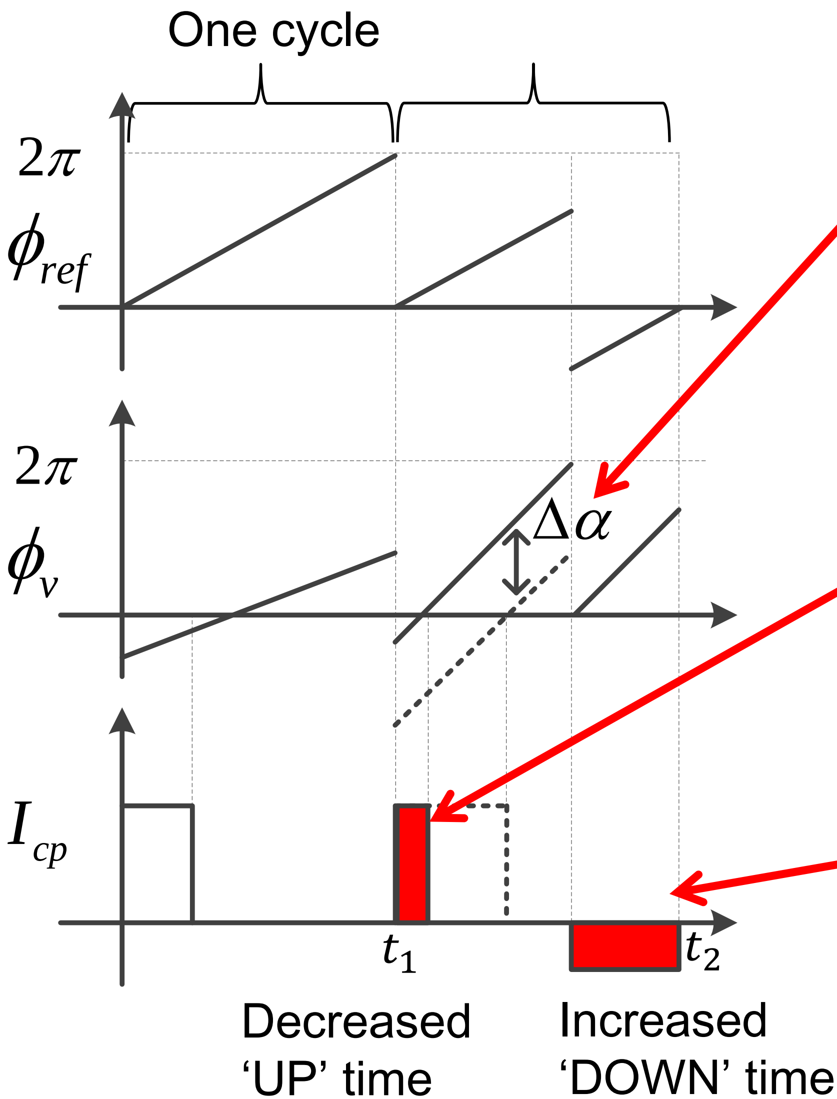
1. Represent oscillator phase sensitivity under perturbation
2. Can be computed directly from PSS solution



PPV curve of an oscillator

[2] X. Lai and et.al. *CICC*, 2004.

PPV Calculated of Phase Deviation and Jitter



Phase deviation and jitter caused by perturbation

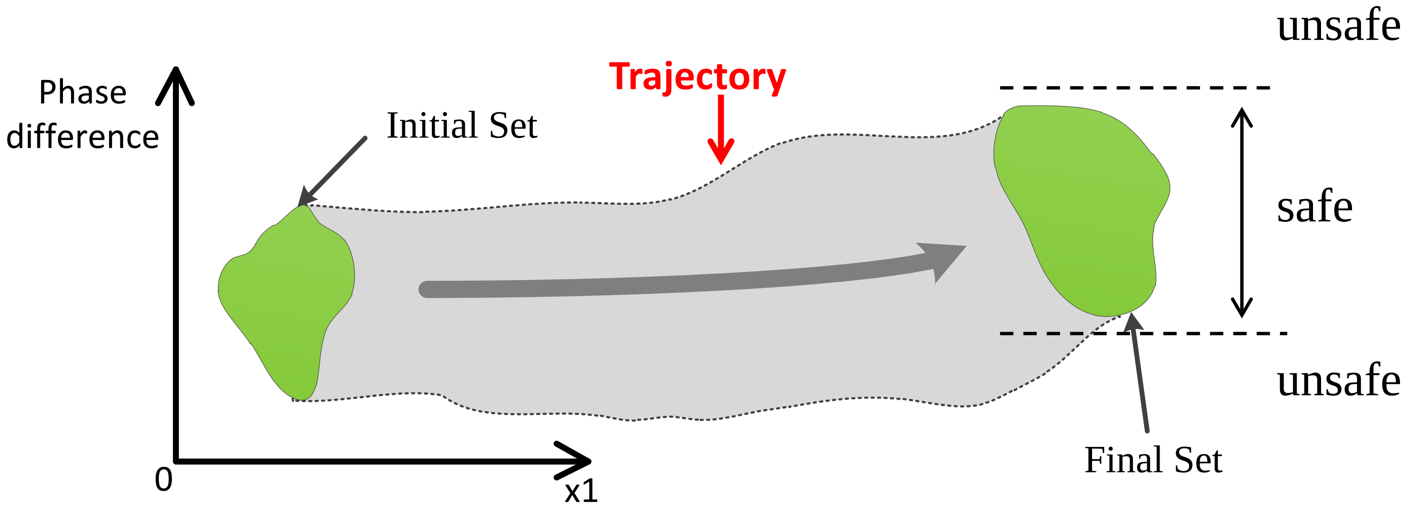
Up active: $\phi_v(t_1) < 0, \phi_{ref}(t_1) > 0$

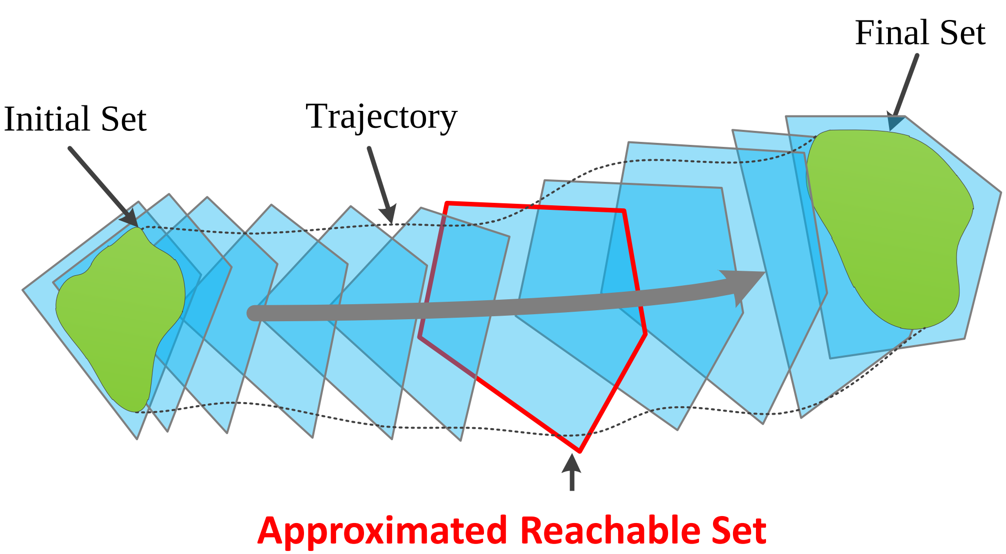
$$t_{on}^{up} = \frac{-\phi_v(t_1) + 2\pi f \cdot \Delta\alpha}{\dot{\phi}_v}$$

Down active: $\phi_v(t_2) > 2\pi, \phi_{ref}(t_2) < 2\pi$

$$t_{on}^{down} = \frac{\phi_v(t_2) - 2\pi + 2\pi f \cdot \Delta\alpha}{\dot{\phi}_v}$$

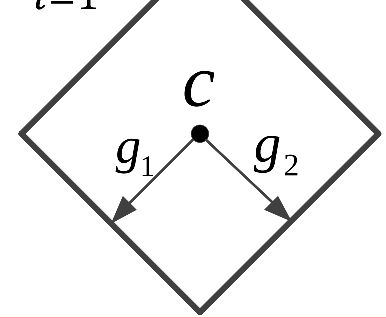
Reachability Analysis: Zonotope





Zonotope

$$z = c + \sum_{i=1}^{e} \beta_i g_i \ , -1 \leq \beta_i \leq 1$$



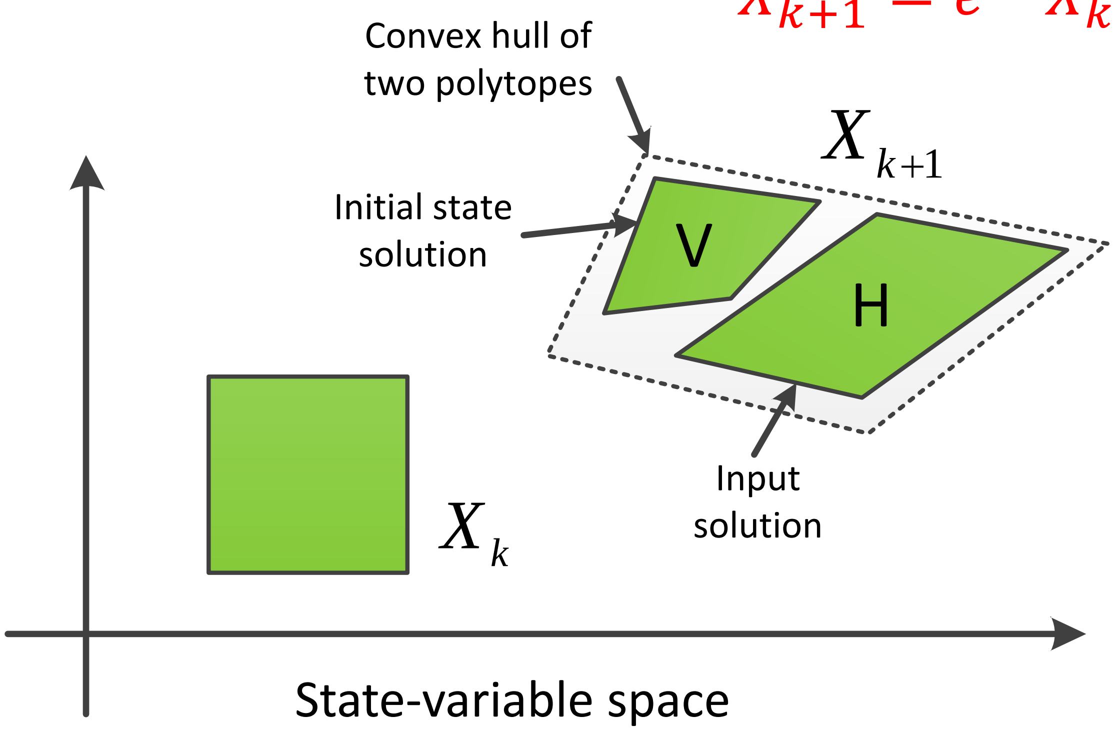
Reachability Analysis: Forward Evolution of New Set

$$\dot{x} = Ax + u$$

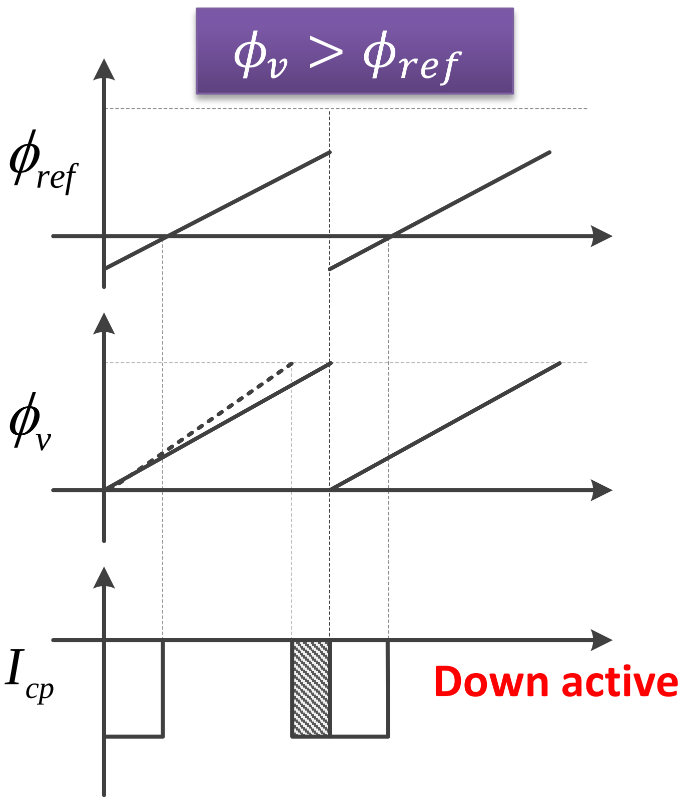
$$x = \underbrace{e^{At}x}_{\text{Initial state solution}} + \underbrace{A^{-1}u(e^{At} - I)}_{\text{Input solution}}$$

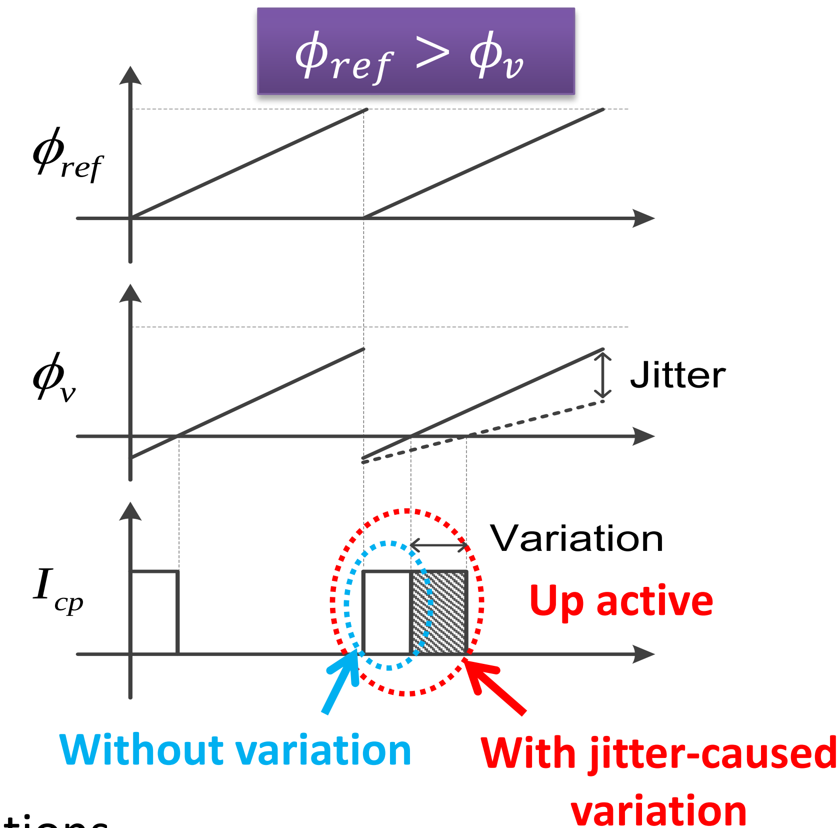
Superposition principle

$$X_{k+1} = e^{At}X_k \oplus X_{input}$$



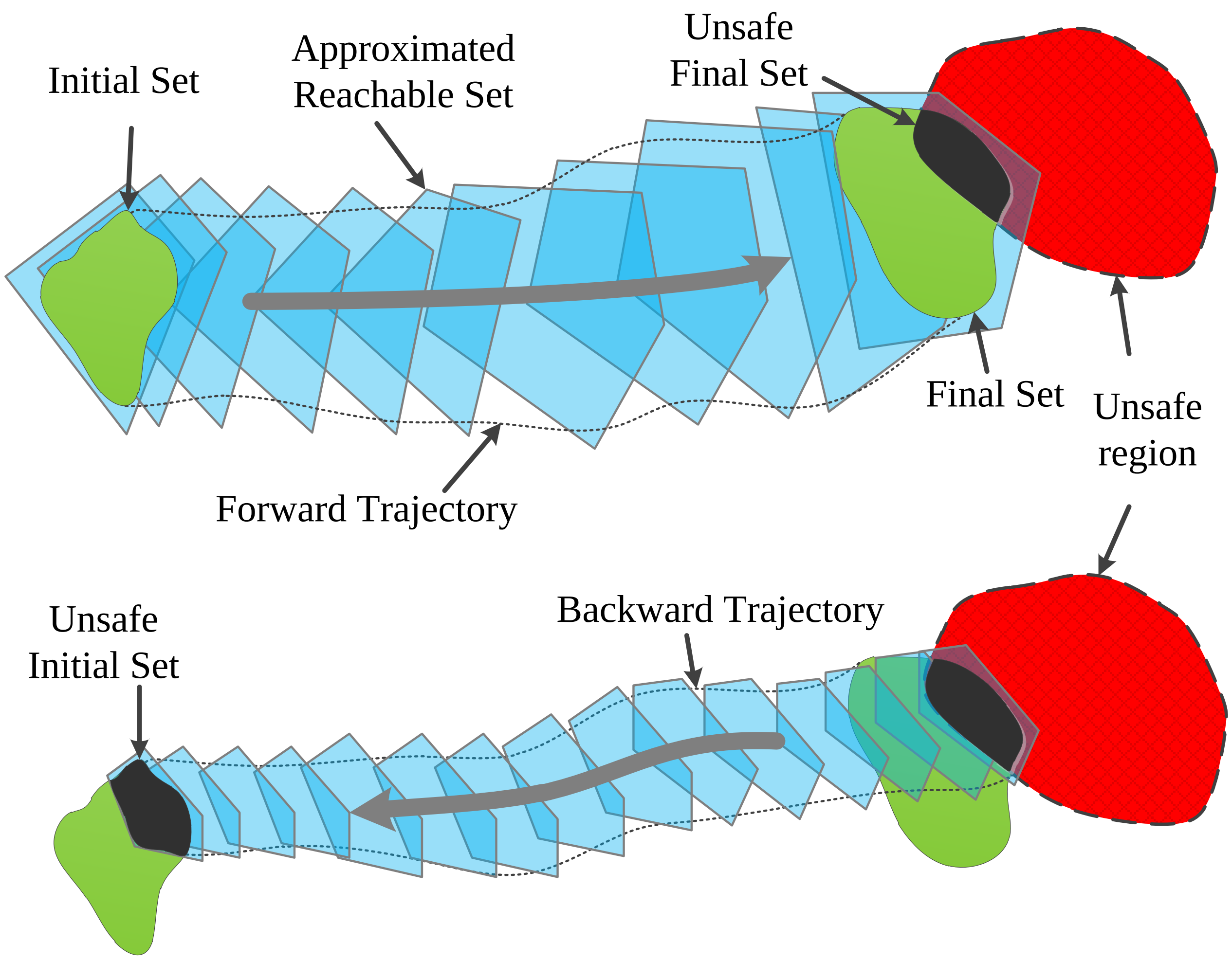
Reachability Analysis for PLL Verification with Jitter





$$X_{k+1} = e^{Ar}X_k \underset{\text{Minkowski sum}}{\oplus} \overbrace{X_{up} \oplus X_{down} \oplus X_{both}}^{\text{Possible input solutions}} \qquad X_{up} = A^{-1}u\left(e^{A(t+\Delta t)} - I\right)$$

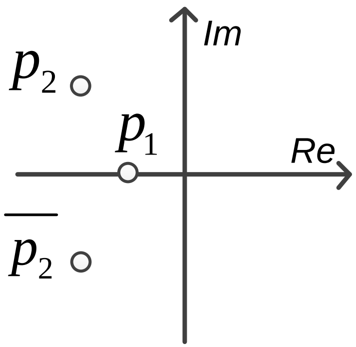
Backward Correction



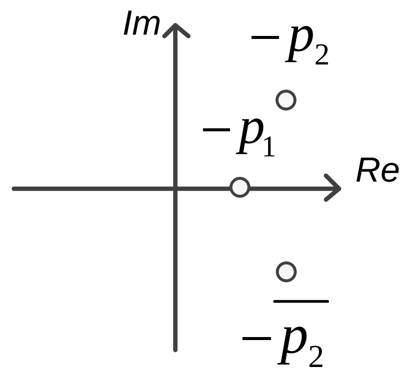
Corrected Initial Set

Stability Problem in Backward Correction

$$X(s) = \frac{Bu}{s-A} \xrightarrow{\text{reverse}} X(s) = \frac{-Bu}{s+A}$$

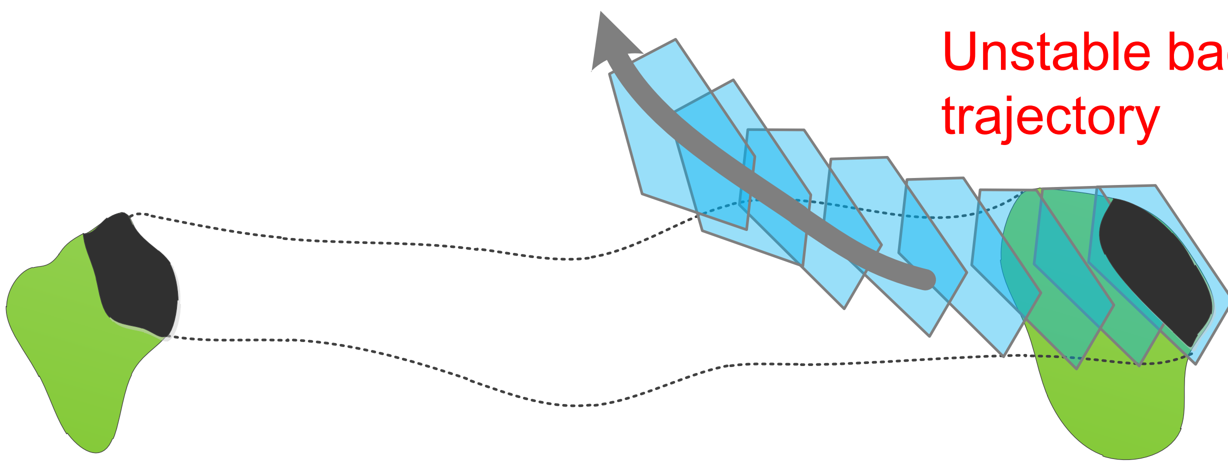


Mirror poles from L-half plane to R-half plane



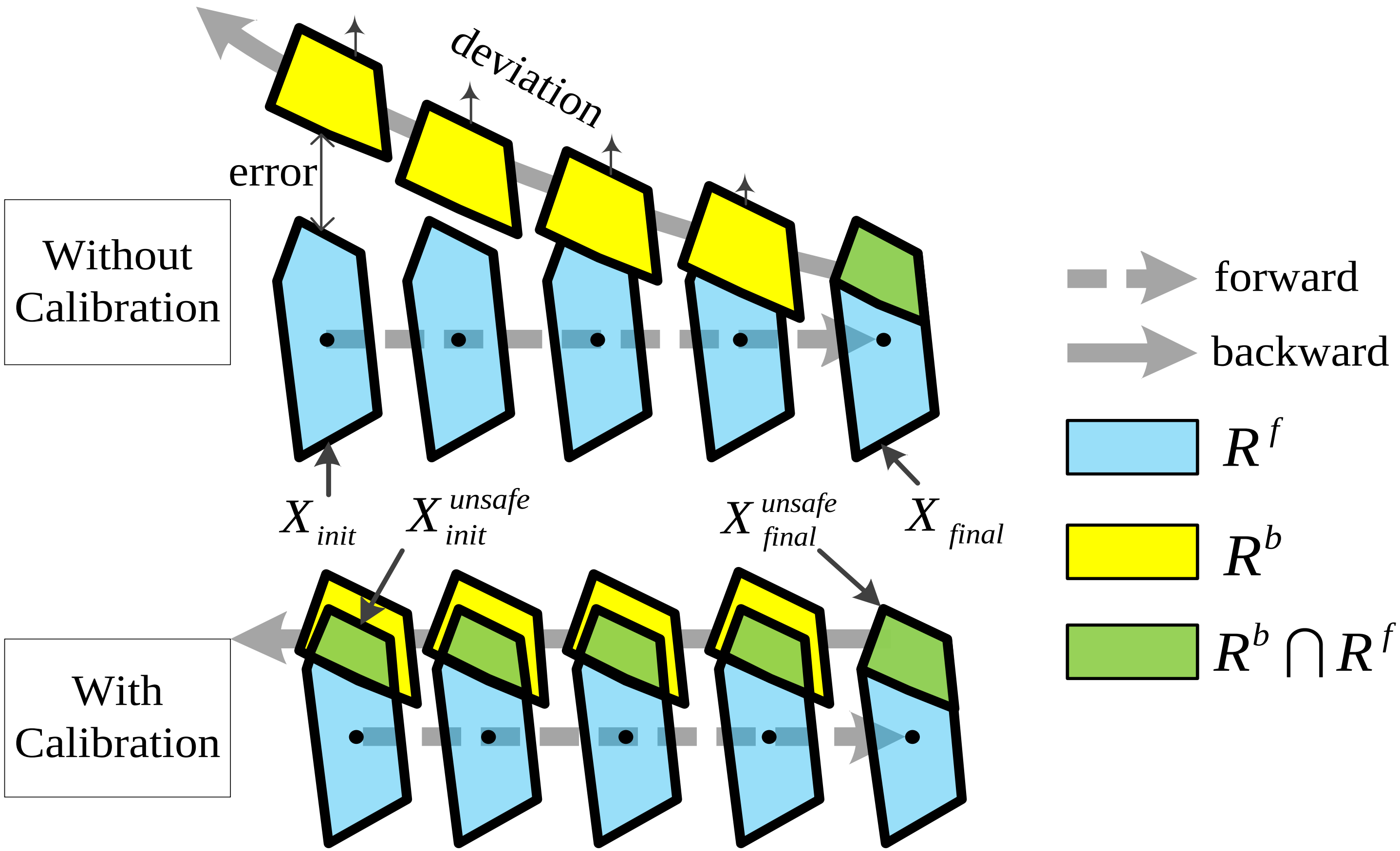
Trajectory difference grows exponentially

1. Over-approximation
2. Estimation of active time of CP



Unstable backward trajectory

Calibration in Backward Correction

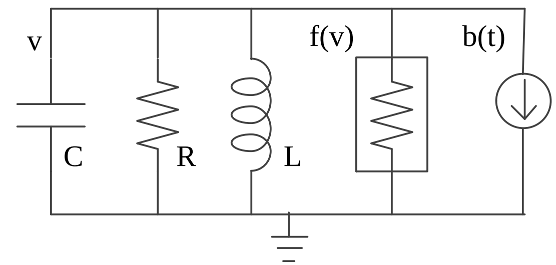


Iteration eq. : $R_{k-1}^b = F^b(\underline{R_k^b \cap R^f})$

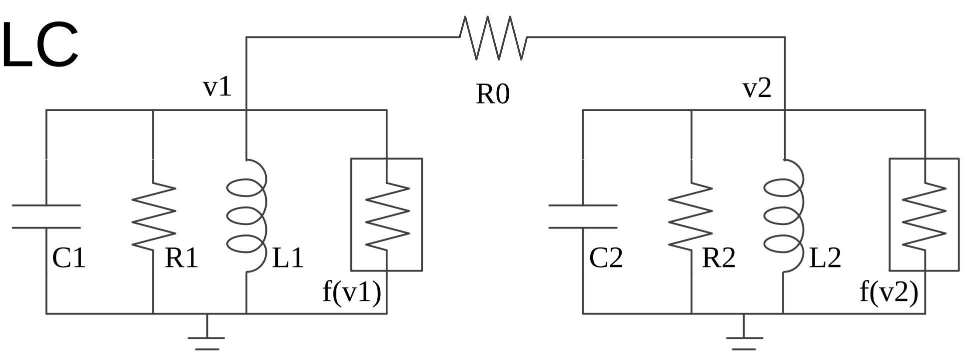
common set

Experimental Results

- Implemented in Matlab
- Platform:
  - Core i5 3.2GHz processor
  - 8GB memory
- Oscillators:
  - Simple LC
  - Resistively coupled LC



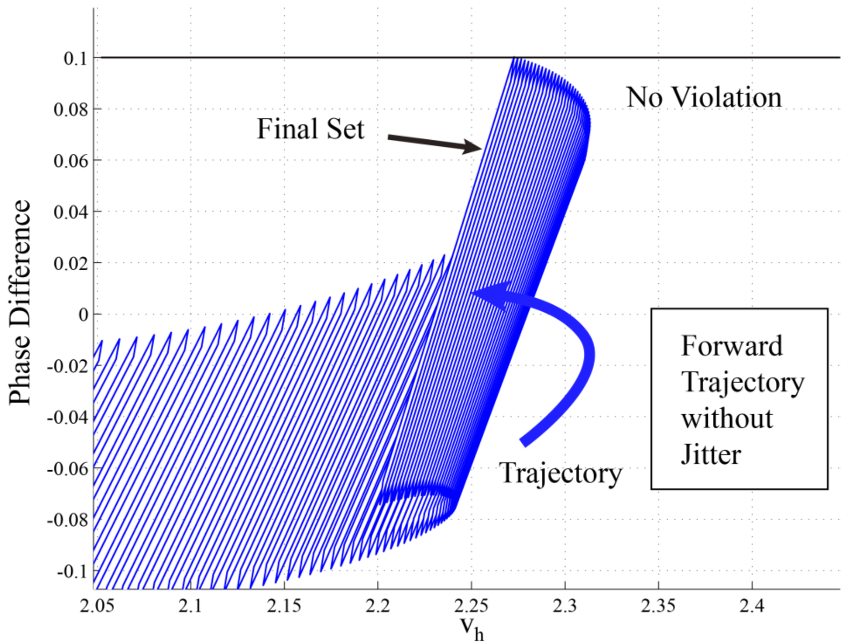
A Simple LC Oscillator



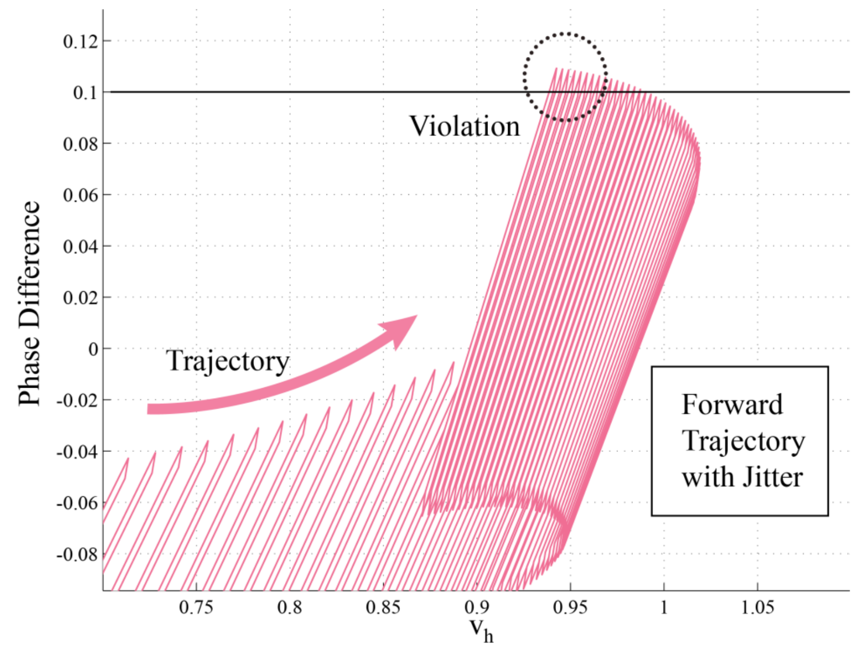
Two Resistively Coupled LC Oscillators

PLL Trajectories with and without Jitter

- Target locking range ($\frac{\phi_v-\phi_{ref}}{2\pi}$) is [-0.1,0.1].
- Suppose phase deviation of $0.01rad$ per simulation step.
- Max. number of simulation cycle is set as 2000.

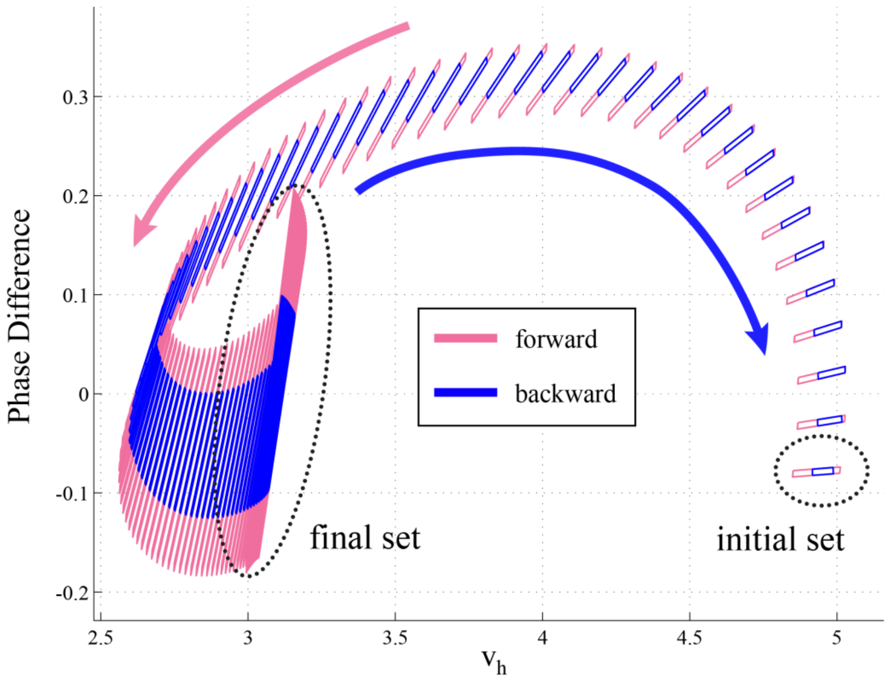


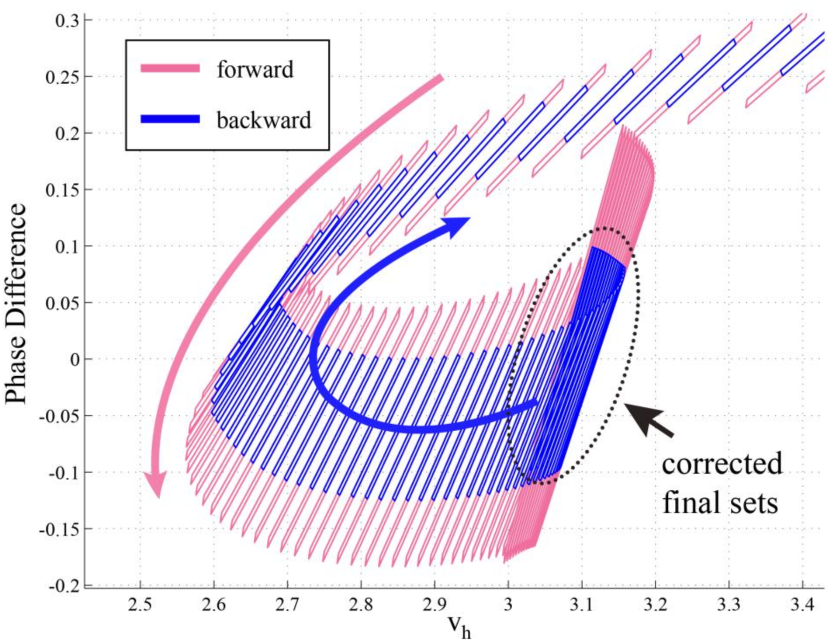
Without Jitter



With Jitter

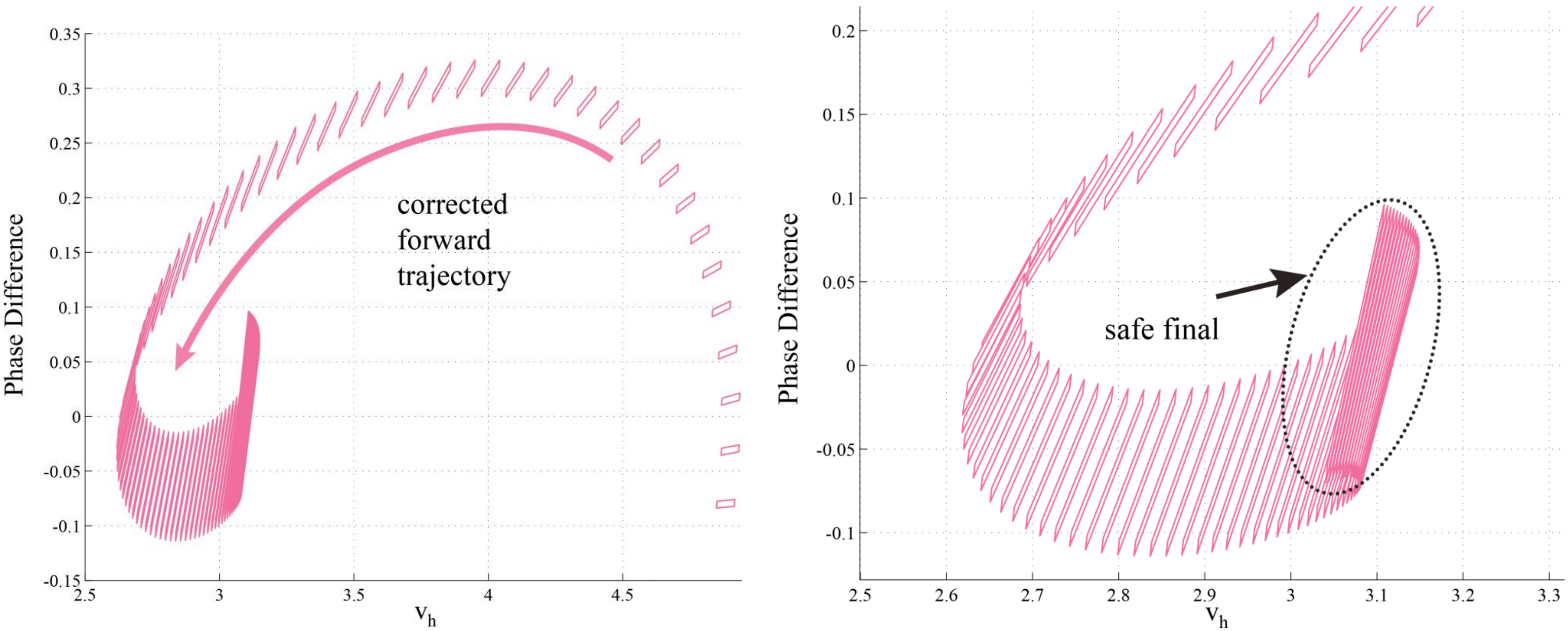
Forward Trajectory





- Start with initial state $v_h \in [4.82, 4.98]$
- End up with final state $(\phi_v - \phi_{ref})/2\pi \in [-0.18, 0.21]$
- Keep corrected final state and trace back to initial state $v_h \in [4.82, 4.89]$

Backward Correction



- Final set after re-run reachability analysis:

$$(\phi_v - \phi_{ref}) / 2\pi \in [-0.07, 0.1]$$

Performance

Oscillator	Iteration	Time(s)	Initial State (vh)	Final State (phase difference)
Simple LC Oscillator	1	202.99	[4.82,4.98]	[-0.18,0.21]
	2	69.98	[4.82,4.89]	**[-0.07,0.10]**
Coupled LC Oscillator	1	187.95	[2.90,3.10]	[-0.22,0.26]
	2	74.68	[2.90,2.96]	**[-0.06,0.09]**

- Phase difference is defined as $(\phi_v - \phi_{ref})/2\pi$
- Aimed locking range is [-0.1,0.1].

Summary

- **Introduced a system behavioral model of PLL with jitter.**
- **Proposed stable backward reachability correction for the verification of PLL phase locking.**
- **Presented a method of calibration to overcome instability of backward correction.**
- **Backward correction helps PLL converge to desired locking range quickly.**

Thank you!

Please send comments to haoyu@ntu.edu.sg

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