Yield Estimation for Analog Circuits based on Performance Bound Analysis

Xue-Xin Liu[1], Adair Palma[1,2], Santiago Rodriguez[1,2],
Sheldon X.-D. Tan[1], Esteban Tlelo-Cuautle[2], Yici Cai[3]

[1]Dept. EE, University of California, Riverside
[2]Institute of Astronomy, Optics, and Electronics, Mexico
[3]Tsinghua University, Beijing, China

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UNIVERSITY OF CALIFORNIA

Outline

- Background
- Review of graph based symbolic analysis
- Optimization based frequency domain bound calculation
- Frequency domain yield estimation
- Experimental results
- Summary

Background

- At the nanometer scale, circuit parameters are no longer truly deterministic and present themselves as probability distributions.
  - Designers must consider these effects to ensure robustness.
- Traditional corner based verification: not accurate enough.
- Monte-Carlo based simulation and yield estimation: general and accurate; but expensive and slow.
- Fast Monte Carlo methods are proposed.
  - important sampling --- circuit specific.
  - Latin hypercube sampling --- doesn’t work for all circuits.
  - Quasi Monte Carlo --- suffers the high-dim problems.

Background

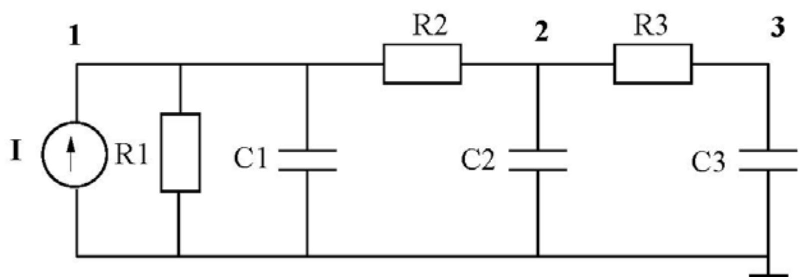
Non MC methods

- Performance bound analysis methods emerged as attractive techniques for statistical analysis and yield estimation.
- Recently some frequency domain performance bound methods were proposed to compute the lower and upper bounds of transfer function’s magnitude and phase.
  - [Qian10] applies a control-based method, and [Saibua11] uses an optimization based method.
  - But no systematic method was proposed to obtain variational performance objective functions. In [Hao11], symbolic analysis approach was applied to derive exact transfer functions. However, it uses affine interval method to compute variational transfer functions, which leads to over-conservative results.

Background

- We present a new non MC yield estimation method based on performance bound analysis in freq domain.
- The exact transfer functions of linearized analog circuits are derived via a graph-based symbolic analysis.
- Then freq response bounds of transfer function in terms of magnitude and phase are obtained by nonlinear constrained optimization.
  - It ensures accurate bounds and also resolve the device correlation issues seen in the previous methods.
- It can be easily extended to the time domain bound and yield estimation.
- Experimental results show that the proposed method can achieve one to two orders of magnitudes speedup over HSPICE's MC on benchmark analog circuits.

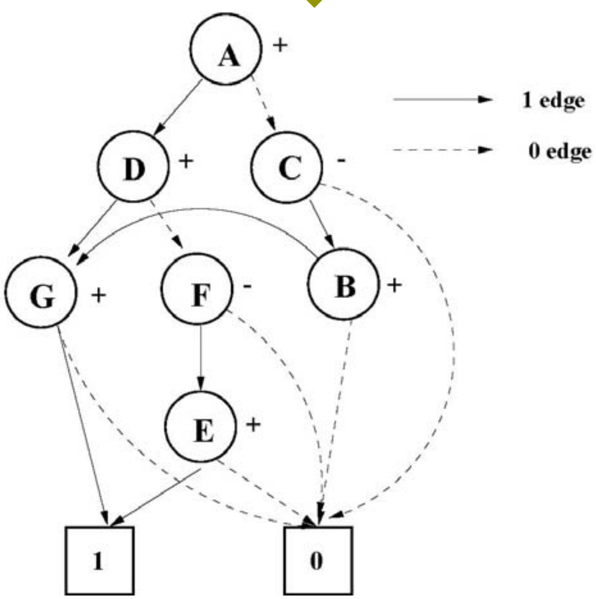
Graph-based symbolic analysis



MNA

$$\begin{vmatrix} A & B & 0 \\ C & D & E \\ 0 & F & G \end{vmatrix} \begin{vmatrix} H \\ I \\ J \end{vmatrix} = \begin{vmatrix} K \\ 0 \\ 0 \end{vmatrix}$$

DDD Creation



DDD Expansion

Symbolic transfer function

$$H(s) = \frac{N(s)}{D(s)} = \frac{\sum_{i=0}^{m} \hat{a}_i s^i}{\sum_{j=0}^{n} \hat{b}_j s^j}$$

- Parametric frequency response
- Good for interactive design aid
- DDD is efficient dealing with exponential symbol complexity

Graph-based symbolic analysis

DDD is short for **Determinant Decision Diagram**, a directed binary graph to represent a determinant.

This recursion is used in all numerical evaluation of DDD and frequency response.

$$D(a_i) = a_i \cdot s(a_i) \cdot D_{a_i} + D_{\overline{a}_i}$$

Value of itself

sign

Value of its 1-edge child

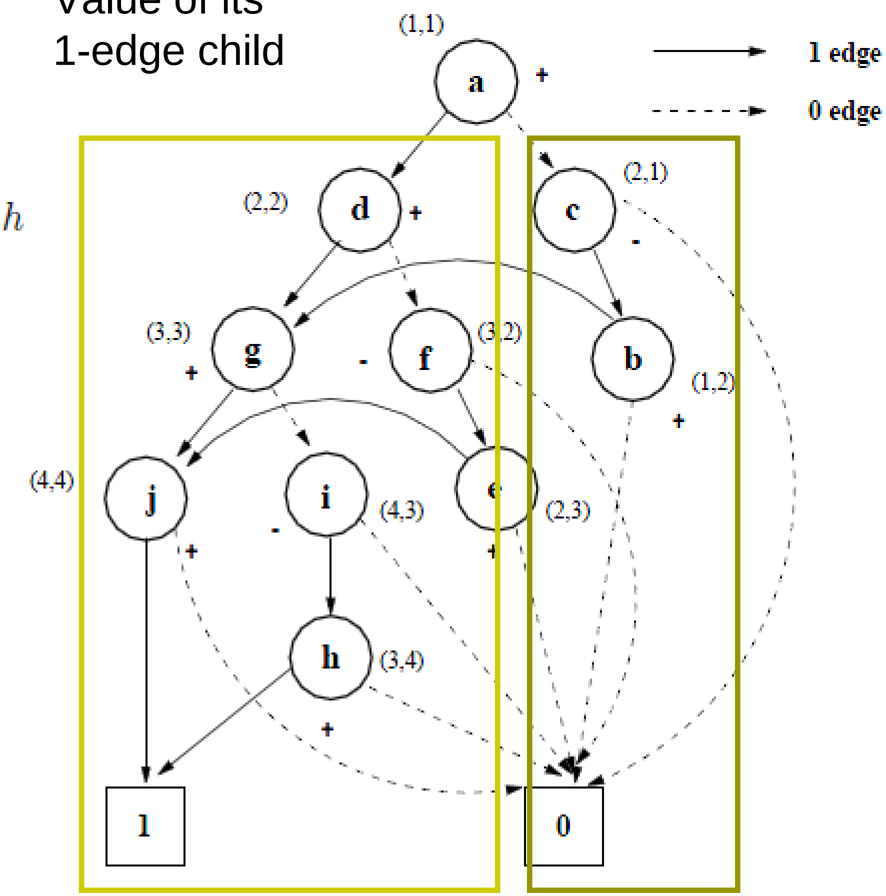
Value of its 0-edge child

$$det(M) = \begin{vmatrix} a & b & 0 & 0 \\ c & d & e & 0 \\ 0 & f & g & h \\ 0 & 0 & i & j \end{vmatrix} = adgj - adhi - aefj - bcgj + cbih$$

$$= \underbrace{\underbrace{a}_{vself}(\overbrace{dgj-dhi-efj}^{\text{Left-subtree}})+c(\overbrace{-bgj+bih}^{\text{Right-subtree}})}_{vtree}$$

$$= a[d(gj-hi)+f(-ej)]+c[b(-gj+ih)]$$

$$= \ldots$$



Graph-based symbolic analysis

- The evaluation of the symbolic expression using nominal design parameters results in nominal transfer function values.
- When parameters are variational, i.e., usually represented in ranges or distributions, both the magnitude and phase are also variational.

nominal design

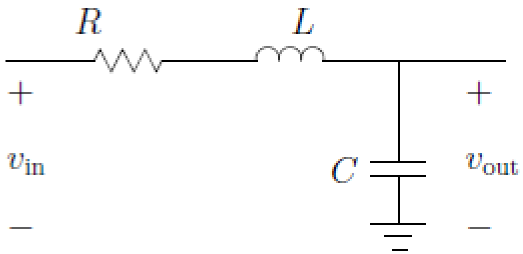
$$\longrightarrow \boxed{H(j\omega) = H(\omega)e^{j\theta(\omega)}} \longrightarrow$$

with process variation

$$\longrightarrow \boxed{\begin{array}{c} H(\omega) \in [H_l(\omega), H_u(\omega)] \\ \theta(\omega) \in [\theta_l(\omega), \theta_u(\omega)] \end{array}} \longrightarrow$$

- Next, we will show the computation of freq domain bounds based on nonlinear constrained optimization.

Computation of freq domain bounds



We first use a simple example to illustrate the computation of bounds.

The transfer function of the series RLC circuit is

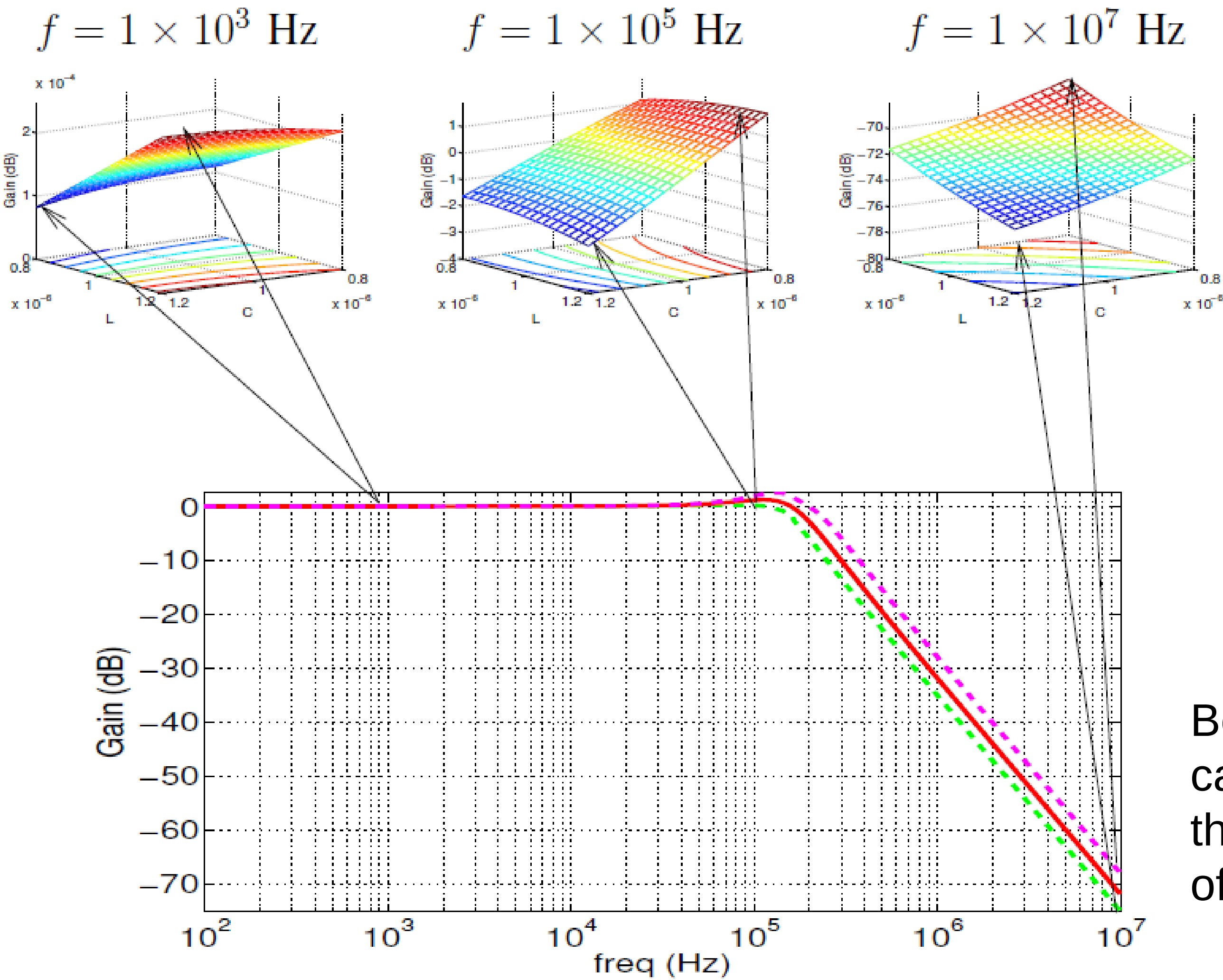
$$H(s) = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{\frac{1}{sC}}{R + sL + \frac{1}{sC}}$$

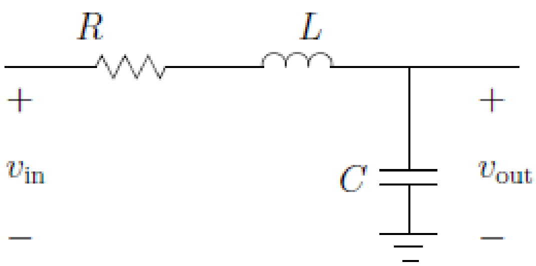
Given its nominal parameters of the resistor, capacitor, and inductor, for example, $R = 1\ \Omega$, $C = 1\ \mu\text{F}$ and $L = 1\ \mu\text{H}$, the nominal magnitude and phase responses can be calculated and plotted straightforwardly.

But how to estimate the bounds if the capacitor and the inductor are 20% variational around nominal values,

$C \in [0.8, 1.2]\ \mu\text{F}$ $\quad L \in [0.8, 1.2]\ \mu\text{H}$?

Computation of freq domain bounds





Both the variations of capacitor and inductor affect the lower and upper bounds of the magnitude.

The lower and upper bounds need to be calculated on all the interested freq points. We formulate each of these calculation into optimization problem.

Computation of freq domain bounds

- To obtain performance bounds for magnitude and phase at one frequency point, four optimization runs are needed: min $|H(j\omega)|$, max $|H(j\omega)|$, min $\angle H(j\omega)$, and max $\angle H(j\omega)$.
- The range of frequency sweep and number of frequency points are determined freely by the designer.
- Take the lower bound of magnitude for example. At freq point ω , a nonlinear constrained optimization is solved.

$$\begin{array}{rl} \text{minimize} & \text{abs}(H(j\omega, \mathbf{x})) \\ \text{subject to} & \mathbf{x}_{\text{lower}} \leq \mathbf{x} \leq \mathbf{x}_{\text{upper}} \end{array}$$

X represent variable values of resistors, capacitors, transconductances, etc., which are subjected to the optimization constraints $[\mathbf{x}_{\text{lower}}, \mathbf{x}_{\text{upper}}]$
In circuit design, these constraints are supplied by foundry measurement and prediction.
Note that the constraints do not have to be limited to circuit parameters. Any functions of them can be used as constraints to which the circuit's behaviors must obey.

Active-set based optimization for computing freq domain bounds

- Solutions to constrained nonlinear optimization problems
  - Active-set method, Interior point method, trust region method
  - Iterative approaches starting with initial guess

- Active set method:
  - Two-phase iterative method
  - First phase, the objective function is ignored while a feasible point is found.
  - Second phase, objective is minimized while feasibility is maintained by method like quadratic programming.
  - But still a localized search method.

Active set is the set of constraints that are satisfied with equality

Computation of freq domain bounds

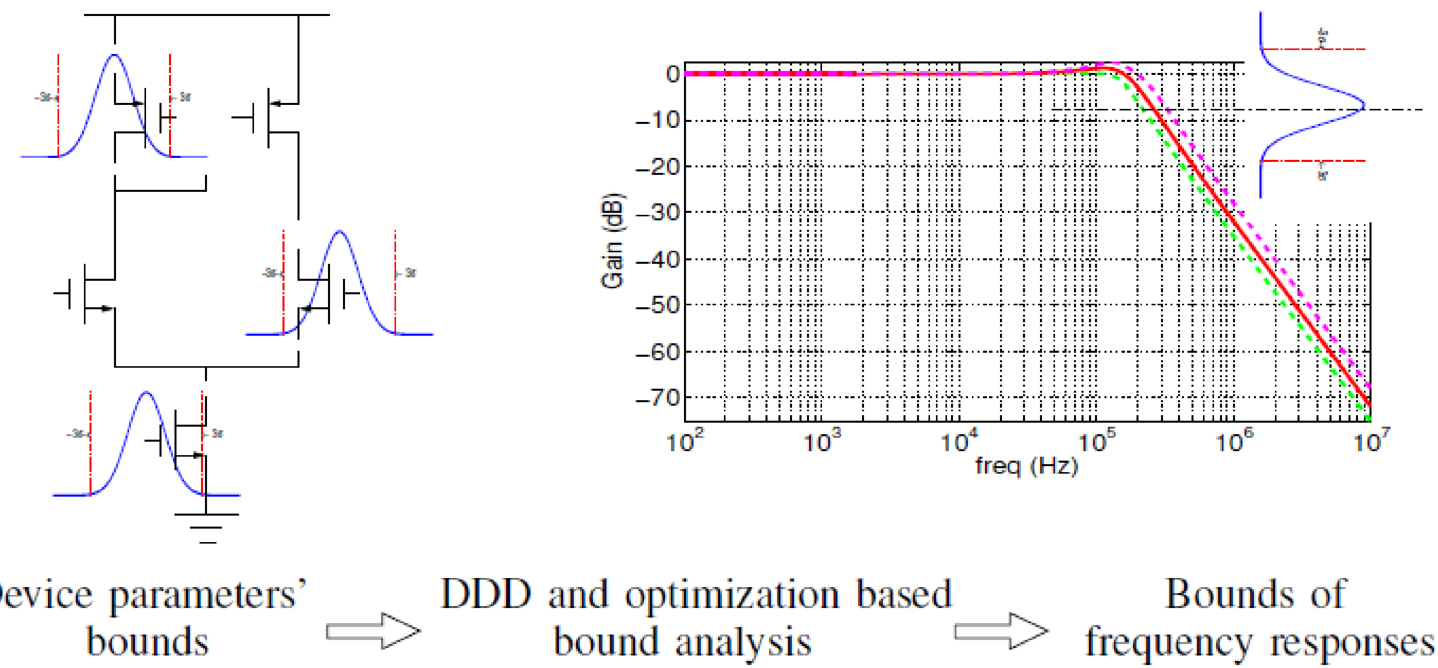
- Since the responses at two neighboring frequency points are usually close to each other, the starting point X for frequency point ω_{i+1} can be set using the solution at the previous frequency point ω_i .
- This strategy tends to reduce the time required by the optimization to search its minimal or maximal point in the whole variable space, and thus speedup the calculation time of the bound analysis.

Yield estimation

- In nanometer level of VLSI technology, designer shall not stop at making the circuits to meet a specification target.
- It is also critical to accurately predict the behavior of the circuits under a range of expected and unexpected conditions, including the process variations among the components.
- Yield analysis helps designers get an insight into the important statistical features.

Yield estimation

- We assume the process variations are Gaussian.
- The characteristic parameters of Gaussian distribution are its mean μ and standard deviation σ.
- In variation aware circuit analysis, the mean value is usually its nominal performance metrics, while the deviation needs to be estimated by statistical method.



Yield estimation

- After our bound analysis, we use the following estimations to calculate the standard deviation at each frequency.

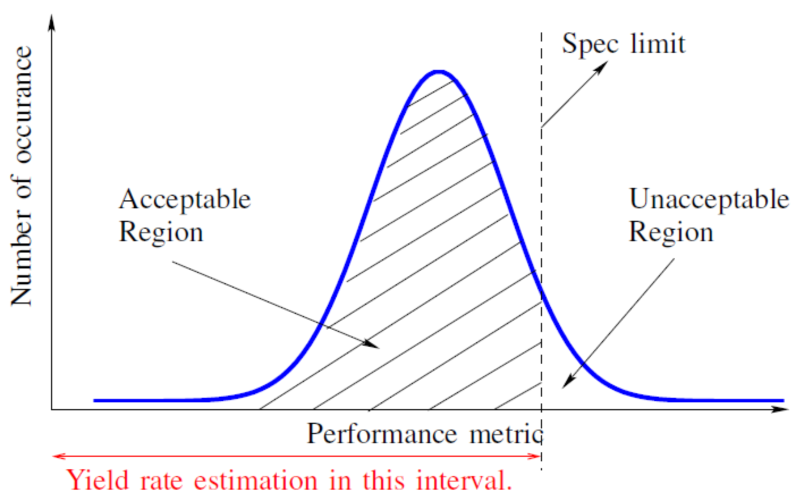
$$\begin{aligned} Y_{\mathrm{u}}(\omega) &= \mu + 3\sigma \\ Y_{\mathrm{l}}(\omega) &= \mu - 3\sigma \end{aligned}$$

- This results in $\sigma = (Y_{\mathrm{u}}(\omega) - Y_{\mathrm{l}}(\omega))/6$
- With mean and std ready, the yield rate can be calculated using cumulative distribution function (CDF),

$$p = \mathrm{normcdf}(Y_{\mathrm{u,spec}}, \mu, \sigma) - \mathrm{normcdf}(Y_{\mathrm{l,spec}}, \mu, \sigma)$$

$$= \frac{1}{\sigma\sqrt{2\pi}} \int_{Y_{\mathrm{l,spec}}}^{Y_{\mathrm{u,spec}}} e^{-\frac{(t-\mu)^2}{2\sigma^2}} \mathrm{d}t,$$

where $Y_{\mathrm{l,spec}}$ and $Y_{\mathrm{u,spec}}$ are preset specifications of allowed performance variations.

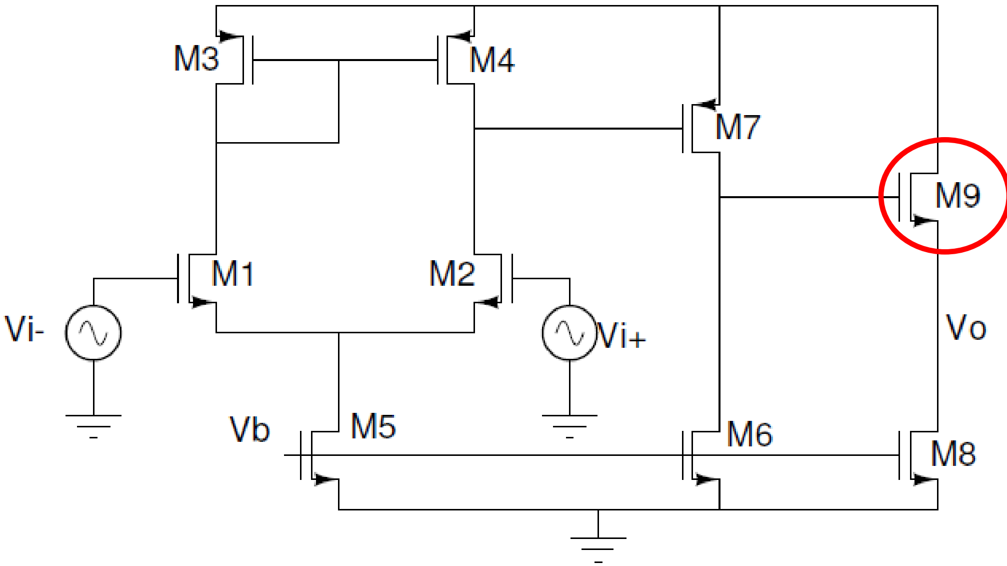


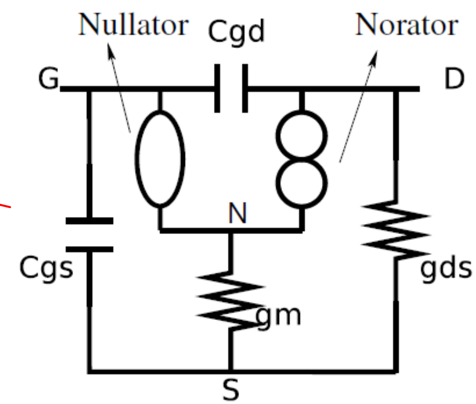
Numerical experiments

Experiment setup

- The proposed bound analysis and yield estimation are implemented using C (the DDD symbolic generation of transfer function) and MATLAB (constrained optimization and all other procedures).
- To test accuracy and efficiency, benchmark circuits are used, such as op-amp and active filter.
  - They are drawn from real designs.
  - Parameter variations are considered.
  - They are generated in SPICE format.
- All experiments are run on a Linux server.
  - 2.4 GHz Intel Xeon quad-core CPU.
  - 36 GBytes memory.

Numerical experiments

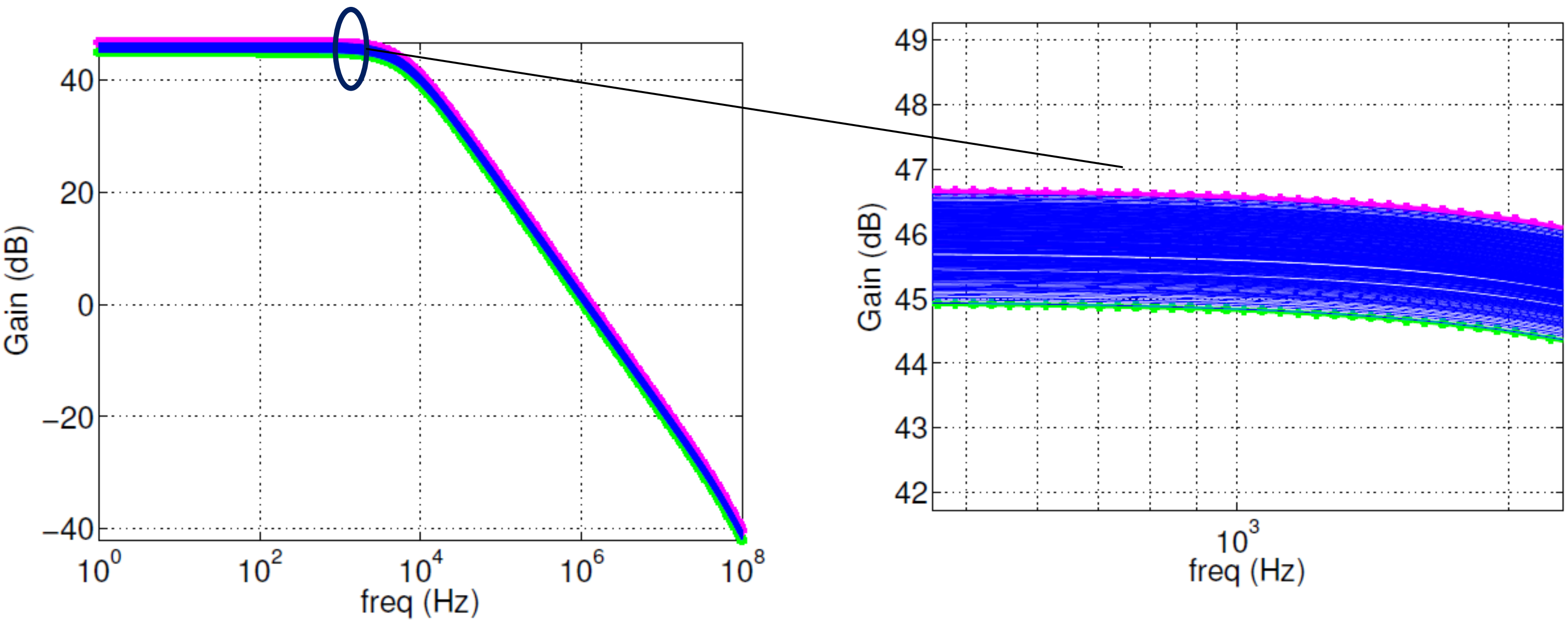




DC analysis is first performed by HSPICE to obtain the operation point, and then small-signal models of nonlinear devices, such as MOS transistors, are used for DDD symbolic analysis and transfer function evaluation.

Nullator doesn't allow current through it and the voltages on its terminals are the same, $V_G = V_N$.
The current generated by the transistor flows only through the resistor gm and the norator as it allows any voltage and any current through it.

Numerical experiments

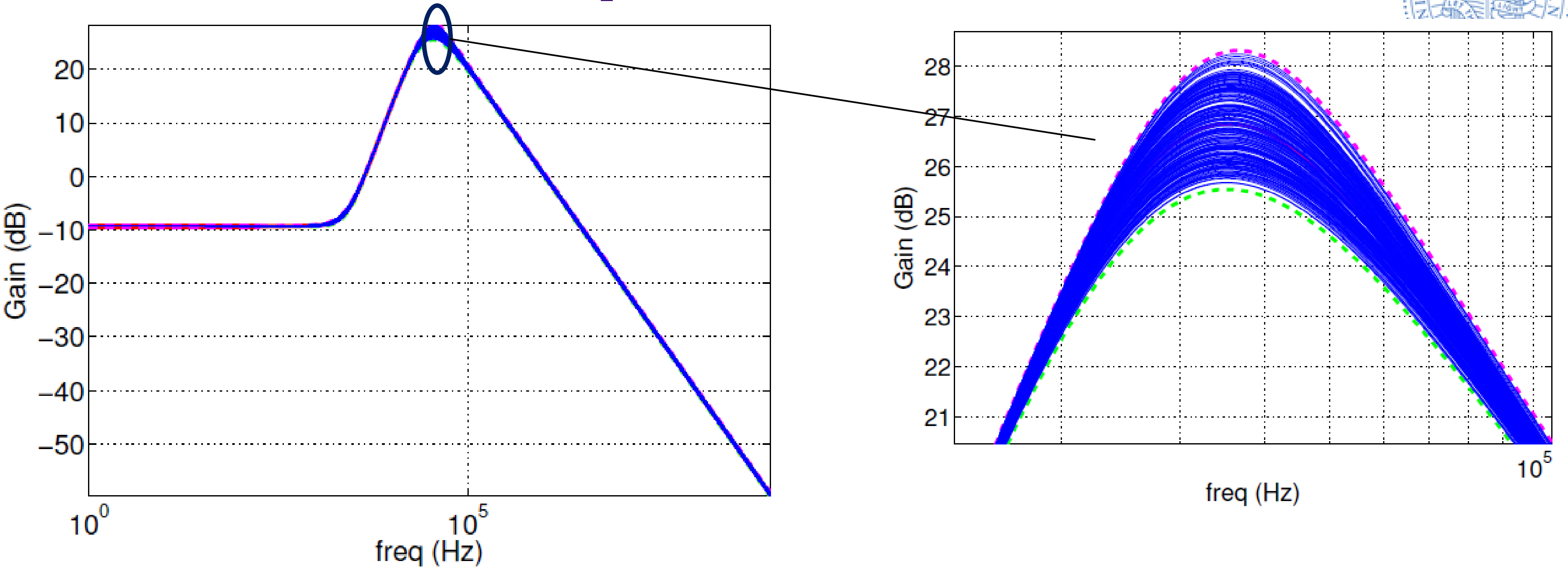


The lower and upper bounds of magnitude response of the op-amp.

The MC results are plotted as thinner blue curves.

We observe that our bounds are accurate and
no over-conservativeness.

Numerical experiments



The lower and upper bounds of magnitude response of the active filter.

Numerical experiments

TABLE I
STATISTICAL INFORMATION OF THE CMOS OP-AMP CIRCUIT.
(COMPARISON WITH 5000 TIMES MONTE CARLO.)

CMOS op-amp		
Runtime (seconds)	MC	85.2
	proposed	3.8
Mean value (μ) Unit: dB	MC	45.8
	proposed	45.8
Std. value (σ) Unit: dB	MC	0.214
	proposed	0.214
Yield rate	MC	98.8%
	proposed	98.4%

TABLE II
STATISTICAL INFORMATION OF THE CMOS FILTER. (COMPARISON WITH 5000 TIMES MONTE CARLO.)

CMOS Filter		
Runtime (seconds)	MC	100.4
	proposed	8.2
Mean value (μ) Unit: dB	MC	26.83
	proposed	26.81
Std. value (σ) Unit: dB	MC	0.389
	proposed	0.384
Yield rate	MC	82.7%
	proposed	84.2%

Summary

- We have proposed a new bound analysis method for analog circuits under process variation.
  - Graph base symbolic technique is used to generate the exact expression of transfer function.
  - The bound computation is formulated using nonlinear constrained optimization.
  - Our bounds are accurate and have no over-conservativeness..
- Mean and deviation are estimated based on the bounds we have calculated.
  - To achieve the same accuracy of yield estimation, one or two orders of speedup is achieved compared to MC simulation.

Reference

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