Range and Bitmask Analysis for Hardware Optimization in High-Level Synthesis

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ASP-DAC

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Motivation

- Software programs mostly use standard 32 and 64 bit datatypes to represent variables.
  - However, don't need 32 bits for a loop counter that only counts to 100!
  - Software is over-engineered, which is fine because processor datapaths are fixed-width.
LegUp

- LegUp is an open-source high level synthesis framework built within the llvm compiler framework.
  - C to Verilog (supports CHStone benchmarks).
  - Targets pure HW or processor/accelerator system.
  - Automated verification.
- Developed at the University of Toronto.
- Freely downloadable at legup.eecg.utoronto.ca
Motivation

- High-level-synthesis (HLS) generates hardware from software program.
- Unlike with software, efficiency of that hardware is dependent on bit-level representation of variables.
- Need bitwidth analysis in HLS to generate minimum bit-level representation for each variable.
This work

- Created a new bitmask analysis approach and combined it with existing variable range analysis techniques.
- Built bitwidth analysis pass into LegUp HLS.
Bitwidth Minimization

- Minimize variable bitwidths by propagating constants through the program instructions.
- Variables represented in one of two ways:
Bitwidth Minimization

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Bitwidth Minimization

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  2) As a bitmask of known values (0 or 1), unknowns (?), or sign-extended bits (S).
     e.g. “S?10”
Bitwidth Minimization

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    e.g. “S?10”

Focus of our work
Bitwidth Minimization

- Software program represented as a control dataflow graph (CDFG) of llvm operators.
- Traverse CDFG in forward and backward directions, propagating bitwidths through operators.
- For each llvm operator, we created forward and backward transit functions.
  - e.g Xor, Shl, Ashr, Mul, Div, etc.
Examples

Forward
Examples

Forward
Examples

LShr

00??

0010

AShr

0010

????

Forward
Examples

Forward
Examples

LShr

00??

AShr

SS??

And

Forward

0010

0010

0010
Examples

Forward
Examples

LShr

00??

????

0010

????

0010

????

0010

SS??

????

00?0

????

????

0010

Mul

Forward
Examples

LShr
????
00??

0010

????
0010

????
0010

????
0010

SS??

And

00?0

Mul

????

????

????

????

????

?????

0010

Forward

???????0
Examples

- LShr
  - 00??
- AShr
  - SS??
- And
  - 00?0
- Mul
  - Forward
  - ???0
Examples

LShr

AShr

And

Mul

Backward
Examples

\[ \text{Mul} \]

\[ ???0 \times ??? = ???0 \]

Backward
Examples

\[
\begin{array}{c}
\text{0000} \\
\times \text{????} \\
\text{0000} \\
\text{000000}
\end{array}
\]
Examples

\[ ????0 \]
\[ \times ???0 \]
\[ ????0 \]
\[ ???00 \]
\[ ???000 \]
Examples

\[ ????0 \times ???? =
\\begin{array}{l}
????0 \\
????00 \\
????000 \\
+ ????0000
\\end{array} \]
Examples

\[
\begin{array}{c}
\text{???0} \\
\times \text{???0} \\
\hline
\text{???0} \\
\text{???00} \\
\text{???000} \\
+ \text{???0000} \\
\hline
\text{???0} \\
\end{array}
\]
Examples

\[
\begin{array}{c}
???0 \\
x 0??? \\
\hline
???0 \\
???00 \\
???000 \\
+ 0000000 \\
\hline
???0
\end{array}
\]

Backward
Examples

???

Shl

0010

Xor

???

???

Mul
Examples
Examples

Shl

Xor

Mul

0010

??00

??00
Examples

```
```

```
```
Examples

??00

??00

??00

00??

00??

0010

???

Shl

Xor

Mul
Range vs. Bitmap analysis

Range

0->4  0->3

Add

0->7 (3 bits)
Range vs. Bitmask analysis

**Range**

- 0->4
- 0->3
- 0->7
  - (3 bits)

**Bitmask**

- ???
- 0???
- ????
  - (4 bits)
Range vs. Bitmask analysis

**Range**

- $0 \rightarrow 4$
- $0 \rightarrow 3$
- $0 \rightarrow 7$
  (3 bits)

**Bitmask**

- $???$
- $0??$
  (4 bits)

**WINNER!**
Range vs. Bitmask analysis

Range
0->15
2
0->60 (6 bits)
Range vs. Bitmask analysis

Range

0->15 2

0->60 (6 bits)

Bitmask

???? 10

????00 (4 bits)
Range vs. Bitmask analysis

Range
0->15
2
0->60
(6 bits)

Bitmask
????
10
????00
(4 bits)

WINNER!
Range vs. Bitmask analysis

Range and bitmask analyses are complementary
Experimental Methodology

- Target Altera Cyclone II FPGAs.
- Used 10 CHStone benchmarks
  - All circuits were simulated after bitwidth reduction using ModelSim and golden inputs provided with CHStone to verify correct functionality.
Experimental Methodology

- Bitwidth analysis LLVM pass.
  - Result: Sum of instruction widths.
Experimental Methodology

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  - Result: Sum of instruction widths.
- LegUp HLS llvm pass uses bitwidth analysis to generate minimized RTL.
Experimental Methodology

- Bitwidth analysis llvm pass.
  - Result: Sum of instruction widths.
- LegUp HLS llvm pass uses bitwidth analysis to generate minimized RTL.
- Quartus generates optimized FPGA implementation.
  - It also minimizes bitwidth!
  - Results: Area in LUTs and registers, speed in Fmax.
Experimental Methodology

- 5 flows
  - Bitmask analysis by itself

- Static bitmask analysis
  - LegUp HLS
    - RTL
    - Altera Quartus
      - Bitwidth results
      - Area and Speed results
Experimental Methodology

- 5 flows
  - Bitmask analysis by itself
  - Range analysis by itself (Campos et. al 2012)
Experimental Methodology

- 5 flows
  - Bitmask analysis by itself
  - Range analysis by itself (Campos et. al 2012)
  - Range & bitmask analysis
Experimental Methodology

- 5 flows
  - Bitmask analysis by itself
  - Range analysis by itself (Campos et. al 2012)
  - Range & Bitmask analysis
  - Profiling-based dynamic range analysis

```
Dynamic range analysis

LegUp HLS

RTL

Altera Quartus

Bitwidth results

Area and Speed results
```
Experimental Methodology

- 5 flows
  - Bitmask analysis by itself
  - Range analysis by itself (Campos et. al 2012)
  - Range & Bitmask analysis
  - Profiling-based dynamic range analysis
  - Profiling-based dynamic range analysis & bitmask analysis
Bitwidth Reduction Results

Percentage Bitwidth Minimization (average)

- Bitmask
- Range
- Bitmask+Range
- Dynamic
- Dynamic+Bitmask

LSBs
MSBs
Bitwidth Reduction Results

Percentage Bitwidth Minimization (average)

- Bitmask
- Range
- Bitmask+Range
- Dynamic
- Dynamic+Bitmask

LSBs vs. MSBs
Bitwidth Reduction Results

![Bar chart showing bitwidth reduction results for different techniques: Bitmask, Range, Bitmask+Range, Dynamic, Dynamic+Bitmask. The x-axis represents the techniques, and the y-axis represents the percentage bitwidth minimization (average). The chart indicates that Bitmask+Range achieves the highest percentage bitwidth minimization, followed by Dynamic+Bitmask.]
## Bitwidth Reduction Results

<table>
<thead>
<tr>
<th></th>
<th>Bitmask</th>
<th>Range</th>
<th>Bitmask+Range</th>
<th>Dynamic</th>
<th>Dynamic+Bitmask</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Percentage</strong></td>
<td>0%</td>
<td>10%</td>
<td>20%</td>
<td>30%</td>
<td>40%</td>
</tr>
<tr>
<td><strong>Bitwidth</strong></td>
<td>50%</td>
<td>60%</td>
<td>70%</td>
<td>80%</td>
<td></td>
</tr>
</tbody>
</table>

The graph shows the average bitwidth minimization percentages for different techniques:

- **Bitmask**
- **Range**
- **Bitmask+Range**
- **Dynamic**
- **Dynamic+Bitmask**

The x-axis represents the different techniques, and the y-axis shows the percentage bitwidth minimization.
Bitwidth Reduction Results

Percentage Bitwidth Minimization (average)

- Bitmask
- Range
- Bitmask+Range
- Dynamic
- Dynamic+Bitmask

Legend:
- LSBs
- MSBs
Area Results

![Bar chart showing percentage reduction for different categories: Static (average), Static (sha), Dynamic (average), Dynamic (adpcm). The categories Static (average) and Static (sha) have a smaller reduction compared to Dynamic (average) and Dynamic (adpcm).]
Area Results

Percentage Reduction

- Static (average)
- Static (sha)
- Dynamic (average)
- Dynamic (adpcm)

LUTs
FFs
Conclusions and Future work

- Opportunities exist to optimize instruction bitwidths in HLS that are not present in RTL synthesis.
  - 9% area improvement over Quartus.
- Using range and bitmask analysis approaches together yields better results than using either in isolation.
- Excellent dynamic range-analysis results show that program information can be used to further reduce area.
  - In hybrid system, minimized HW with SW fallback.
  - User hints for variable use.
Bitwidth minimization will be part of the LegUp 3.0 release. Soon to be available at:

http://legup.eecg.utoronto.ca