The All Programmable SoC FPGA for Networking and Computing in Big Data Infrastructure

Ivo Bolsens,
Senior Vice President & CTO
Moore’s Law: The Technology Pipeline

LOGIC DEVICE ROADMAP

<table>
<thead>
<tr>
<th>V_{dd}</th>
<th>1.0/1.1V</th>
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<tbody>
<tr>
<td>Advanced Gate Stack Engineering</td>
<td>Fully-depleted Channel Electrostatics</td>
<td>Band-Engineered Channel for Enhanced Transport</td>
<td>New Transport &amp; Extreme Channel Electrostatics</td>
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Metal Gate +High-k | Multigate FETs / FDSOI | III/V & Ge channels | Nanowires Tunnel FETs | Novel Materials

2D Quantum Materials, (graphene, topological insulators) spintronics

Tech Node

32/28nm | 14nm | 7nm | 5nm | 10nm | 22/20nm

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Industry Debates on Transistor Cost

The last 50 years of the semiconductor industry have been all about the manifestation of Moore’s Law with regard to the dimensional scaling of Integrated Circuits (ICs). As consumers of electronic devices, we all love to see better products at a lower cost with each and every new product cycle. But now storm clouds are forming.

EE Times
Is the cost reduction associated with IC scaling over?
Zvi Or-Bach, MonolithIC 3D Inc.
7/16/2012 12:20 PM EDT

EXTREME TECH
Nvidia deeply unhappy with TSMC, claims 20nm essentially worthless
Joel Hruska
March 23, 2012 at 12:13 pm
One of the unspoken rules of customer-foundry relations is that you virtually never see the former speak poorly of the latter. Only when things have seriously hit the fan do partners like AMD or Nvidia
28nm = 2x 45nm cost

> $170 M

## Growing Problems for ASIC & ASSP Offerings

### >50% of Top 16 ASSP Vendors Losing Money

<table>
<thead>
<tr>
<th>Communications ASSP Vendors</th>
<th>Operating Margin</th>
<th>2009</th>
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<th>2011</th>
<th>2012 (proj)</th>
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**Source** – Public reports, Xilinx estimates

### Growing ASSP Gaps

- Eroding customer confidence in vendors
- High cost burden from over design for diverse needs
- No ability to differentiate or customize
Trend Mobile Infrastructure: Scalable Platforms

**Capacity**

**Indoor**
- **Residential Femto**
  - 4-16 Users<br>  - <100mW
- **Office**
  - Home
- **Enterprise Femto**
  - 30-60 Users<br>  - <250mW
- **Picocell**
  - 30-200 Users<br>  - <1W
- **Dense Indoor**
  - (Malls, Transport Hubs)

**Outdoor**
- **Macrocell + Active Antennas**
- **Macrocell**
- **Microcell**
- **Urban Infill**
  - ~200 Users/sector<br>  - 20-100W Multi-Sector
- **Wide Area**
  - 2-3x Data Capacity of RRU

**Coverage**
Trend Services: Different Figures of Merit
Trend Wired Infrastructure: Software Defined Networks

Software Defined Networking gains industry mindshare

The best thing about OpenFlow or SDN, is that it’s brought back a new hope to networking. Networking is cool again - Jayshree, CEO - Arista Networks
Trend Data Center Infrastructure: Cloud Computing

Big Data
Increasing Volume, Velocity, and Variety

Low power
Reduce operation and cooling costs

Security
Both outside and inside
Impact of trends
(1) Networking

New network fabrics
• Faster, Fatter, and Flatter

Software defined networking
• Software control plane
• Hardware data plane

Content-aware networking
• Deep packet inspection
• Enhanced security
Impact of trends (2) Compute

ARM-based microservers
  • Improved performance per watt

Hybrid SoC
  • CPU+accelerators+fabric
  • Cost and power reduction

Larger memory
  • Hybrid NVRAM and DRAM
  • Latency reduction
Impact of trends (3) Storage

Specialized functions

- Compression, encryption, memcached

Custom SSD controllers
- Higher performance
- Reduced latency

Data-aware storage
- Integrated database support
- Offload from processor
Future Data Centre Architecture

Internet

"Intelligent Appliances" (router, firewall)

Intelligence in the network
Further convergence
Fewer tiers

New topologies (torus NIC)

Convergence

Low latency NICs

Direct-attached storage

FibreChannel

SAN

Network attached storage
Generic Data Center

- x86
- DRAM
- Coherent Memory Bus
- Memory Bus
- PCIe
- PCIe Fabrics
- 40/80G NIC
- Core Network
- Ethernet
- Switch 100/400G
- Network Attach Storage
- Storage Ctrl
- Storage
- Direct Attach Storage
- NVM
- H:R
- PCIe Fabrics
- I/O Bus and Fabrics
- I/O Bus
- I/O Attach Accel.
- Coherency
- Lowest Latency
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The New Data Center

**Networking**
- Security, DPI
- Low latency switch/bridge
- Custom fabrics
- SDN control plane

**Core Network**

**Ethernet**

**Storage**
- Custom SSD
- Low latency
- Memcache appliance
- Data aware storage
- Encrypt, Compress

**Computing**
- Transcode
- Search / Database
- DSP Filters
- Large Memory
- Hybrid NVM/DRAM

**Networking**
- Fabric
- Bridge
- Node Ctrl
- Coherent Memory Bus

**Networking**
- PCIe
- Fabrics

**Networking**
- NIC
- 40/80G

**Networking**
- Switch
- 100/400G
MACHINES THAT UNDERSTAND

SMART Data Center Revolution
New Opportunities to Control Costs and Increase Strategic Advantage…

Smart wireless networks to the rescue
Carriers are turning toward more intelligent network management…

Smart Factories
For factory management in the future, it will become essential to strive to implement smart capabilities…

The Next Big, Digital Economy; ‘Smart Energy’
The energy market is undergoing a major transformation…

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# Programmable & Smart Across All Markets

<table>
<thead>
<tr>
<th>All Programmable</th>
<th>Smarter</th>
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<tbody>
<tr>
<td>• Multiple Spectrums</td>
<td>• Self Organizing Networks (SON)</td>
</tr>
<tr>
<td>• Multiple Standards (LTE, 3G)</td>
<td>• Cognitive Radio</td>
</tr>
<tr>
<td>• Multiple Levels of QoS</td>
<td>• Smart Antenna</td>
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<tr>
<td>• Network Function Virtualization (NFV)</td>
<td>• Context Aware Network Services</td>
</tr>
<tr>
<td>• Multiple Stds (400Gb etc.)</td>
<td>• Self-Healing Networks</td>
</tr>
<tr>
<td>• Dynamic QoS Provisioning</td>
<td>• Video Caching at the Edge</td>
</tr>
<tr>
<td>• Software Defined Networks (SDN)</td>
<td>• Data Pre-Processing &amp; Analytics</td>
</tr>
<tr>
<td>• Multiple Stds (FCoE, iSCSI ...)</td>
<td>• Virtualized Resource Optimization</td>
</tr>
<tr>
<td>• Config Storage (SAN, NAS, SSD...)</td>
<td>• Intelligent Appliances</td>
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<tr>
<td>• Changing Resolutions (MPixel, Fps)</td>
<td>• Object Detection &amp; Analytics</td>
</tr>
<tr>
<td>• Emerging Video Stds (UHD, 8K/4K)</td>
<td>• Automotive Collision Avoidance</td>
</tr>
<tr>
<td>• Evolving Video Processing Algorithms</td>
<td>• Industrial Machine Vision</td>
</tr>
</tbody>
</table>

- **Wireless Comms**
- **Wired Comms**
- **Data Center**
- **Embedded**
Industry Mandates

Programmable Imperative

Programmable Systems Integration

Insatiable Intelligent Bandwidth
The All Programmable Platform

- Security: Bit level operations
- Packet Processing: Wide Datapaths
- DSP Processing: Pipelined Datapaths
- Graphics Processing: Parallel Micro-Engines
- System Management: Finite State machines

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The Heterogeneous MPSoC

- Heterogeneous
- Connected
- Scalable
- Parallel
- Configurable
The Era of Heterogeneous Processing Unit
The UltraSCALE FPGA SoC
CPU + FPGA Use Models

0. Pipelined datapath
   - HDL programmed

1. Pipelined datapath with SW control
   - CPU sets register values

2. CPU + FPGA co-processing
   - FPGA part of explicit address space

3. CPU + FPGA peer processing
   - Cache Coherency
CPU + FPGA  Evolution

**IO-Connected**

- Processor
- Processor
- Processor
- Processor

Up to 4.2 GB/s Platform Bandwidth

**Coherent**

- Processor
- Processor
- Processor
- Processor

**Integrated**

- ARM
- AXI

QPI

Legend:
- Bi-directional bus
- Unidirectional link

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Complexity of building MPSoC systems

- High-Speed Analog Design
- High-Speed Interface Design
- SOC System Assembly
- DSP Hardware Design
- Software Development

Requires distinct design skills!
Platform IP Integrator

- Build/ Re-Use IP Subsystems
- Link/Assemble Subsystems
- Generate SW Drivers
High Level Synthesis (HLS)

- Create IP from C/C++/System C algorithm specification
- Abstract algorithm verification to the specification level
- Traditional FPGA design experience not required
Quality of Results

**FPGA:** >38 times better performance than DSP video processor

**QOR:** C2FPGA equal to or better than RTL synthesis

**Ease-of-use:** C2FPGA 2x fewer lines of C code than DSP processor
Programming Heterogeneous Multi-core

OpenCL

Hardware / Software partitioning & interfacing

HS-SW Interfacing Domain Specific API

C
Compile / Debug

C-HLS
Accelerator synth

FPGA

Application-Specific

Video codec
Encryption
Packet Processing
FFT
Search

ARM Processor

A9
A9

Commercial Software Ecosystem

Commercial Software Ecosystem

ARM Processor

A9
A9

C
Compile / Debug

HS-SW Interfacing Domain Specific API

C-HLS
Accelerator synth

FPGA

Application-Specific

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HW/SW Design Flow: SW Programmer View

C-compiler \(\rightarrow\) Concurrent SW \(\rightarrow\) C-synthesis

SW-drivers \(\leftrightarrow\) Middleware \(\leftrightarrow\) Libraries

AXI \(\leftrightarrow\) Hardware \(\leftrightarrow\) Wires

CPU \(\leftrightarrow\) Data Movement \(\leftrightarrow\) Interconnect

Memory

Video Codec

Encryption

LTE Modem

Application Programming
Programmable Platform: 
CPU + FPGA Peer Processing

Capabilities
- Coherent Caches for HW
- Coherent Caches for SW
- Coherency Management

Coherency Benefits:
- **Peer Processing**: Direct Cache-2-Cache data movement
- **Latency**: Very low latency access to CPU (FPGA) data
- **Usability**: No SW cache flush needed
Domain Specific Abstractions

Abstraction

Automation

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ZED Board

- Zynq Evaluation and Development Kit
- Low cost Zynq based community board (XC7Z020)
- Partnership between Avnet, Digilent, Xilinx
- Digilent will fulfill academic market for Xilinx University Program

www.ZEDboard.org

Open source SW and IP
- Linux
- Eclipse based IDE
- Vivado HLS: C to FPGA
- Reference designs
Conclusions

- New Markets Require Heterogeneous Multi-Core SoC
- Modern FPGA are All Programmable SoC
- Software Centric Design Flow Becoming Possible
- Democratizing SoC Design: Targeted Teaching Platform