Call for Papers
ASP-DAC 2014

Asia and South Pacific Design Automation Conference 2014

http://www.aspdac.com/aspdac2014/

January 20-23, 2014

Singapore

Aims of the Conference:

ASP-DAC 2014 is the nineteenth annual international conference on VLSI design automation in Asia and South Pacific regions, one of the most active regions of design and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC.

Areas of Interest:

Original papers in, but not limited to, the following areas are invited.

Paper Submission Deadline:
July 10, 2013, 5:00 PM JST (UTC +09:00)

[1] System-Level Modeling and Simulation/Verification:
System-level modeling, specification, language, performance analysis, system-level simulation/verification, hardware-software co-simulation/co-verification.

[2] System-Level Synthesis and Optimization:
System-on-chip and multi-processor SoC (MPSoC) design methodology, hardware-software partitioning, hardware-software co-design, IP/platform-based design, application-specific instruction-set processor (ASIP) synthesis, low power system design.

[3] System-Level Memory/Communication Design and Networks on Chip:
Communication-based architecture design, network-on-chip (NoC) design methodologies and CAD, interface synthesis, system communication architecture, memory architecture, low power communication design.

[4] Embedded and Real-Time Systems:
Embedded system design, real-time system design, OS, middleware, compilation techniques, memory/cache optimization, interfacing and software issues, *with focuses on integration on or real-time properties to embedded systems*.

[5] High-Level/Behavioral/Logic Synthesis and Optimization:
High-Level/behavioral/RTL synthesis, technology-independent optimization, technology mapping, interaction between logic design and layout, sequential and asynchronous logic synthesis, resource scheduling, allocation, synthesis.

[6] Validation and Verification for Behavioral/Logic Design:
Logic simulation, symbolic simulation, formal verification, equivalence checking, transaction-level/RTL/gate-level modeling and validation, assertion-based verification, coverage-analysis, constrained-random testbench generation.

[7] Physical Design:
a. Partitioning, floorplanning, placement, buffer insertion, interconnect planning, post-placement optimization, cell library design, gate sizing, high-level physical design and synthesis.
b. Routing, clock network synthesis, post-routing optimization, layout verification, package/PCB routing.

[8] Timing, Power, Thermal Analysis and Optimization:
Deterministic and statistical static timing analysis, statistical performance analysis and optimization, low power design, power and leakage analysis, power/ground and package analysis and optimization, thermal analysis.

[9] Signal/Power Integrity, Interconnect/Device/Circuit Modeling and Simulation:
Signal/power integrity, clock and bus analysis, interconnect and substrate modeling/extraction, package modeling, device modeling/simulation, circuit simulation, and high-frequency electromagnetic simulation of circuits.

[10] Design for Manufacturability/Yield and Statistical Design:
DFM, DFY, CAD support for OPC and RET, variability analysis, yield analysis and optimization, reliability analysis, design for resilience and robustness, cell library design, design fabrics.

[11] Test and Design for Testability:
Testable design, fault modeling, ATPG, BIST and DFT, memory test and repair, core and system test, delay test, analog and mixed signal test.

[12] Analog, RF and Mixed Signal Design and CAD:
Analog/RF synthesis, analog layout, verification and simulation techniques, noise analysis, mixed-signal design considerations.

[13] Emerging Technologies and Applications
a. EDA and Design Methodologies for Emerging Technologies: Nanotechnology, quantum devices, emerging memory technologies, molecular electronics, CNT, optical interconnect, 3D integration, probabilistic computing, spin logic.
b. Emerging Applications: Multimedia, consumer electronics, communication, networking, sensor and sensor networks, ubiquitous computing, biologically-inspired computing, bioelectronics, biomedical applications.

All accepted papers must be presented by one of the authors. IEEE reserves the right to exclude a paper from distribution after the conference (e.g., removal from IEEE Xplore) if the paper is not presented at the conference. Please also note that ASP-DAC will work cooperatively with other conferences and symposia in the field to check for double submission.

Submission of Papers:

Deadline for submission:	**5 PM JST** (UTC+9)	**July 10 (Wed), 2013**
Notification of acceptance:		**Sept. 11 (Wed), 2013**
Deadline for final version:	**5 PM JST** (UTC+9)	**Nov. 11 (Mon), 2013**

For detailed instructions for submission, please refer to the "Authors' Guide" at:
http://www.aspdac.com/aspdac2014/

Panels, Special Sessions, and Tutorials:

Suggestions and proposals are welcome and have to be addressed to the Conference Secretariat (aspdac2014-sec@mls.aspdac.com) no later than May 31 (Fri), 2013.

Prospective Sponsors:

ACM SIGDA, IEEE CASS, IEEE CEDA, Singapore Chapter of IEEE CASS

ASP-DAC2014 Chairs:

General Co-Chairs:
Yong Lian and Yajun Ha (National Univ. of Singapore)
Technical Program Chair:
Nagisa Ishiura (Kwansei Gakuin Univ., Japan)
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Tulika Mitra (National Univ. of Singapore)

Contact: Conference Secretariat: aspdac2014-sec@mls.aspdac.com TPC Secretariat: aspdac2014-tpc@mls.aspdac.com

Call for Designs

University LSI Design Contest
ASP-DAC 2014
http://www.aspdac.com/aspdac2014/
January 20-23, 2014
Singapore

ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE

Aims of the Contest:

As a unique feature of ASP-DAC 2014, the University LSI Design Contest will be held. The aim of the Contest is to encourage education and research on VLSI design at universities and other educational organizations. We solicit designs that fit in one or more of the following categories:

(1) Designed, and actually implemented on chips in universities or other educational organizations during the last two years;
(2) Designs that report actual measurements from implementations;
(3) Innovative design prototypes.

Interesting or excellent designs selected will be honored by providing the opportunities for presentation in a special session at the conference. Award(s) will be given to a few numbers of outstanding designs, selected from those presented at the conference.

Areas of Design:

Application areas or types of circuits of the original LSI circuit designs include (but are not limited to):
(1) Analog, RF and Mixed-Signal Circuits, (2) Digital Signal Processing, (3) Microprocessors.
Methods or technology used for implementation include:
(a) Custom ASIC and Cell-Based LSIs, (b) Gate Arrays, (c) FPGA/PLDs.

Submission of Design Descriptions:

A camera-ready summary is requested to be prepared within 2 pages including figures, tables, and references. It is strongly recommended that the original LSI circuit design measured experimental results and a chip micrograph are included in the summary. Please do not submit the same paper as a regular paper.

Specification of the submission format will be available at **http://www.aspdac.com/aspdac2014/**

Deadline for summary:	5PM JST (UTC+9) Jul. 10 (Wed.), 2013
Notification of acceptance:	Sep. 11 (Wed.), 2013
Deadline for camera-ready:	5PM JST (UTC+9) Nov. 11 (Mon.), 2013

Review:

Submitted designs will be reviewed by the Design Contest Committee in a process similar to the review process for the technical papers. The following criteria will be applied in the selection of designs:
(1) Reliability of design and implementation, (2) Quality of implementation, (3) Performance of the design,
(4) Novelty of application, algorithm, architecture, (5) Others.
Interesting or excellent designs selected will be presented at a special session of the conference.

Presentation:

Shortlisted designs will be presented at a special session of ASP-DAC 2014. A 2-page summary of each design to be presented will be included in the conference proceedings.

Contact Email: aspdac2014-udc@mls.aspdac.com

ASP-DAC 2014 Chairs

General Co-Chairs:	**Yong Lian and Yajun Ha (National University of Singapore)**
Technical Program Chair:	**Nagisa Ishiura (Kwansei Gakuin University, Japan)**
Design Contest Chair:	**Chun Huat Heng (National University of Singapore)**