# A High-Speed and Low-Complexity Lens Distortion Correction Processor for Wide-Angle Cameras

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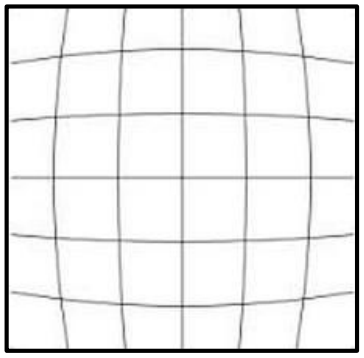
# Background

- **Image sensing systems with a wide-angle camera**

**More images**

**Lens distortion**



**Barrel distortion**

**Distorted image**

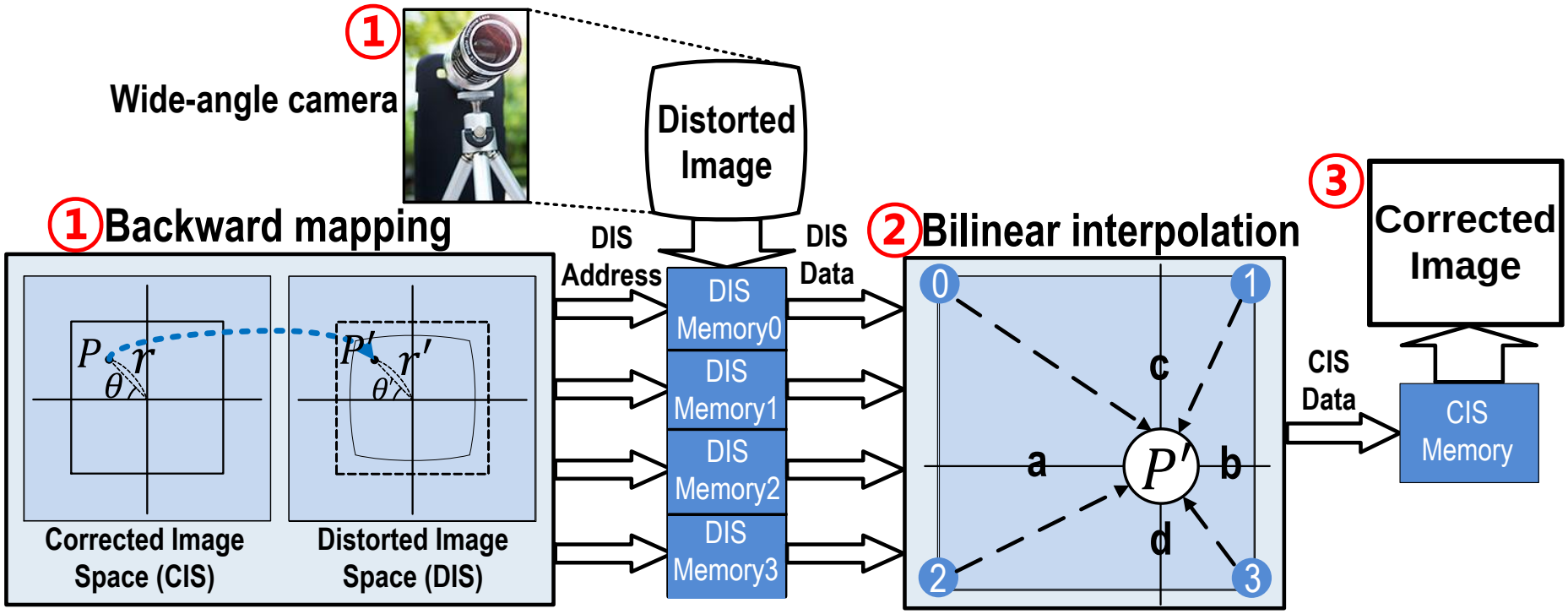
- **Lens Distortion Correction (LDC) processor is required for the image sensing systems.**
  - **High correction speed for the real-time operation**
  - **Low-complexity implementation for the miniaturized low-cost systems**

# LDC Process

- **Backward-mapping-based LDC process**

- **Step 1 : Backward mapping**

- **Step 2 : Interpolation**

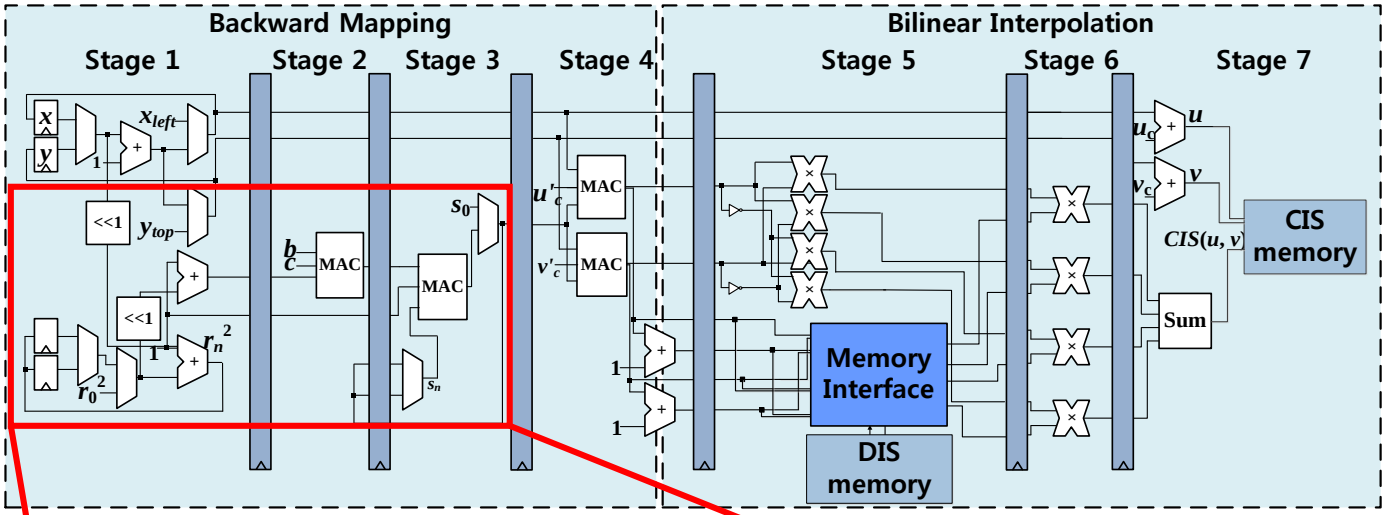



$P' = P \times$ Scaling factor

CIS Data = DIS Data0×b×d + DIS Data1×a×d
+ DIS Data2×b×c + DIS Data3×a×c

# Proposed LDC Processor

## ◆ Low-complexity backward mapping




- 7-stage pipeline
- Stage 1 to 4 : Backward mapping
- Stage 5 to 7 : Bilinear interpolation

**Conventional scaling factor**

$$s_n = a + b \times r_n^2 + c \times r_n^4 \quad (r_n^2 = u^2 + v^2)$$

**Applying the incremental method**

$$s_{n+1} - s_n = (r_{n+1}^2 - r_n^2)\,(b + c(r_{n+1}^2 + r_n^2))$$

$$r_{n+1}^2 - r_n^2 = 2u+1 = \{u,1\}$$

$$r_{n+1}^2 + r_n^2 = 2r_n^2 + 2u + 1 = r_n^2 << 1 + \{u,1\}$$

**Proposed scaling factor**

$$s_{n+1} = s_n + \{u,1\}(b + c(r_n^2 << 1 + \{u,1\}))$$

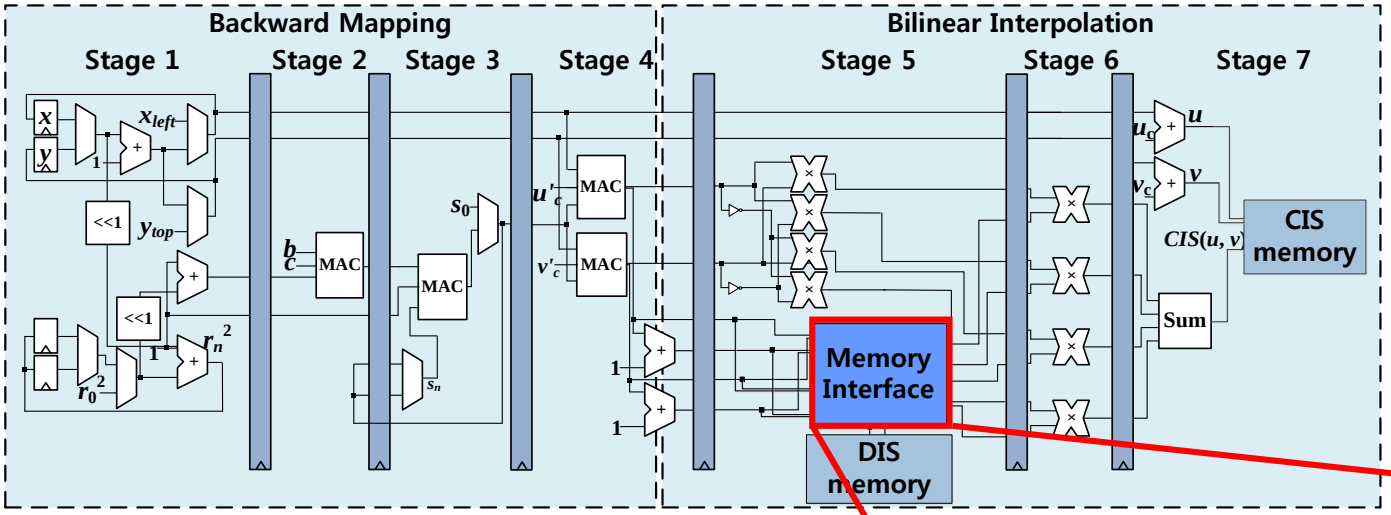
| Architecture | This work | [2] |
|---|---|---|
| 24 bit × 24 bit multiplier | 0 | 7 |
| 24 bit × 16 bit multiplier | 0 | 2 |
| 19 bit × 12 bit multiplier | 1 | 0 |
| 16 bit × 16 bit multiplier | 0 | 2 |
| 12 bit × 11 bit multiplier | 2 | 0 |
| 11 bit × 7 bit multiplier | 1 | 0 |

[2] S. Chen, H. Huang, and C. Luo, "Time multiplexed v… architecture for real-time barrel distortion correction in v… *Trans. Circuits and Systems for Video T…* Nov. 2011.

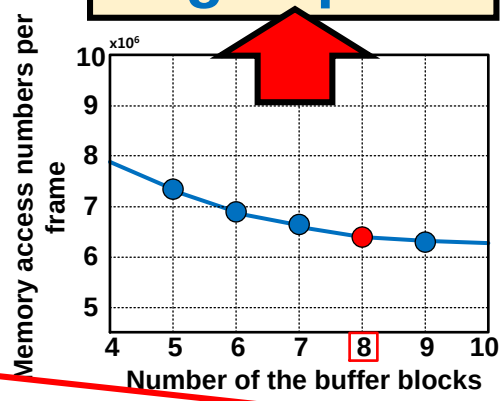
**Low complexity**

# Proposed LDC Processor

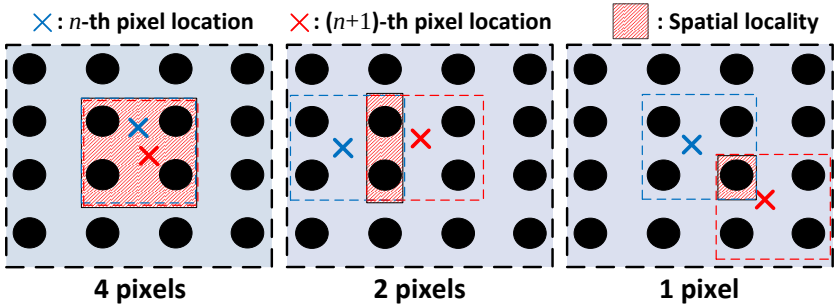
## ◆ Efficient memory interface

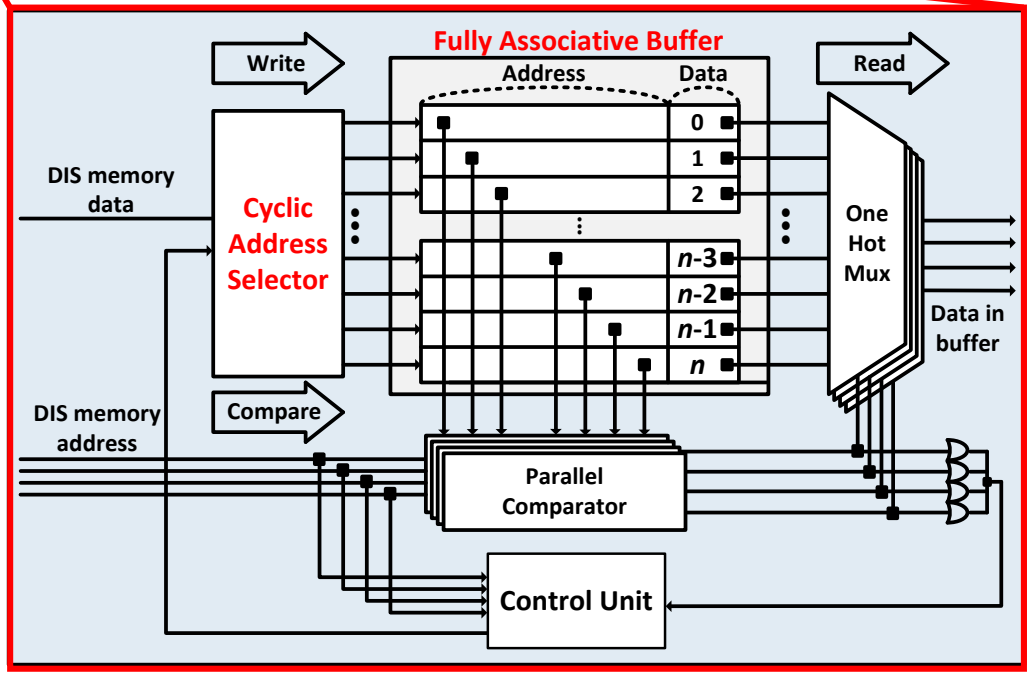



**Low power**
**High speed**




- **Read operations for the bilinear interpolation have the spatial locality.**



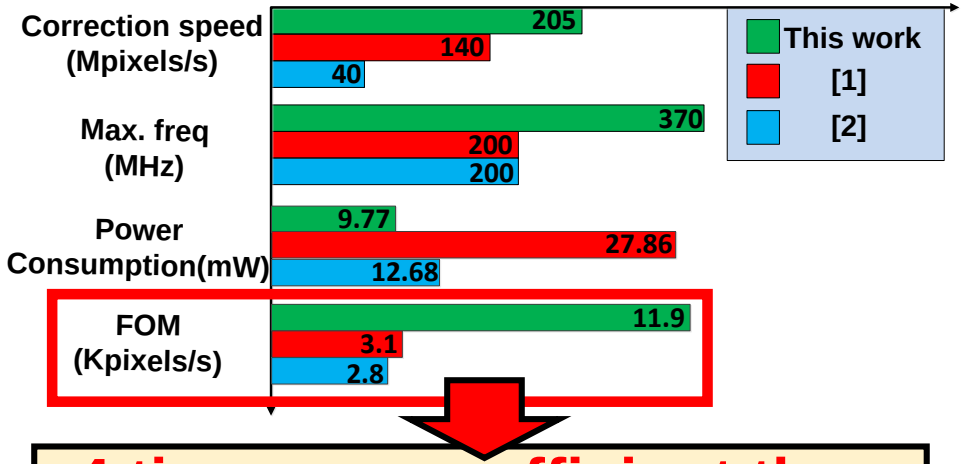



# Results

## ◆ Implementation results

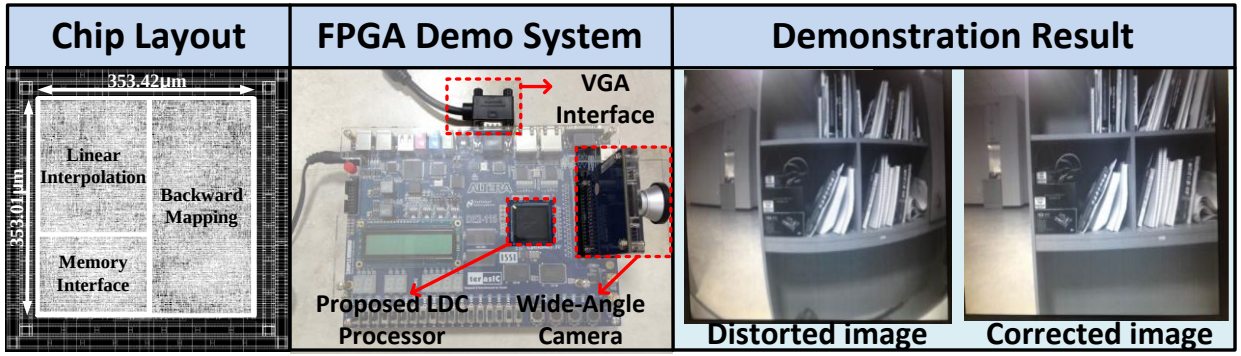
| | This work | [1] | [2] |
|---|---|---|---|
| CMOS technology ($\mu$m) | 0.11 | 0.18 | 0.18 |
| Equivalent gate count[1)] | 17223 | 44992 | 13917 |
| Correction speed (Mpixels/s) | 205 | 140 | 40 |
| Max. frequency (MHz) | 370 | 200 | 200 |
| DIS memory size (byte)[2)] | 4M | 4 x 4M | 4M |
| Maximum supported frame size | 2048 x 2048 | 1024 x 1024 | 1024 x 1024 |
| Power consumption (mW)[3)] | 9.77 | 27.86 | 12.68 |
| FOM (Kpixels/s)[4)] | 11.9 | 3.1 | 2.8 |

1) The smallest 2 input NAND cell is counted as one.
2) 8-bit gray scale, Frame size : 2048 x 2048
3) External memory power (0.11$\mu$m tech. process, single-port synchronous memory, time units : 1 ns)
4) Figure of Merit (FOM) : Correction speed(Mpixels/s)/Equivalent gate count(K)




**4 times more efficient than references in terms of FOM**

## ◆ Chip layout and demonstration result





[1] P. Y. Chen, C. C. Huang, Y. H. Shiau, and Y. T. Chen, "A VLSI implementation of barrel distortion correction for wide-angle camera images," *IEEE Trans. Circuits Syst. II Express Briefs.*, vol. 56, no. 1, pp. 51-55, Jan. 2009.
[2] S. Chen, H. Huang, and C. Luo, "Time multiplexed VLSI architecture for real-time barrel distortion correction in video-endoscopic images," *IEEE Trans. Circuits and Systems for Video Tech.*, Vol. 21, no. 11, pp. 1612-1621, Nov. 2011.