

Lithographic Defect Aware Placement Using Compact Standard Cells Without Inter-cell Margin

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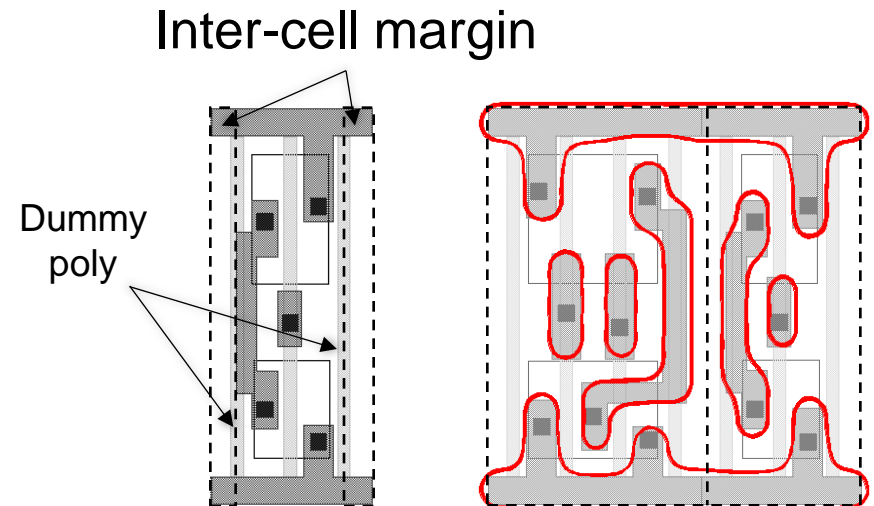
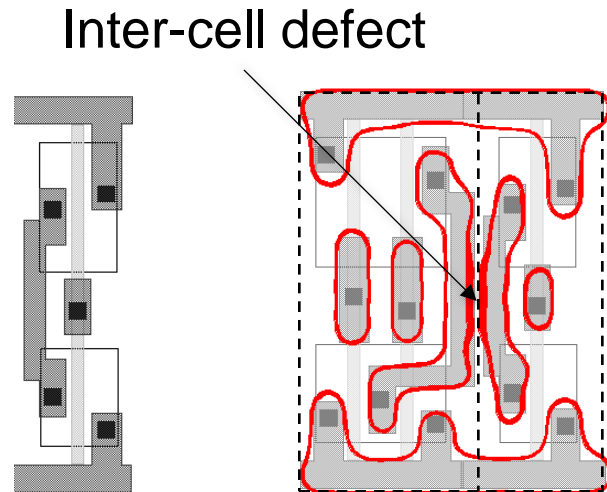
Introduction

Inter-cell defect

- May occur at cell boundary, if no action is taken

Inter-cell margin

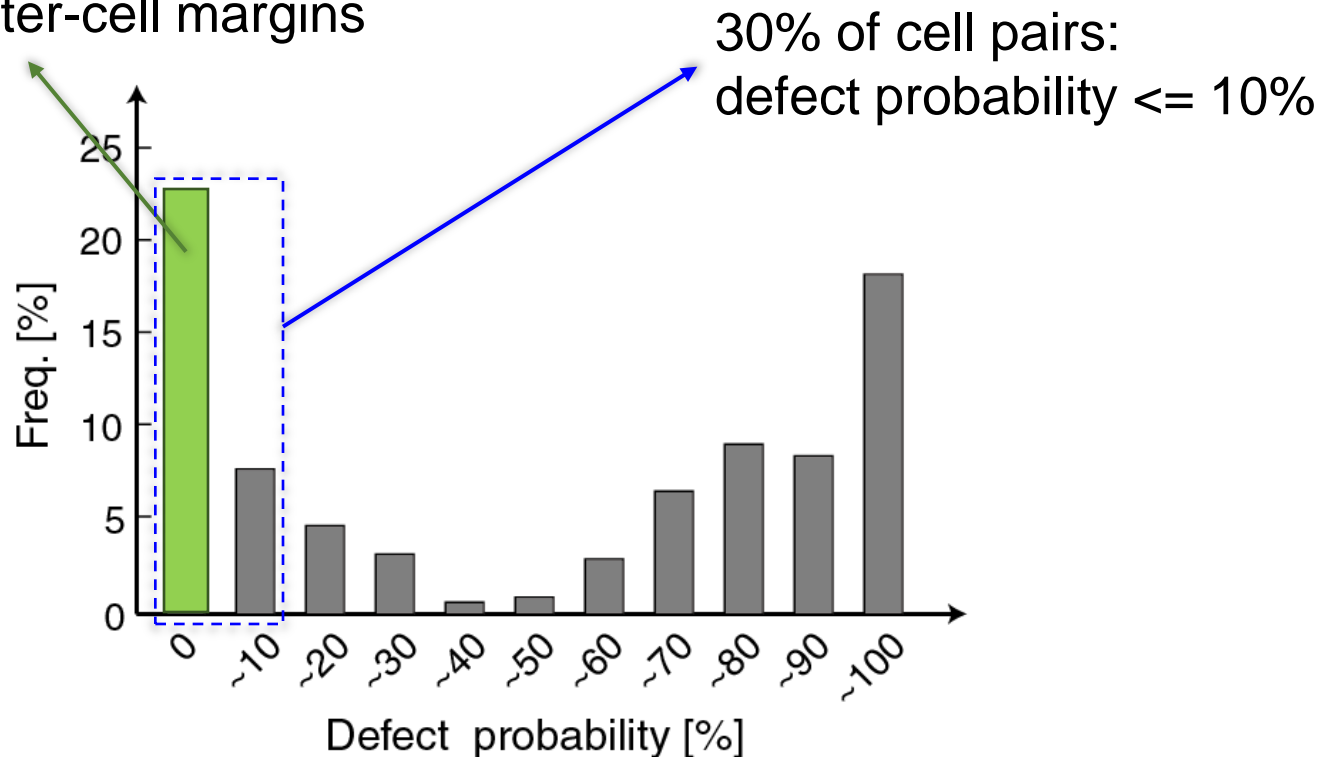
- Extra space at cell boundary with dummy poly
- Causes area overhead



Motivation

What happen if no inter-cell margin at all?

Redundant inter-cell margins



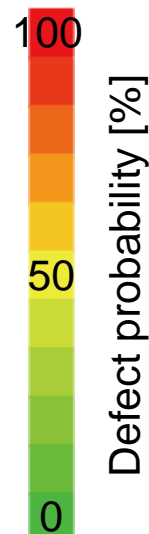
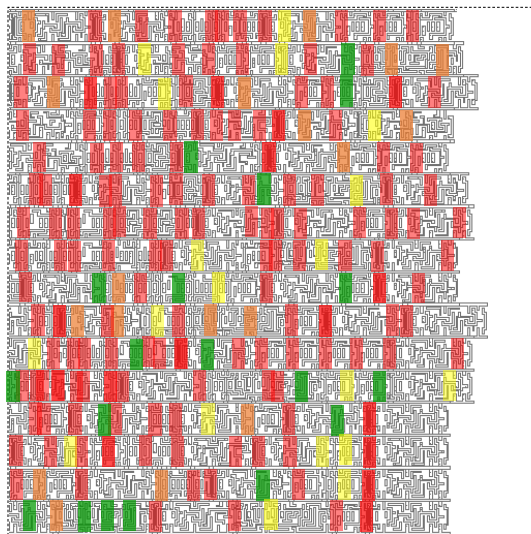
Histogram of defect probability
of all possible cell pairs in 28-nm tech. library

Motivation

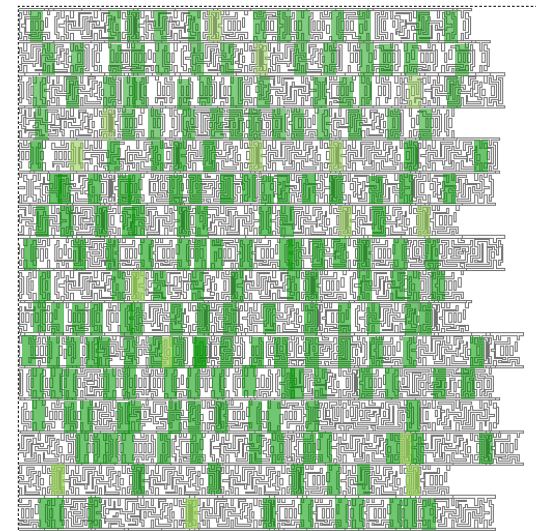
Placement using compact cells without inter-cell margins

- Area saving: ~10%, but cause high defect probability
- **Key problem:** automatic placement while defect probability is taken care

Standard placement
using **compact cells**



New placement
using **compact cells**

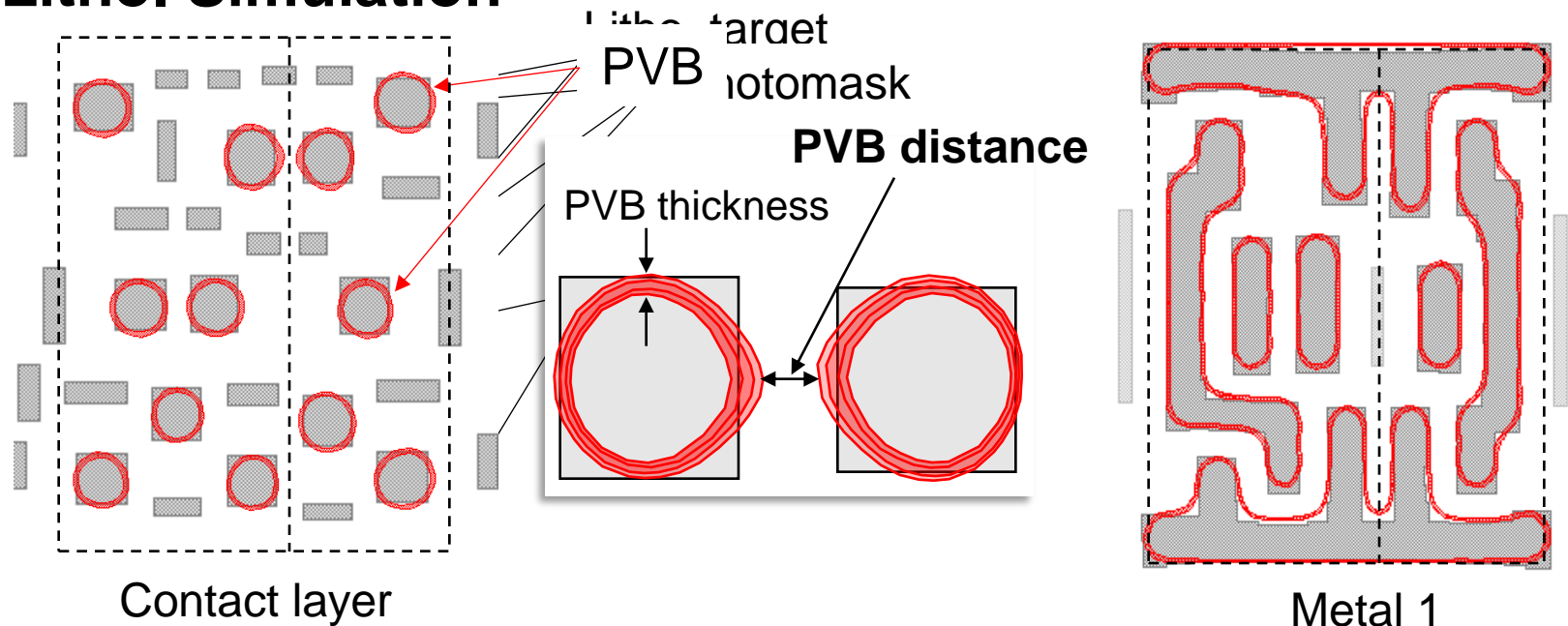


Lithography Simulation

Process variation band (PVB)

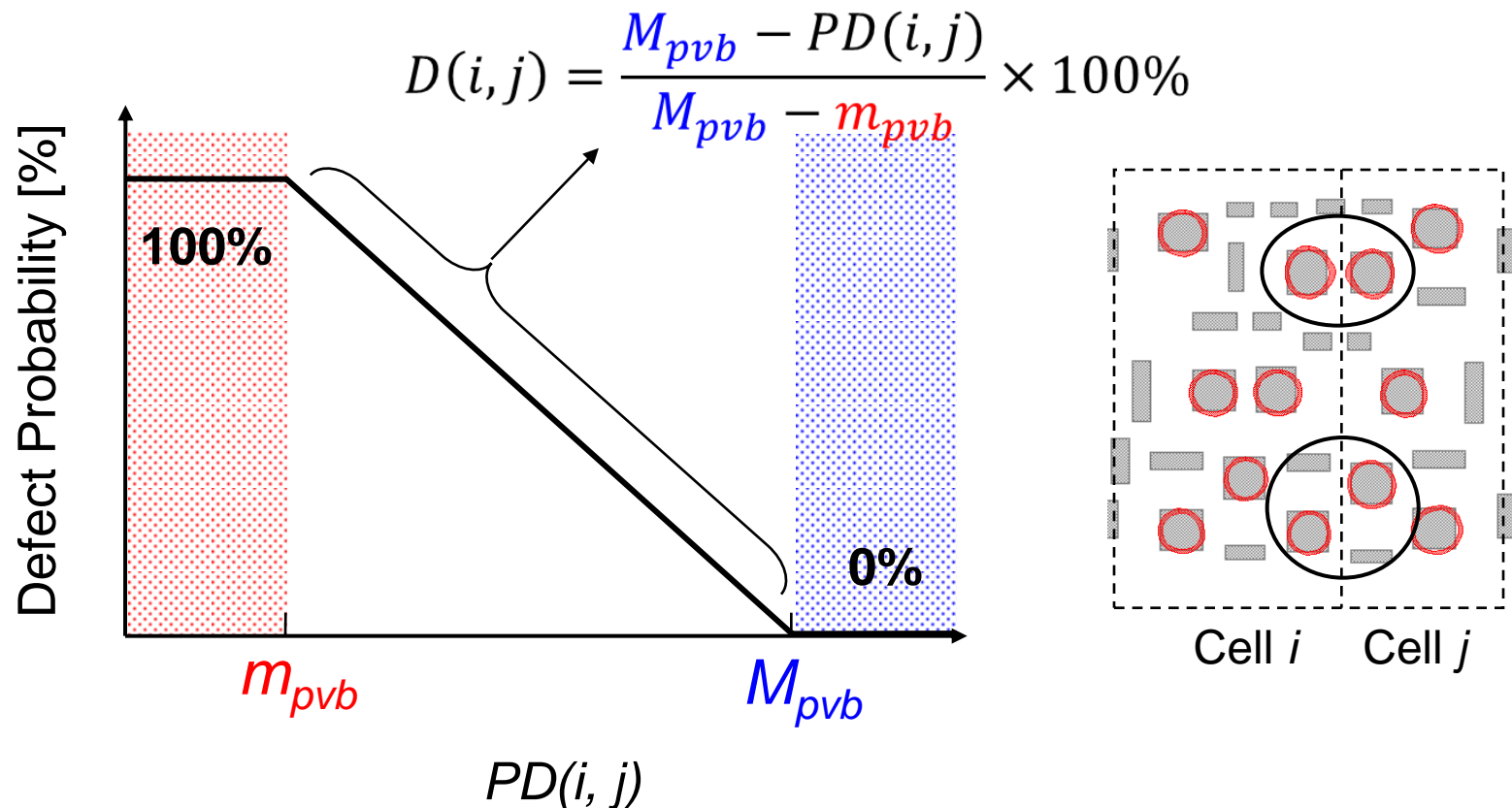
- Made of multiple image contours (@ 27 extreme lithography settings)
- PVB thickness: sensitivity to lithography variations
- **PVB distance (PD)**: criterion of bridging failure (short)

Litho. Simulation



Defect Probability

- $D(i, j)$: defect probability between cells i and j
- $PD(i, j)$: minimum PD along cell boundary
- Maximum value between $D(i, j)$ of contact and metal 1 layer



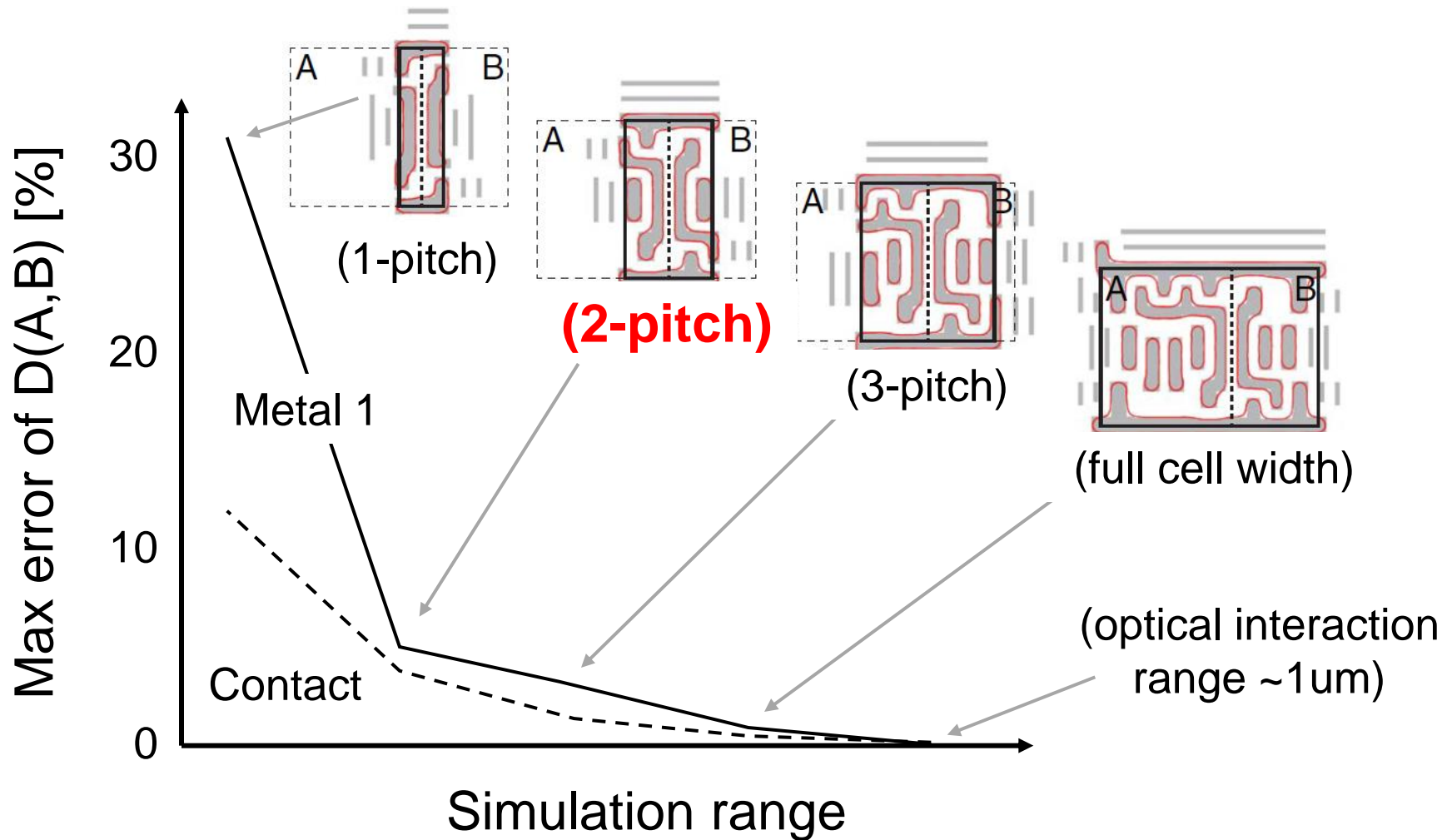
Defect Probability Calculation

Challenge

- One lithography simulation: 0.05 sec
- Lithography simulations for **one cell pair**
 - : $27(\text{litho. settings}) \times 2(\text{contact, metal 1}) \times 0.05 = 2.5 \text{ sec}$
- Total simulation time for **1000 cells**
 - : $(2 \times 1000)^2 \times 2.5 \text{ sec} = \mathbf{100 \text{ days}}$

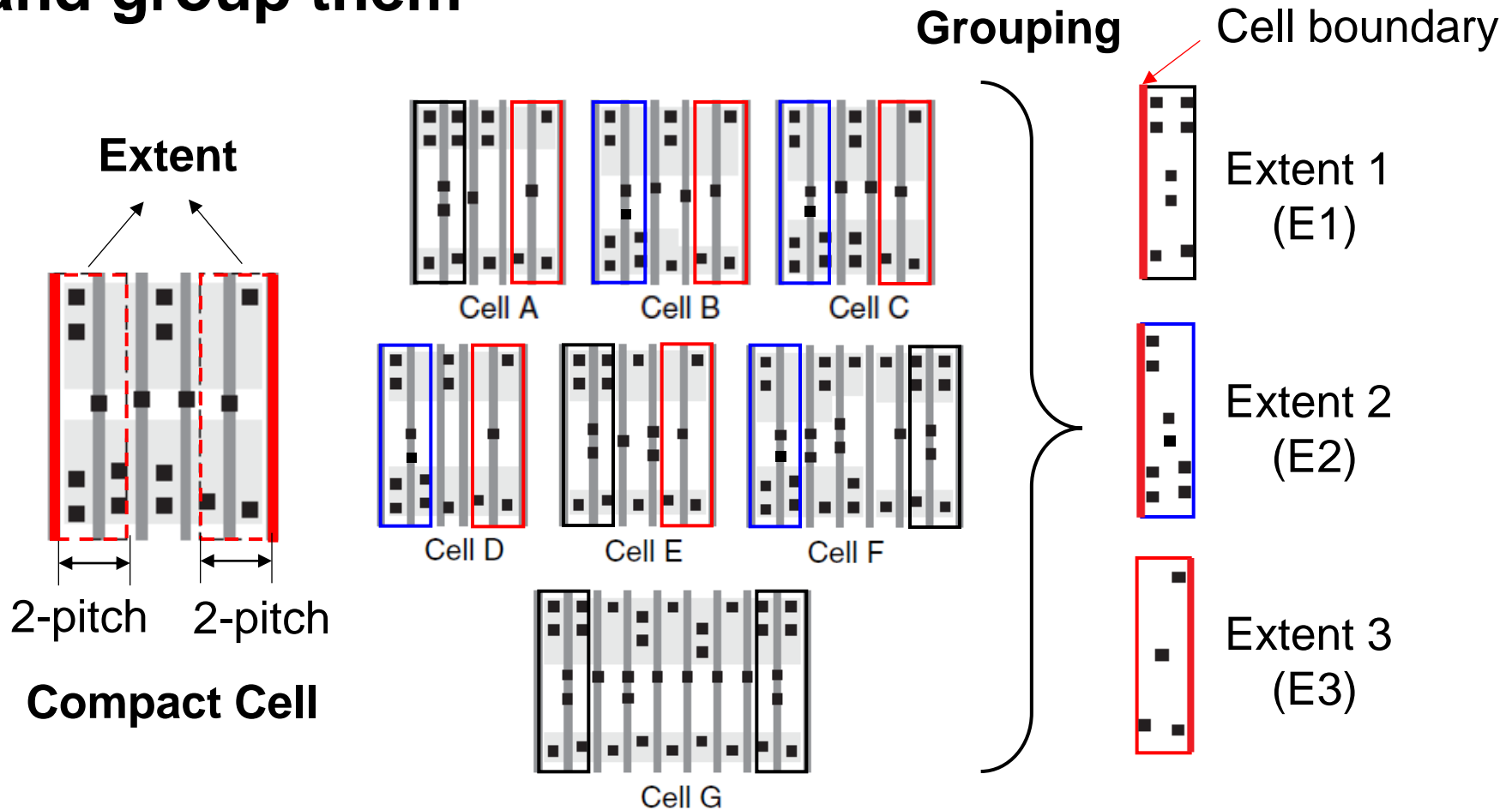
Fast Defect Probability Calculation

Technique 1: reduce simulation range



Fast Defect Probability Calculation

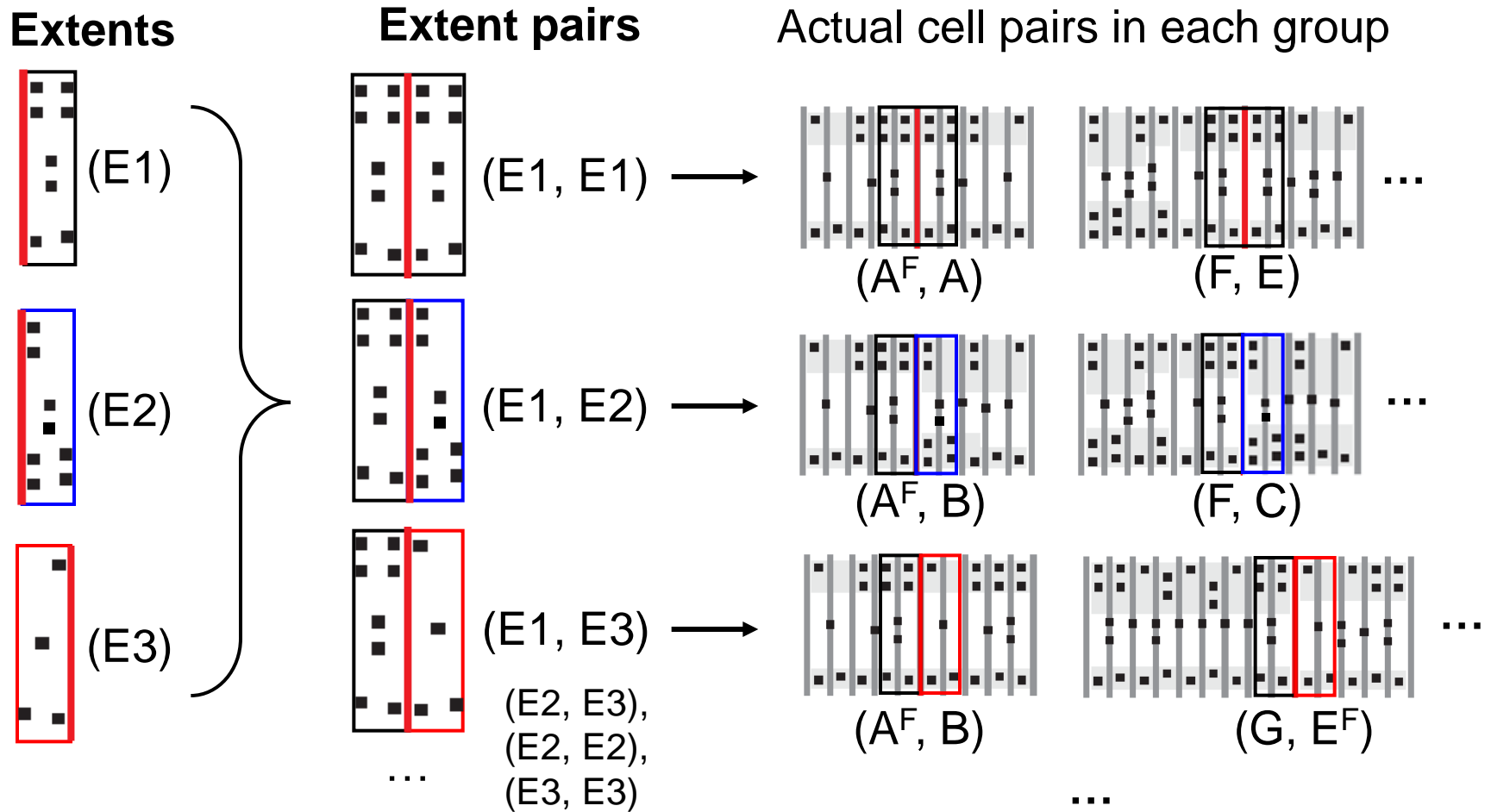
Technique 2: identify patterns along cell boundary and group them



Fast Defect Probability Calculation

Technique 2 (continue)

: Move on to discover extent pairs that exist in actual cell pairs

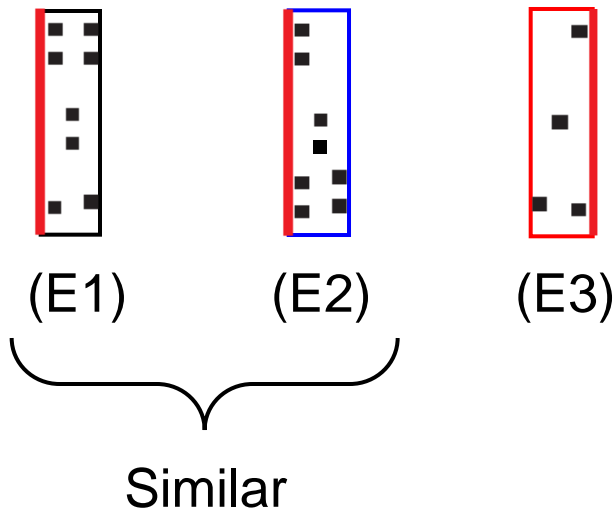


Fast Defect Probability Calculation

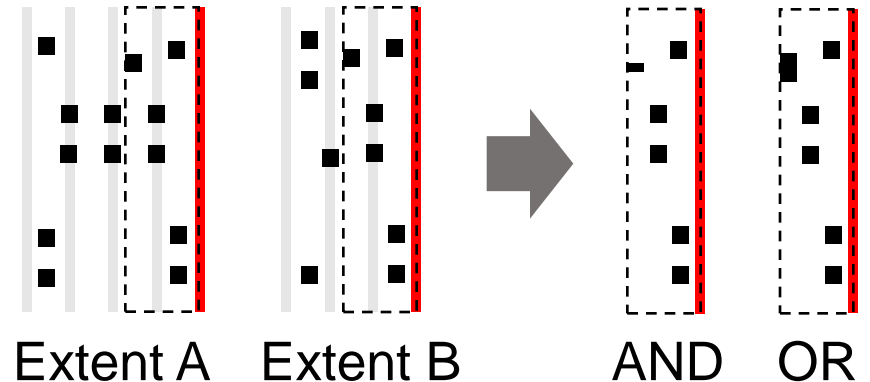
Technique 3: group similar extents

- Reduce # extent groups
- $D(i, j)$ error increases

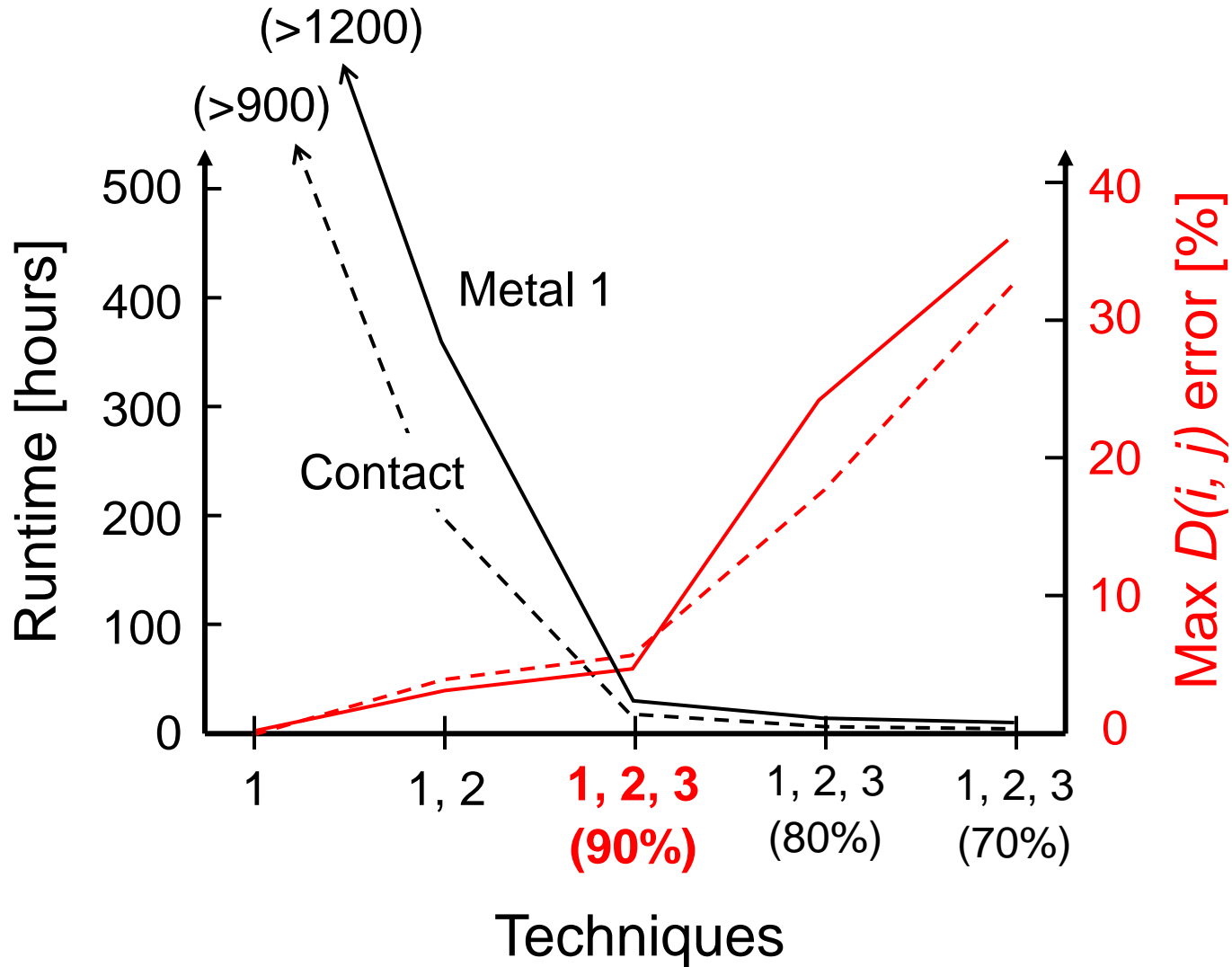
Extents



$$\text{Similarity} = \frac{\text{Area of AND}}{\text{Area of OR}} \times 100\%$$



Result of Fast Calculation

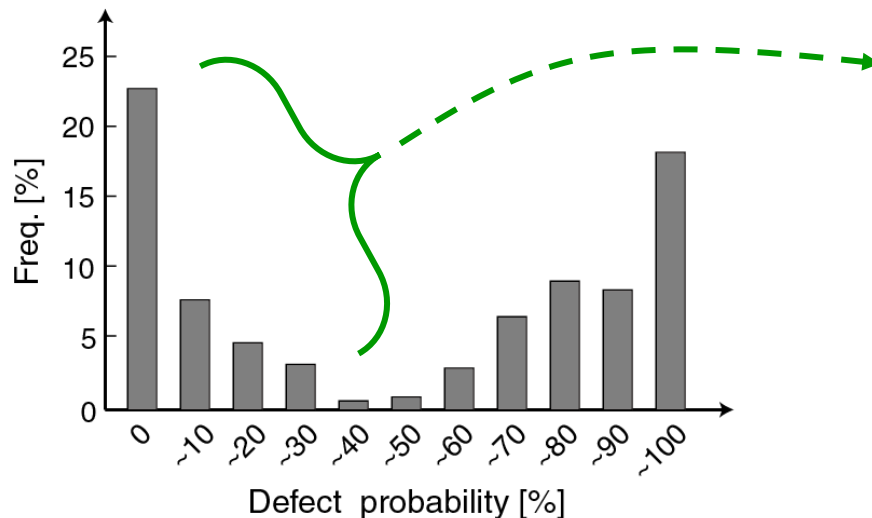


Defect Probability-Aware Placement

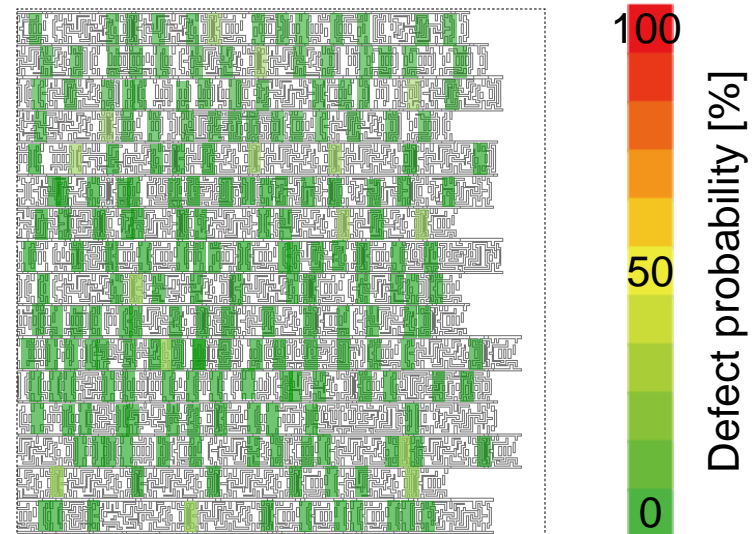
Placement using compact cells without inter-cell margins

- **Key problem:** automatic placement while **average defect probability** and **total wirelength** are **minimized**

Histogram of defect probability of all compact cell pairs



New placement using compact cells



Implementation of Placement

1. Initialization
2. Pre-placement
 - Find values of coefficients in cost function
- 3. SA-based placement**
 - New placement and cost evaluation
 - Acceptance check
4. Whitespace injection

Cost function

$$\Gamma = \alpha C_w + \beta C_r + \gamma C_d$$

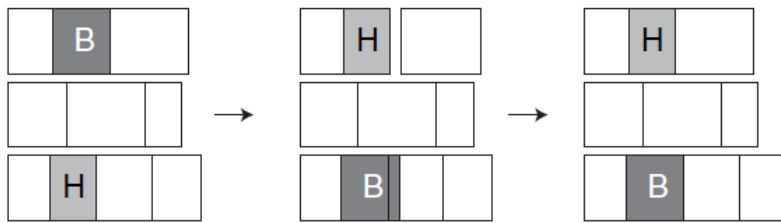
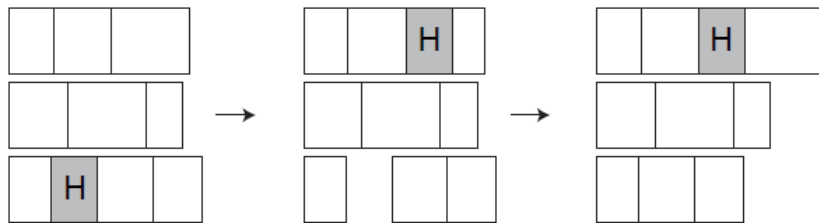
Wirelength

Whitespace

Defect
probability

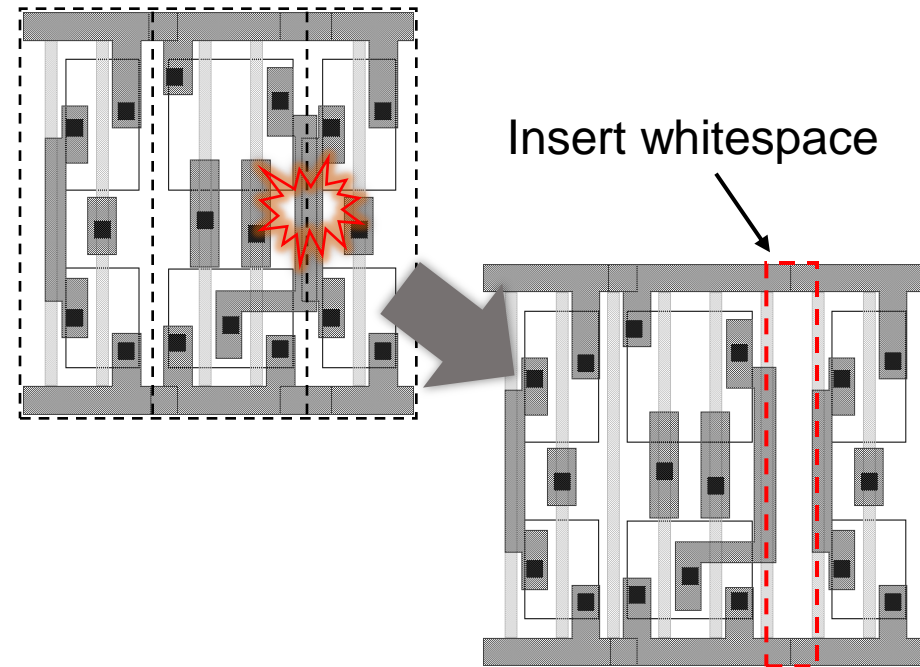
Implementation of Placement

Operations to generate a new placement



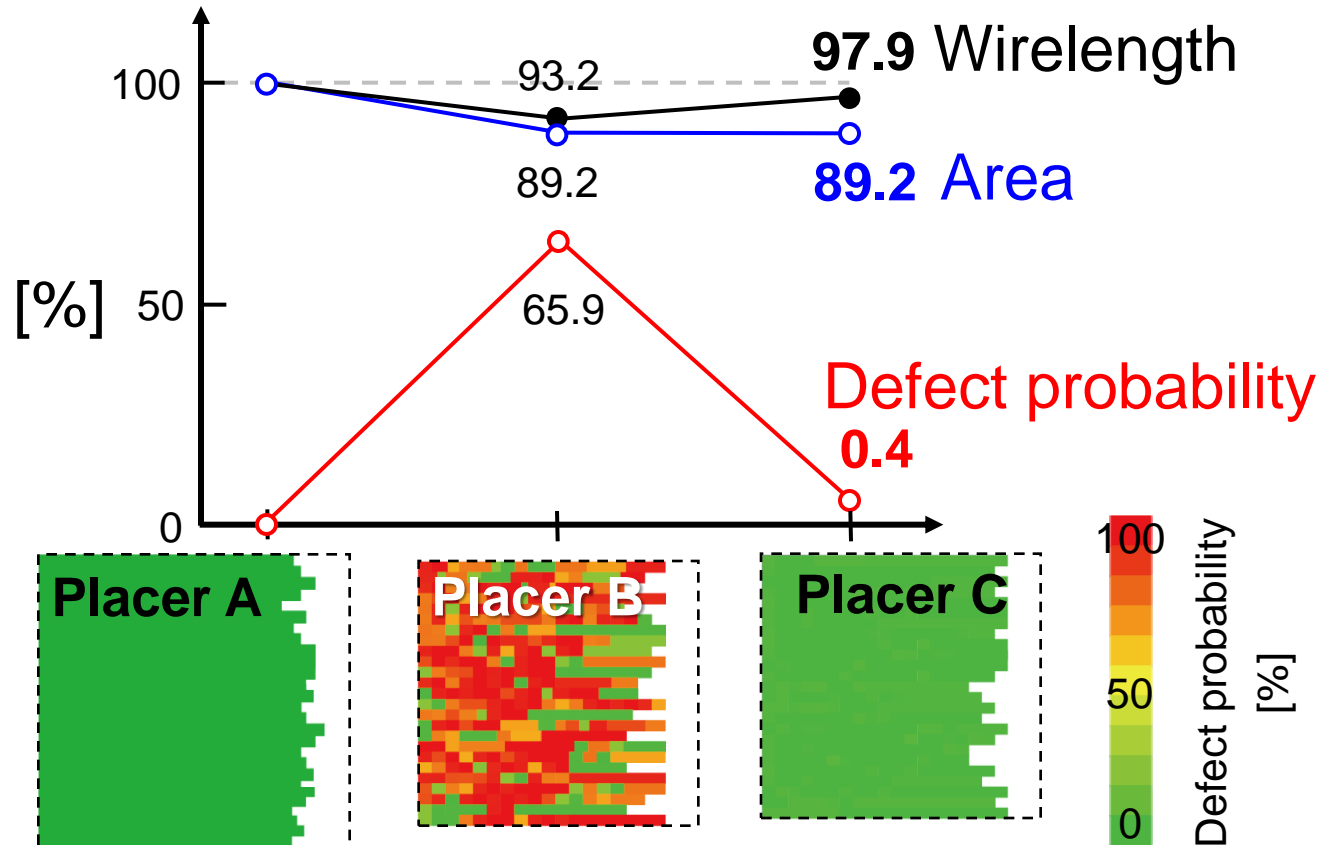
Whitespace injection

- After simulated annealing
- For defect prob. $>$ threshold



Experiment 1

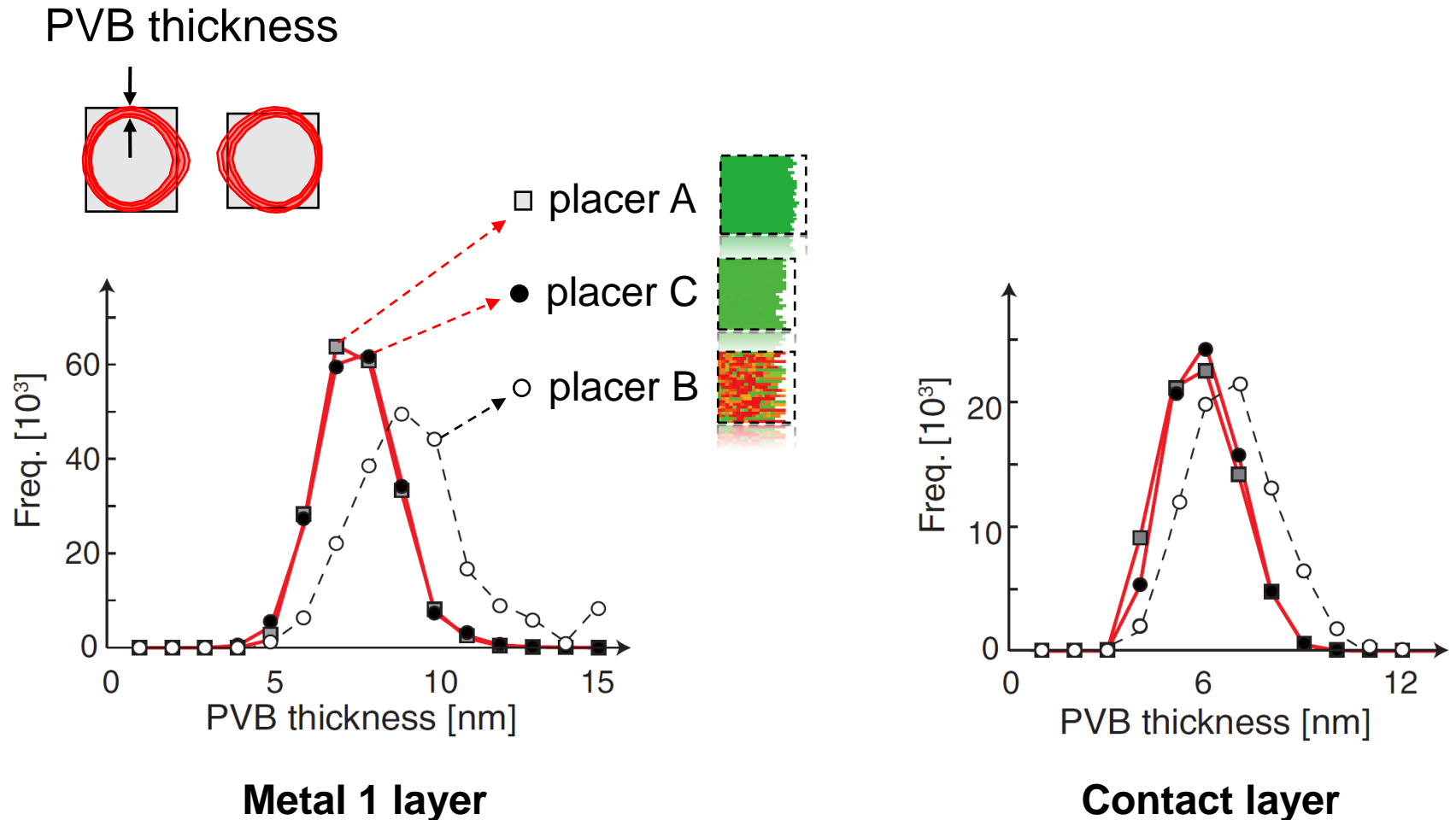
Assessment of placement



Placement	Standard	Standard	New
Cell type	Conventional	Compact	Compact

Experiment 2

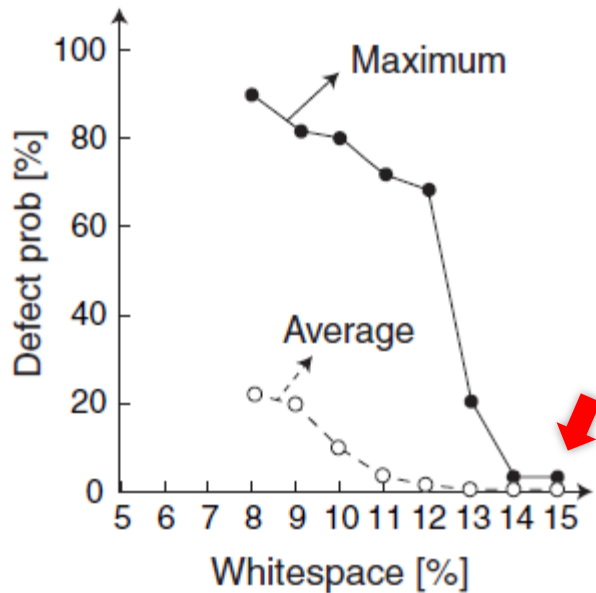
Assessment of PVB thickness



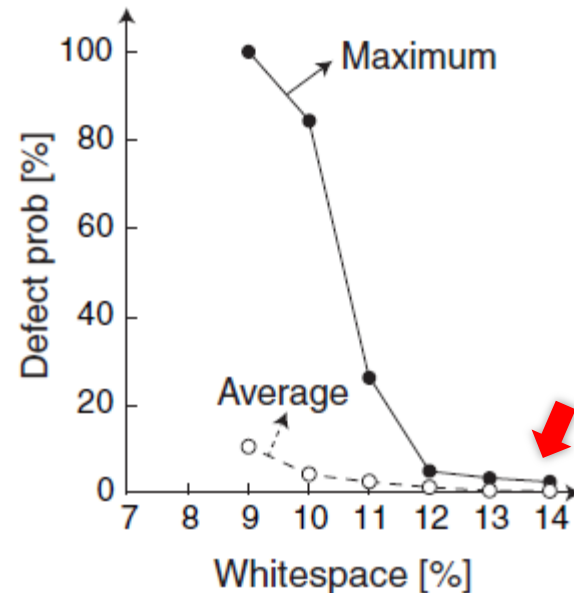
Experiment 3

Amount of whitespace vs defect probability

- More whitespace, easier placement (to decrease defect probability)
- Minimum requirement of whitespace: 15% (max. defect prob. < 5%)



spi

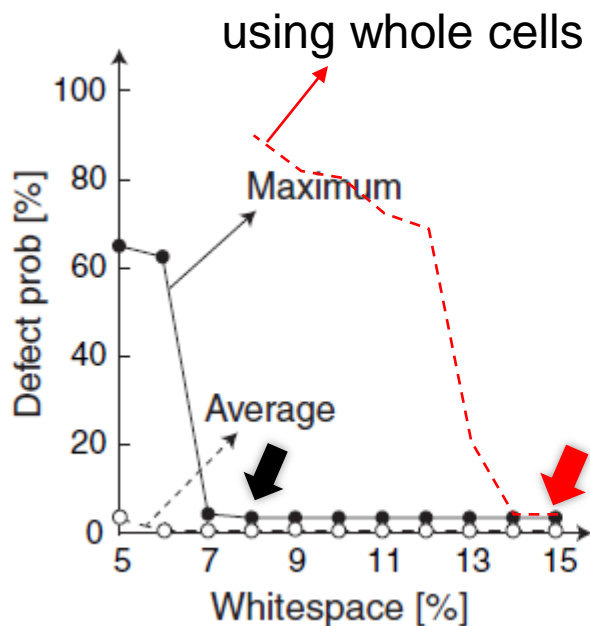
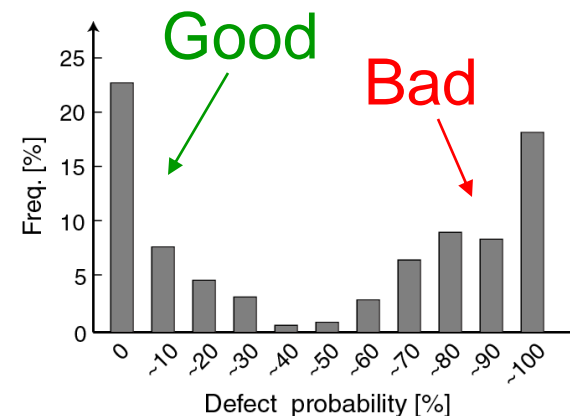


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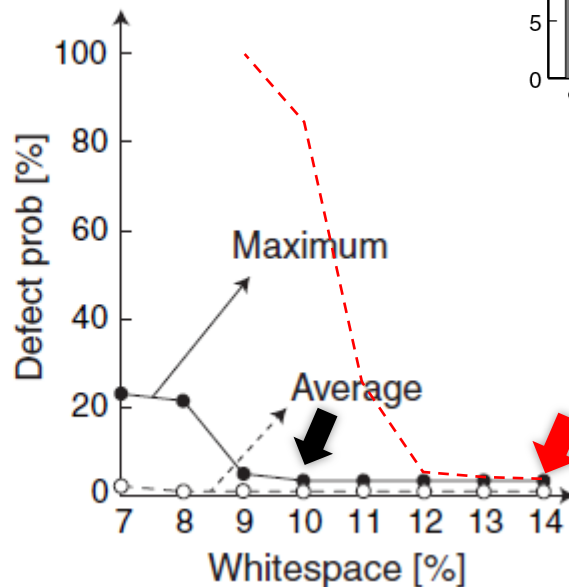
Experiment 4

Defect probability-aware logic synthesis

- Exclude **bad cells** in logic synthesis
- Bad cell: $\text{mean}[D(\text{bad cell}, *)] > 50\%$



spi



sasc

Summary

1. Inter-cell margin is not always necessary
 - Its need is determined by adjacent cell
 - If margin is completely removed, it may be probabilistically okay
2. Defect probability of all cell pairs can be computed very fast
3. Margin-less design has been tried
 - Area saving: 11%
 - Negative effect (lithographic defect) has been taken care of during placement