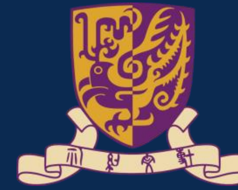
TECHNISCHE UNIVERSITÄT DRESDEN

TU Dresden, Institute of Electromechanical and Electronic Design



Chinese University of Hong Kong, CSE Dept.

Structural Planning of 3D-IC Interconnects by Block Alignment

Johann Knechtel (IFTE), Evangeline F. Y. Young (CUHK), and Jens Lienig (IFTE)

ASP-DAC 2014

Outline

I. Introduction and Motivation

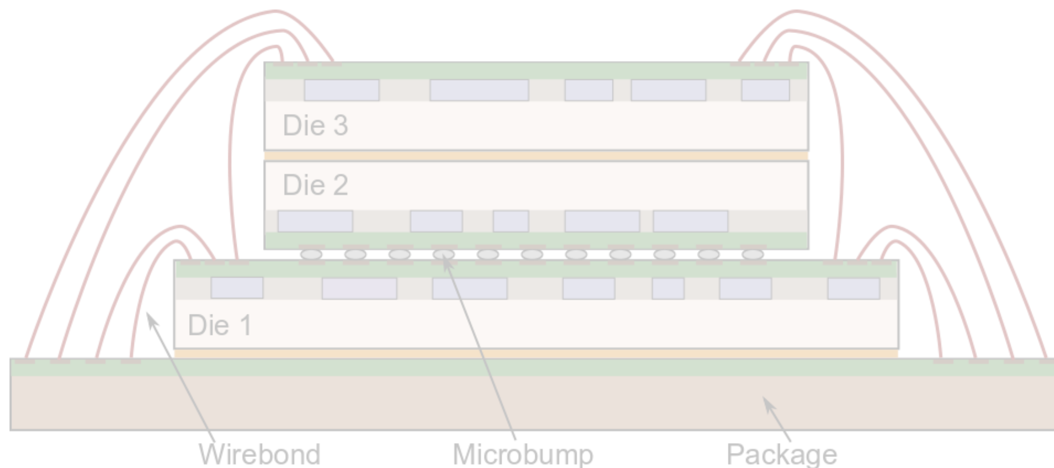
II. 3D-Floorplanning Methodology

III. Results and Summary

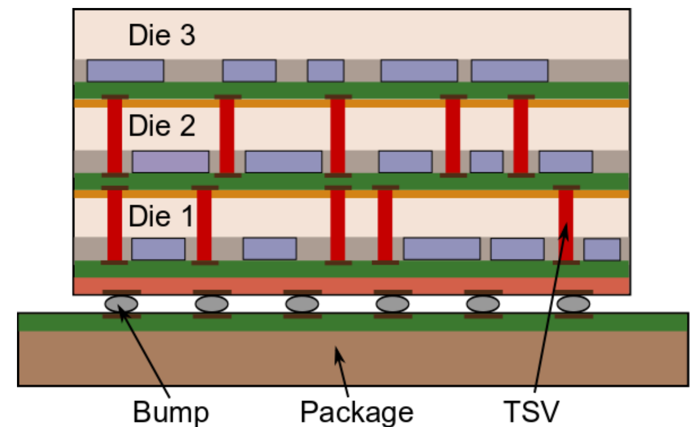
3D-Integrated Devices

- In general: multiple (≥ 2) active layers (dies, chips)
  - (+) Short interconnects: power consumption, delay, bandwidth
  - (+) Separate and smaller dies: heterogeneous integration and overall yield
  - (!) Complex design and manufacturing process

3D Packages



3D Integrated Circuits (3D ICs)



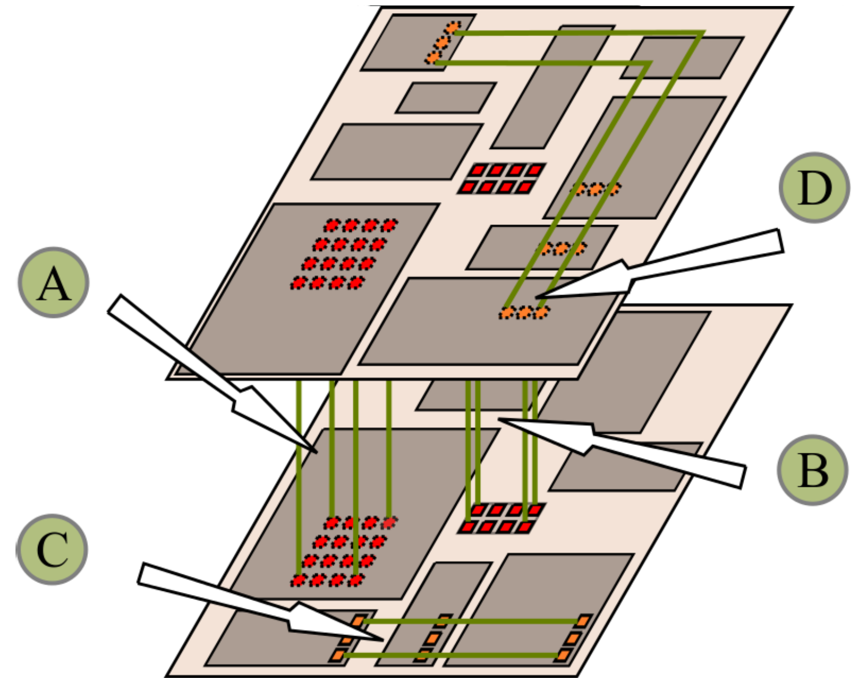
Motivation for Structural Planning of Interconnects

- Massively-parallel interconnects (large-scale 3D ICs)
  - Vertical buses (A), TSV stacks (B)
  - Classical buses, with fixed/flexible pins (C/D)

Massive detours for non-straight (i.e., bended) or long paths

- Depends on block placement and alignment

Targeted alignment of 2D blocks during 3D floorplanning to ensure short routing paths



Source:
Lim, S. K.
Personal Communication
2013

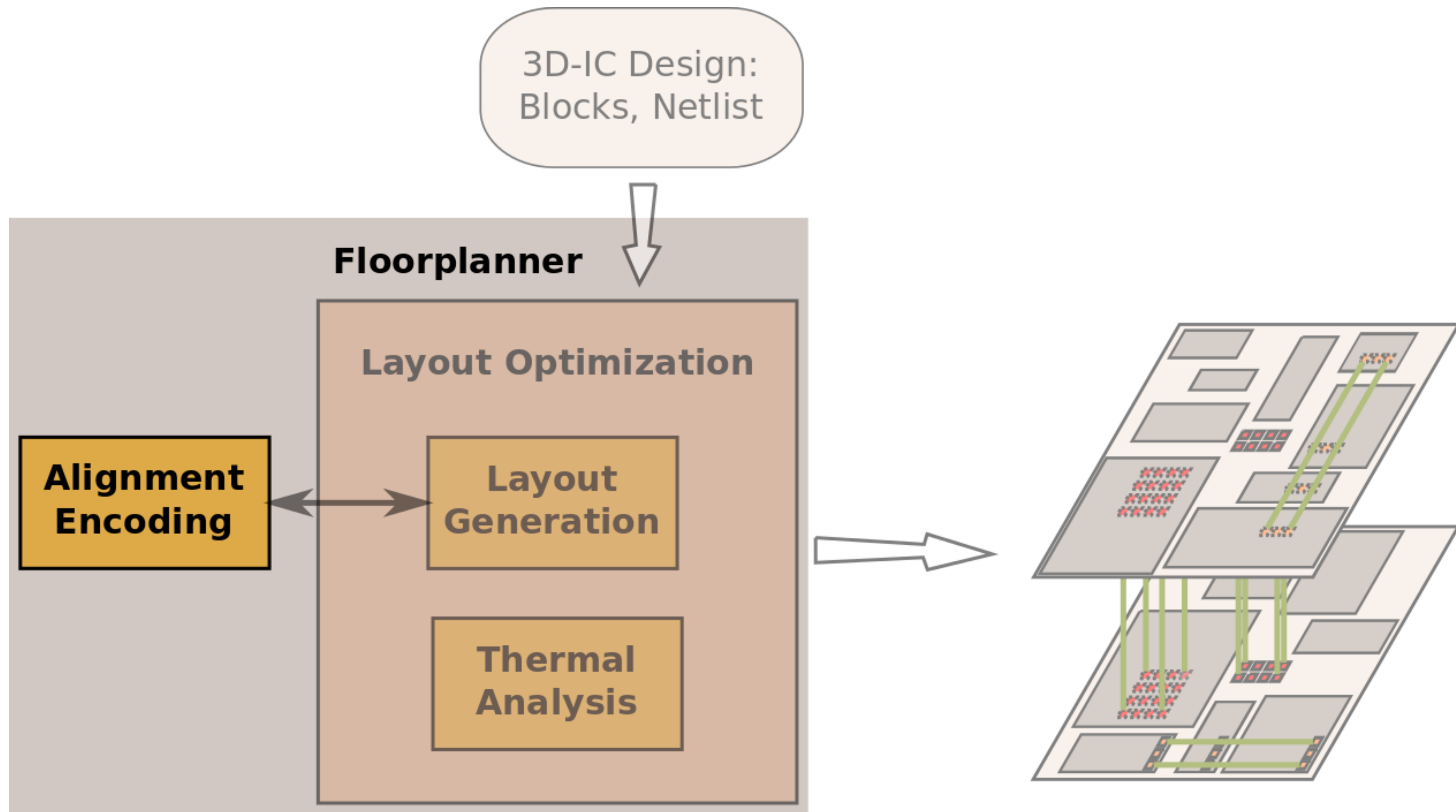
Outline

I. Introduction and Motivation

II. 3D-Floorplanning Methodology

III. Results and Summary

Components of Our 3D-Floorplanning Methodology



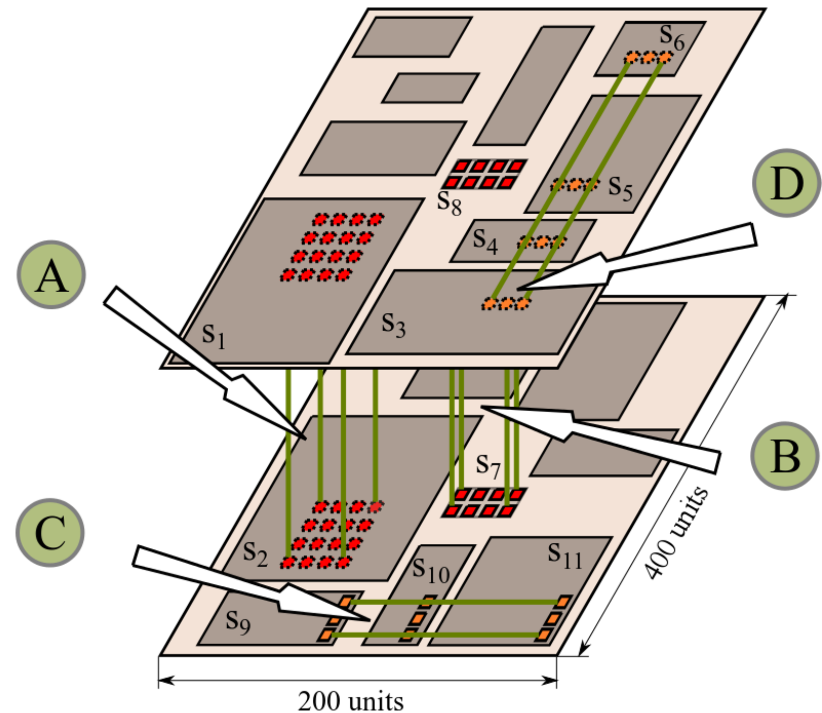
Alignment Encoding

- Minimal overlap "min" (A, C, D)
- Maximal distance "max" (C, D)
- Fixed offset "fix" (B, C)

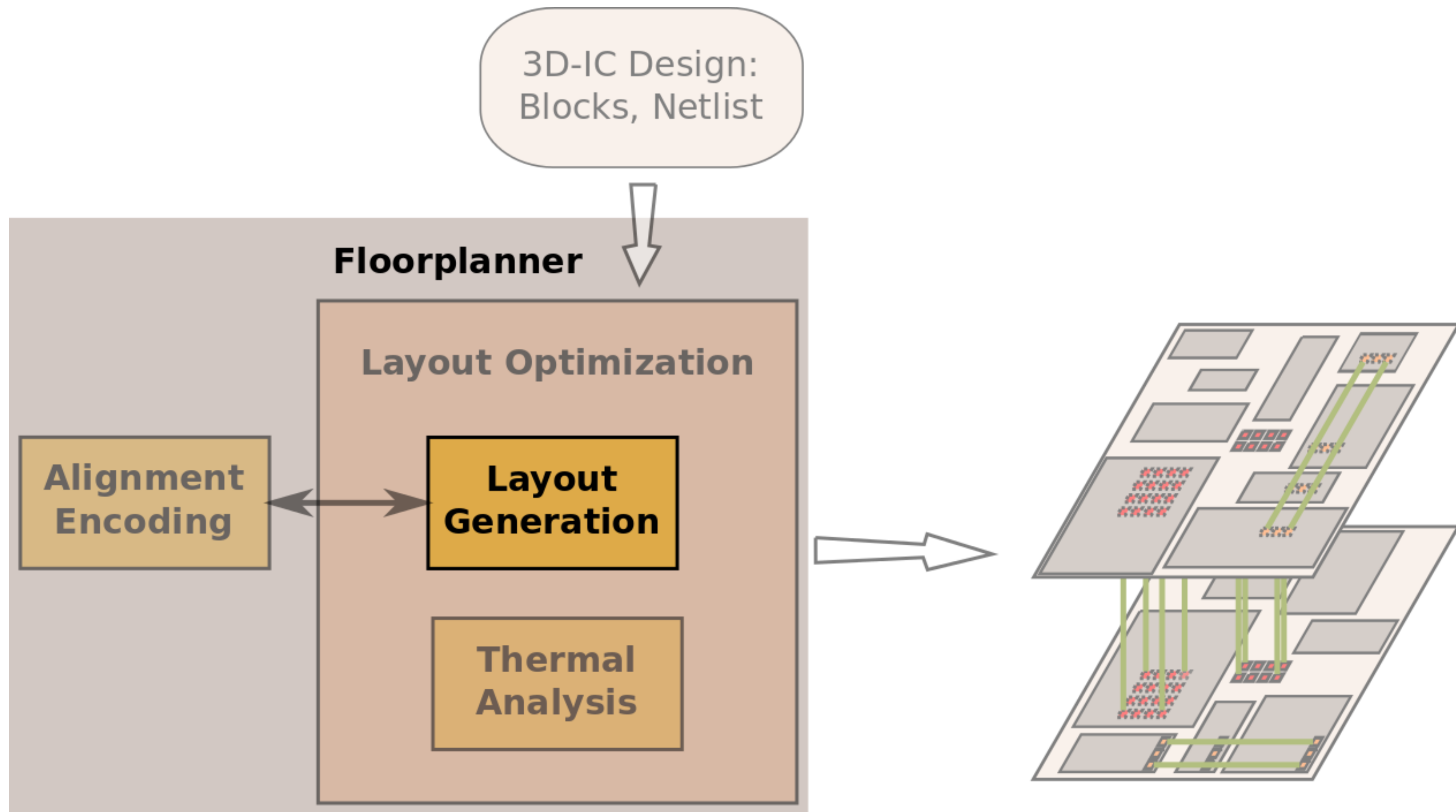
➔ Encoding with tuples (alignment of block pairs)

- E.g. (C):
  $a_1 = (s_9, s_{10}, (150, "max"), (0, "fix")),$
  $a_2 = (s_9, s_{11}, (200, "max"), (0, "fix"))$

➔ Unified approach, for alignment within and across dies

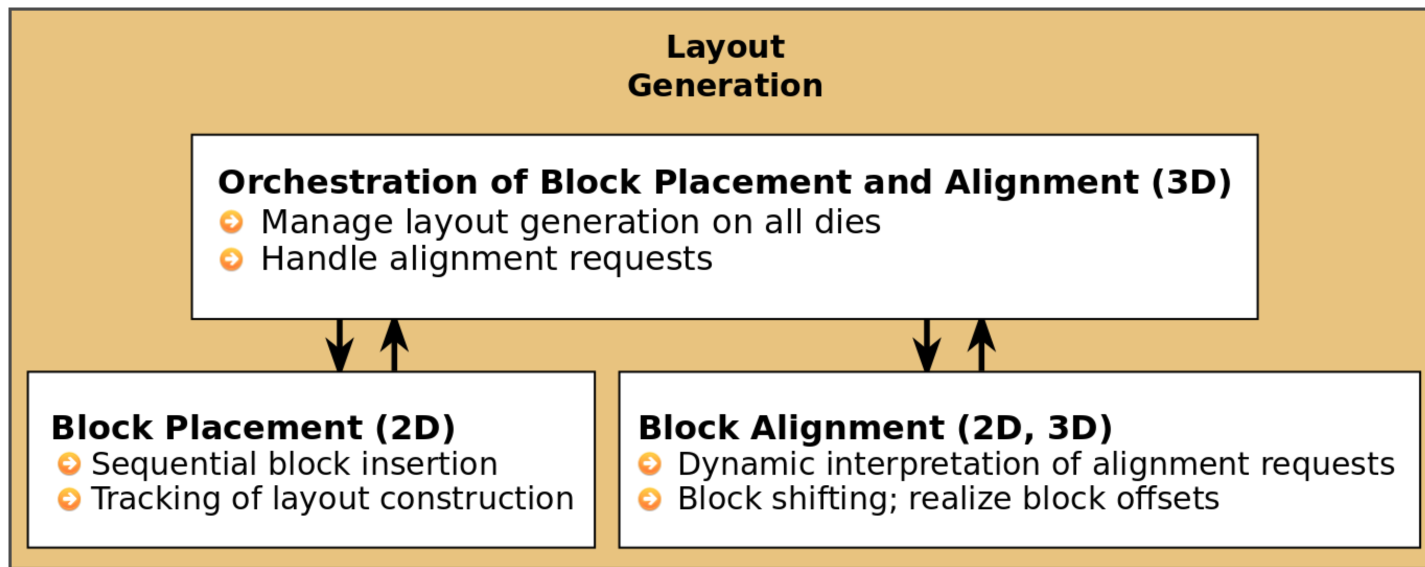


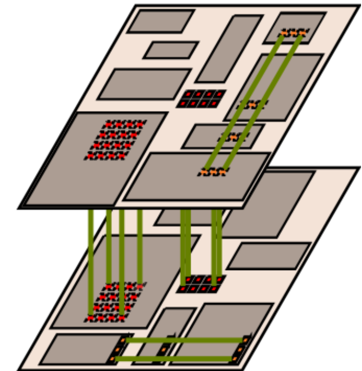
Components of Our 3D-Floorplanning Methodology



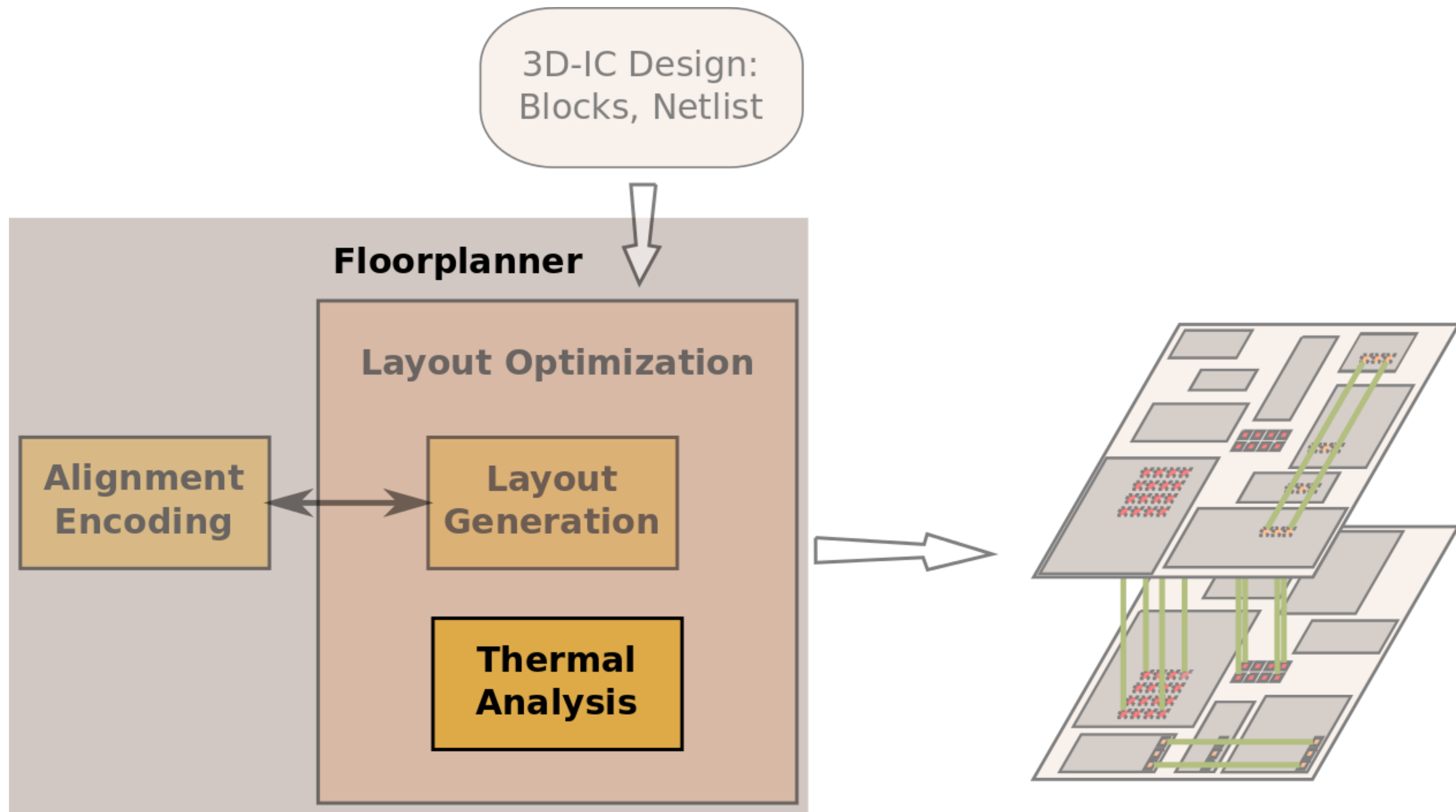
Layout Generation

- Extended Corner Block List
  - Application of alignment encoding
  - Extensions of CBL's placement technique, e.g., implicit packing
  - Orchestrated (i.e. synchronized) processes





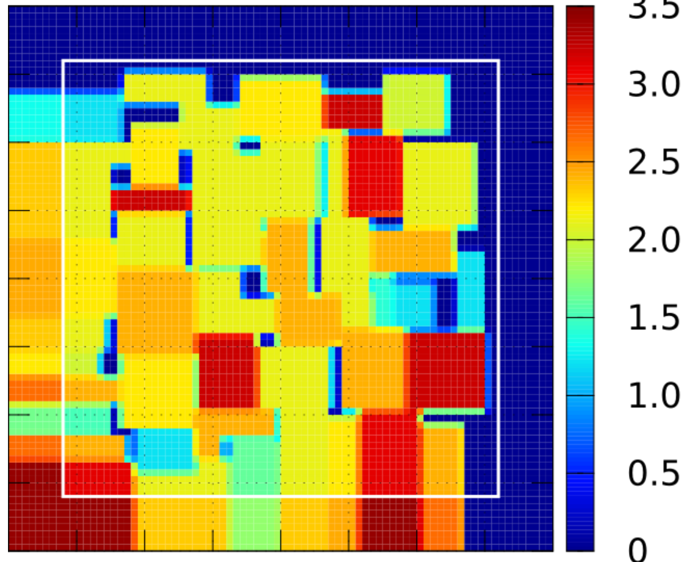
Components of Our 3D-Floorplanning Methodology

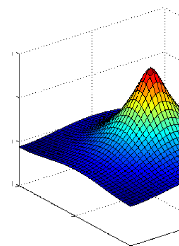


Thermal Analysis

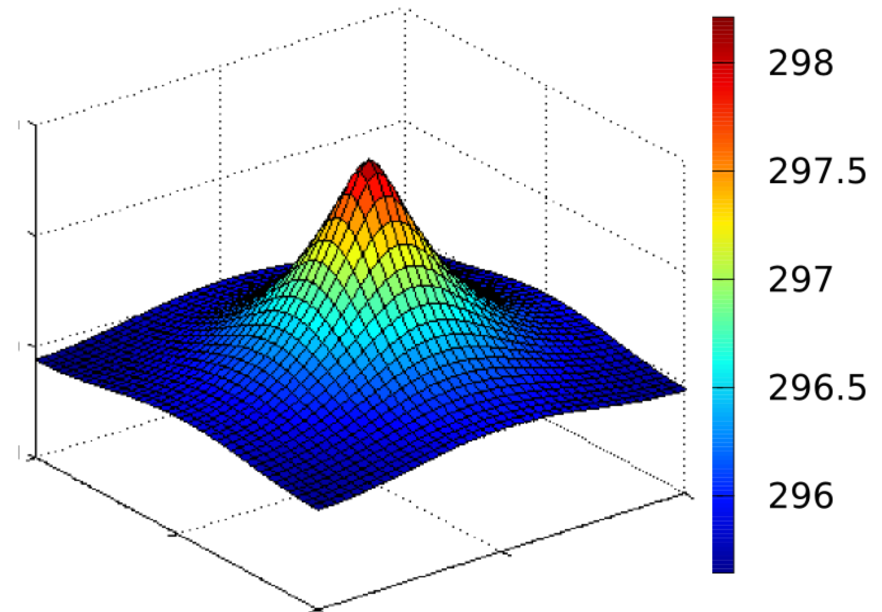
- Based on power blurring, a fast yet accurate approach [Park+09]
  - Matrix convolution; power densities * thermal-impulse responses
- Our extended power blurring: ≈3,000x faster than HotSpot
  - ➔ Symmetric, orthogonal Gauss functions; 2x 1D convolution → speedup ≈4x
  - ➔ Padded power maps; no data checks for convolution → speedup ≈4x

Power Density [10^{-3} μW/μm^2]

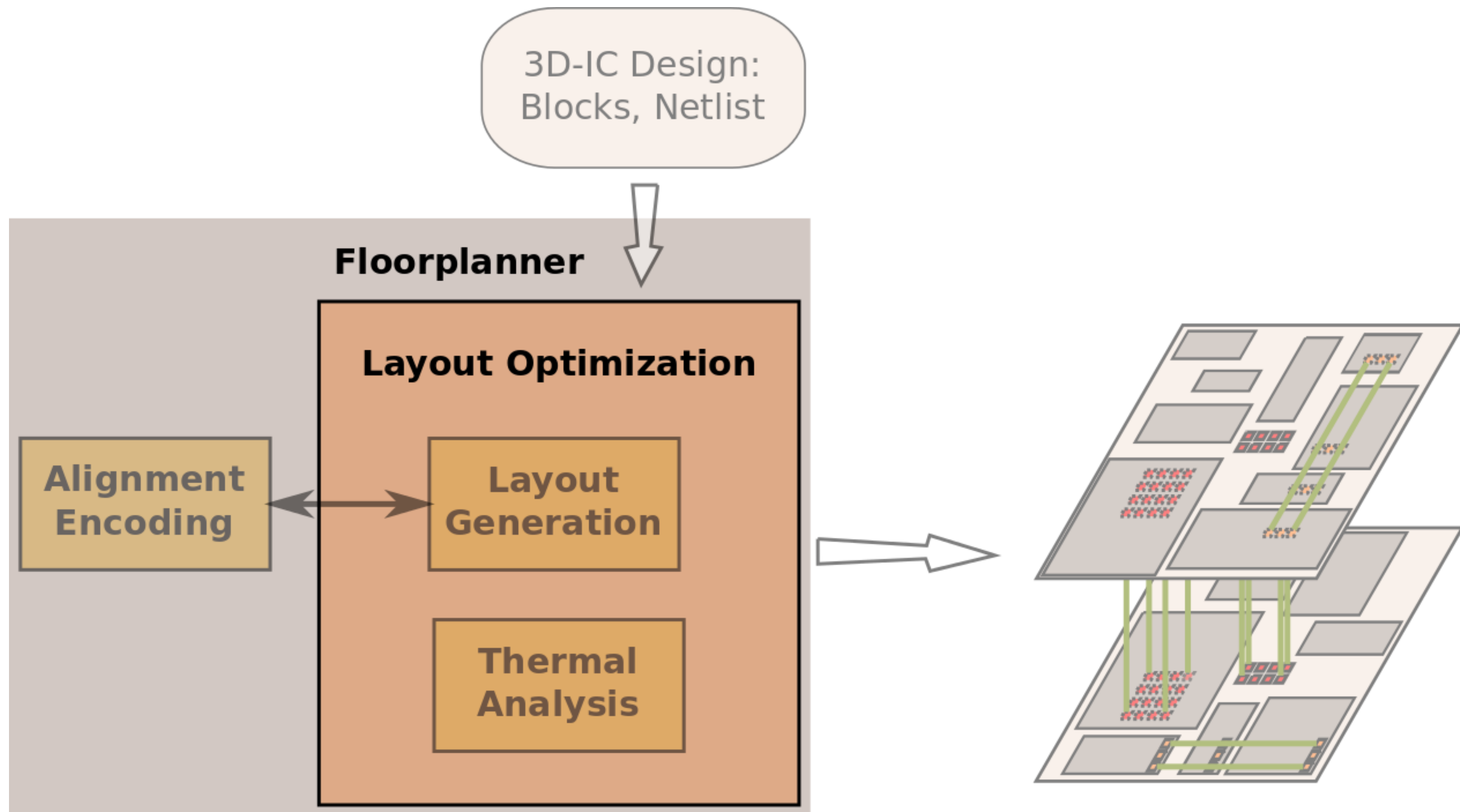




Estimated Temperature [K]



Components of Our 3D-Floorplanning Methodology



Layout Optimization

- Simulated annealing (SA)-based optimization
  - ⚠ 3D floorplanning with inter- and intra-die alignment is challenging
- ➔ Two phases: 1) fixed outline, 2) alignment and layout optimization
- ➔ Adaptive (i.e., robust) optimization schedule

Outline

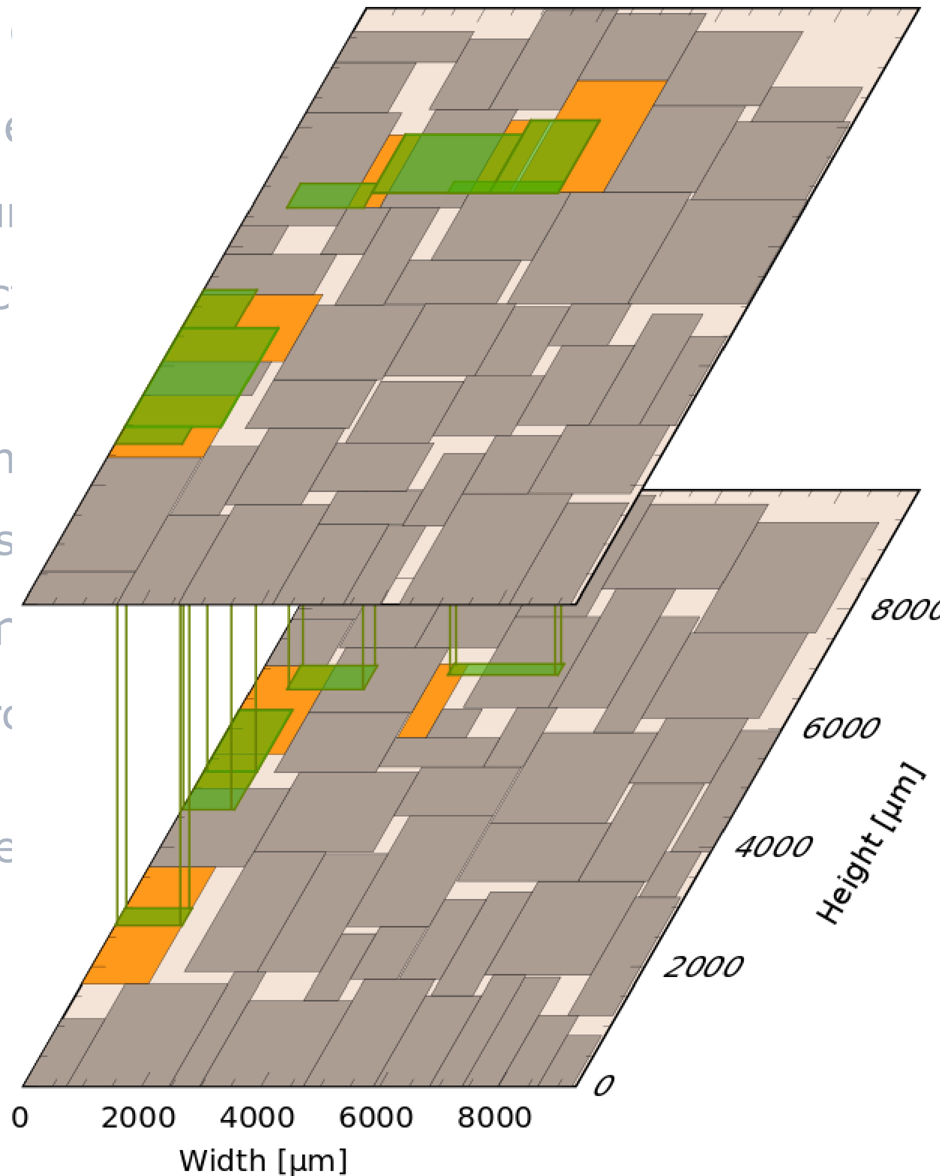
I. Introduction and Motivation

II. 3D-Floorplanning Methodology

III. Results and Summary

Results – Structural Planning of Interconnects

- Scaled-up
- Set of 10 l
  - Each bu
  - Intersec ultiple buses
  - Vertical nment)
  - Fixed an
  - Previous ed pins
- Effective m
  - All interc
  - On avg. to interconnects-unaware

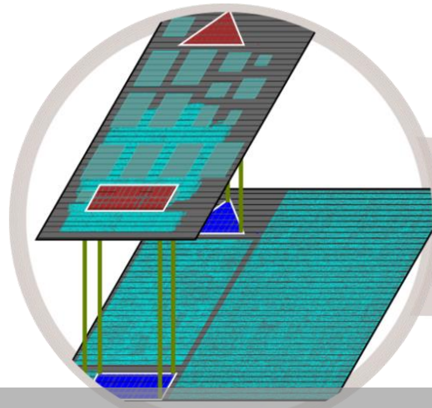


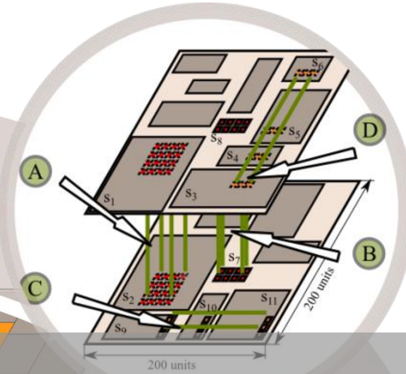
Results – Regular and Large-Scale 3D Floorplanning

- Competitive 3D floorplanner (GSRC benchmarks)
  - 3D-STAF [Zhou+07]:
    - Routing demand and max. temperatures comparable
    - On avg. 17.5% more compact layouts
  - 3DFP [Chen10]
    - Routing demand and max. temperatures reduced (avg. 20% and 40K, resp.)
    - Area slightly increased (avg. 10%)
- Large-scale IBM-HB+ benchmarks successfully applied, for 1st time

Summary

Goal: account for massively-parallel interconnects early on

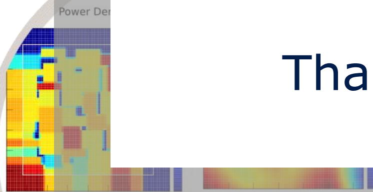


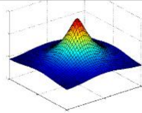


Flexible alignment encoding

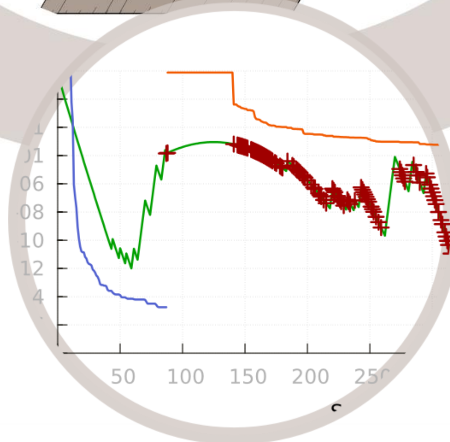
3D-Floorplanner „Corblivar“ Download:
www.ifte.de/english/research/3d-design

Thank you for your attention

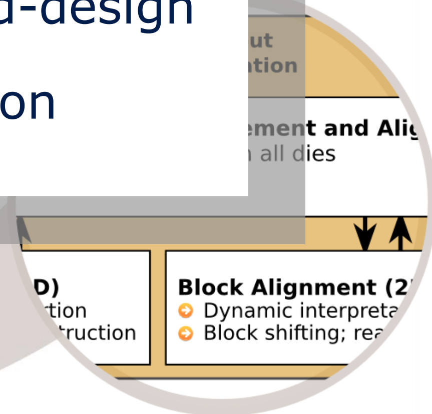




Fast yet accurate thermal analysis

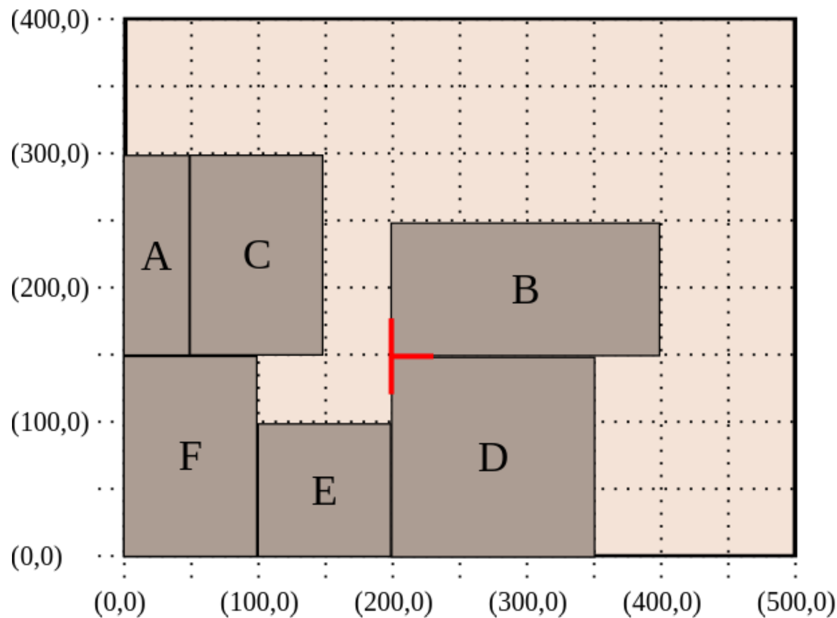


Effective layout optimization



Orchestrated block placement and alignment

Principles of Corner Block List



CBL:

S = (F, E, A, C, D, B) Insertion order

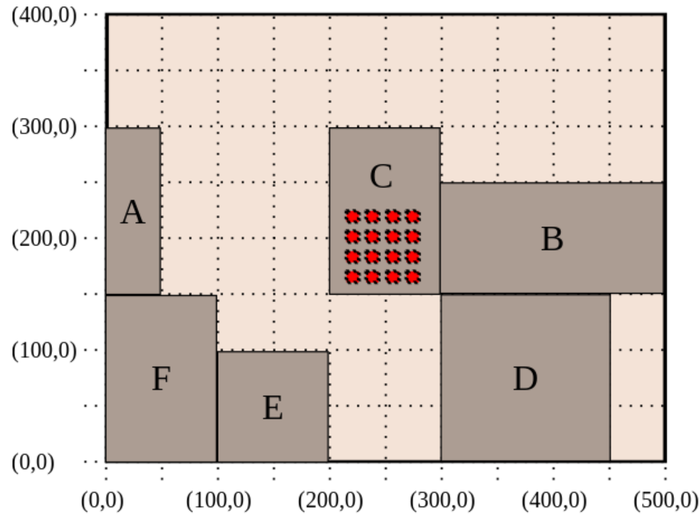
L = (h, v, h, h, v) Insertion direction

T = (0, 1, 0, 1, 0) T-junctions

Horizontal T-junctions

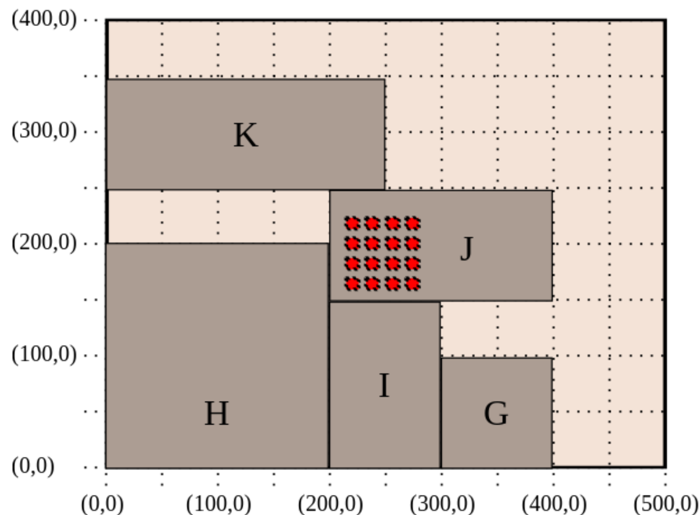
Vertical T-junctions

Extended Corner Block List



Die 1

CBL_1:
S_1 = (F, E, A, C, D, B)
L_1 = (h, v, h, h, v)
T_1 = (0, 1, 0, 1, 0)

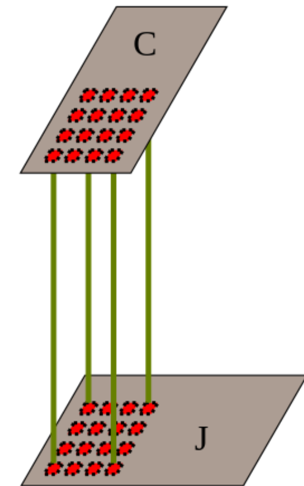


Die 2

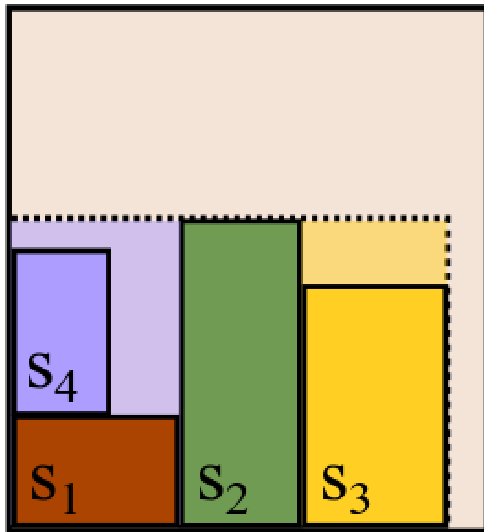
CBL_2:
S_2 = (H, I, G, J, K)
L_2 = (h, h, v, v)
T_2 = (0, 0, 1, 1)

Vertical bus, to be embedded in blocks C and J

a_1 = (C, J, (0,"fix"), (0,"fix"))



Implicit Packing – Virtual CBL Adaption



CBL Encoding:

$S = (s_1, s_2, s_3, s_4)$

$L = (h, h, v)$

$T = (0, 0, 2)$

Equivalent Encoding Example:

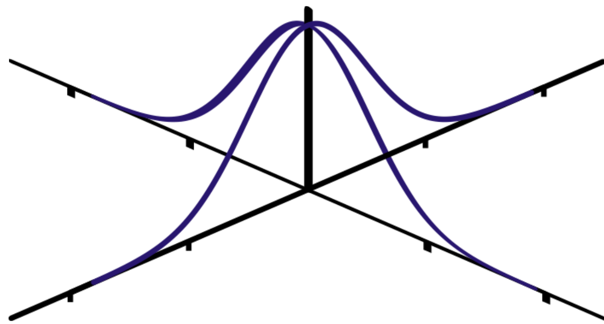
$S = (s_1, s_4, s_2, s_3)$

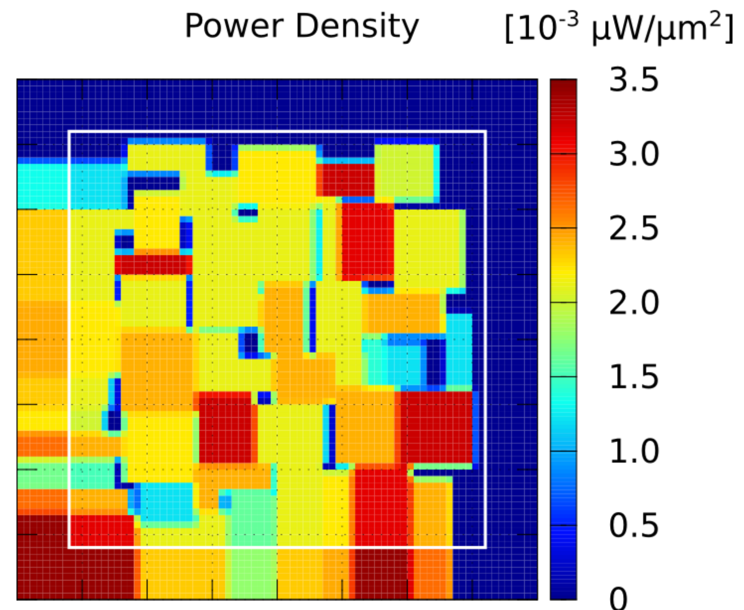
$L = (v, h, h)$

$T = (0, 1, 0)$

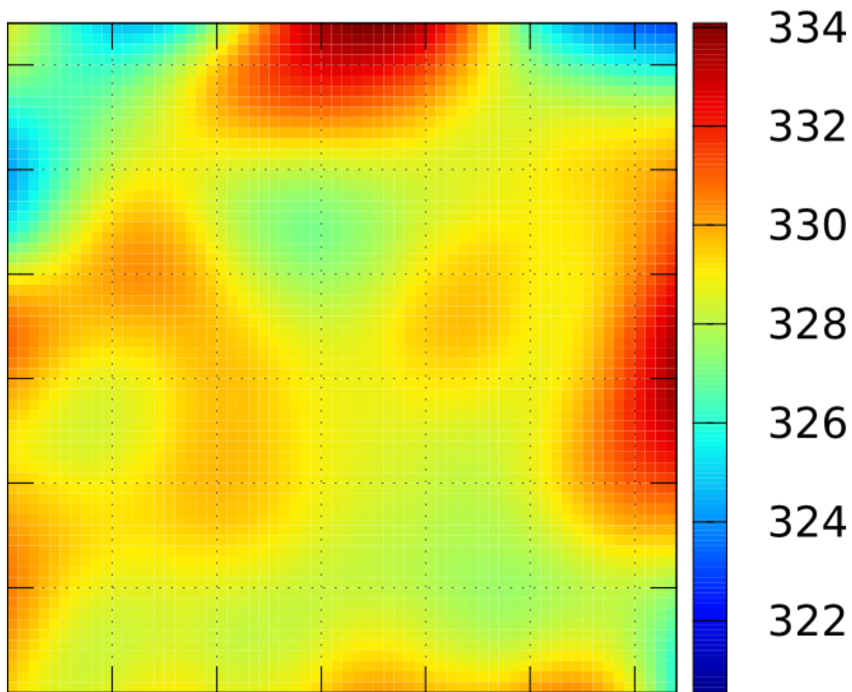
Extended Power Blurring

- Thermal-impulse responses modeled as orthogonal Gauss functions
  - No FEA runs required; parameterization based on HotSpot references
  - Symmetric functions; 2D convolution as 2x 1D convolution → speedup ≈4x
- Padding of power-density maps
  - Flexible error compensation for (adiabatic) die boundaries
  - No data checks for convolution loops → speedup ≈4x

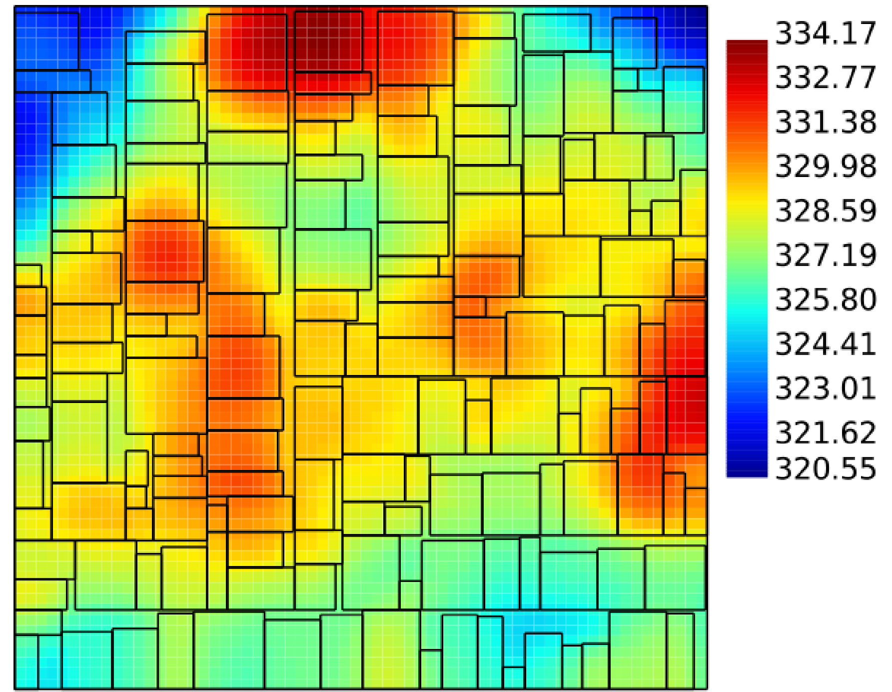




Accuracy of Power Blurring



Analysis w/ power blurring



Analysis w/ HotSpot (thermal RC network)