FROM RESEARCH TO INDUSTRY

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3DCoB: A new design approach for Monolithic 3D Integrated Circuits

CEA-Leti, Grenoble, FRANCE

Hossam SARHAN, Sébastien THURIES, Olivier BILLOINT & Fabien CLERMIDY

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leti & list

Outline:

- Introduction to 3D Integrated Circuits
- 3D Monolithic Integration (3DMI) Technology
- Previous 3DMI Approaches
- 3D Cell-on-Buffer (3DCoB) Approach
- 3DCoB Design Flow
- Results and Conclusion

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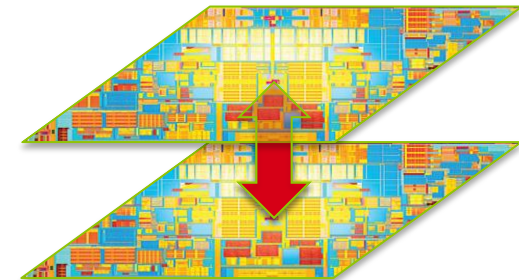
Introduction to 3D Integrated Circuits

Why logic-on-logic 3D stacking ?

- Better performances (shorten wires → less delay)
- Less power (shorten wires → less parasitics)
- Smaller footprint.

> **Overcomes technology scaling limitation !**

2D IC



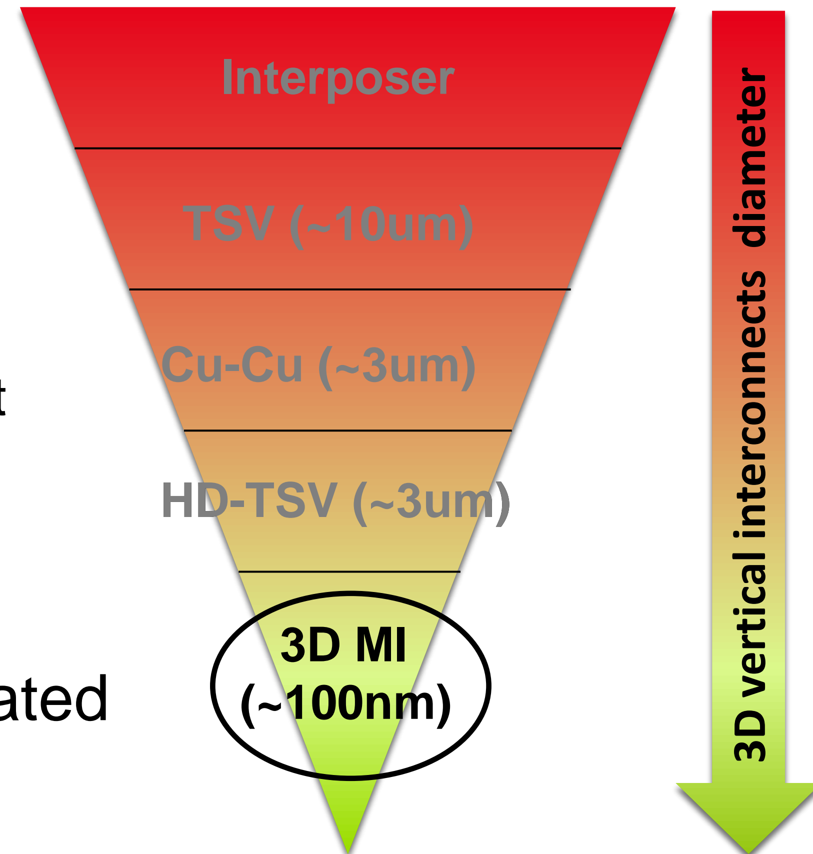
3D IC

3D Technology Limitations:

- Large size of the 3D interconnects (area overhead).
- Limited number of vertical interconnects (3D-Vias).
- 3D interconnects parasitics (resistance/capacitance).

3D Integration Technologies

- **Parallel Integration**
  Dies fabricated separately then vertically stacked, such as:
  - ➔ Passive/Active Interposer
  - ➔ Through-Silicon-Via (TSV)
  - ➔ Copper-to-Copper (Cu-Cu) contact
  - ➔ High-Density TSVs
- **Sequential Integration**
  Second transistor layer is fabricated directly on the top of first one. (Cold process)
  - ➔ **3D Monolithic Integration (3DMI)**



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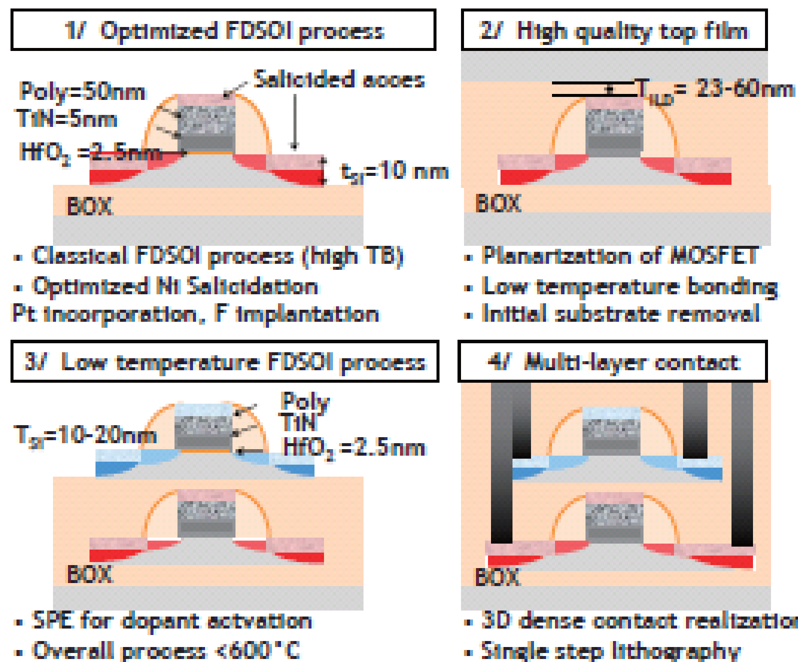
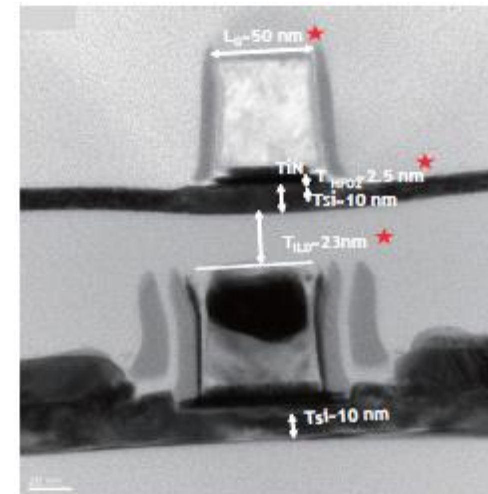
Monolithic 3D Integration Technology

+ Second transistor layer is fabricated sequentially on top of the first one.
+ High alignment precision, and very small 3D vias

→ 30 times smaller compared to state-of-the-art "HD-TSV & Cu-Cu"





[*] P. Batude et al.,"Demonstration of low-temperature 3D sequential FDSOI integration down to 50 nm gate length" VLSI Technology (VLSIT), symposium on, IEEE, 2011.

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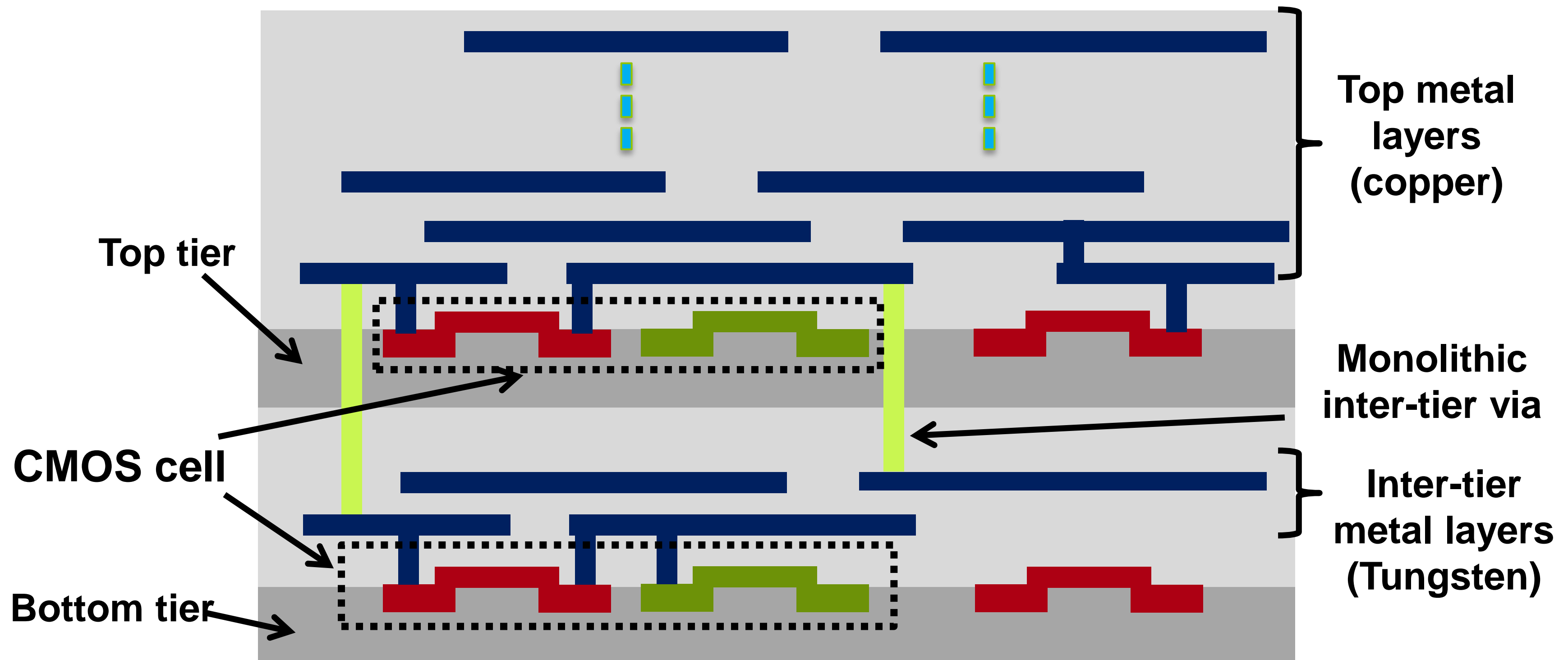
Previous 3DMI Approaches (1/2)

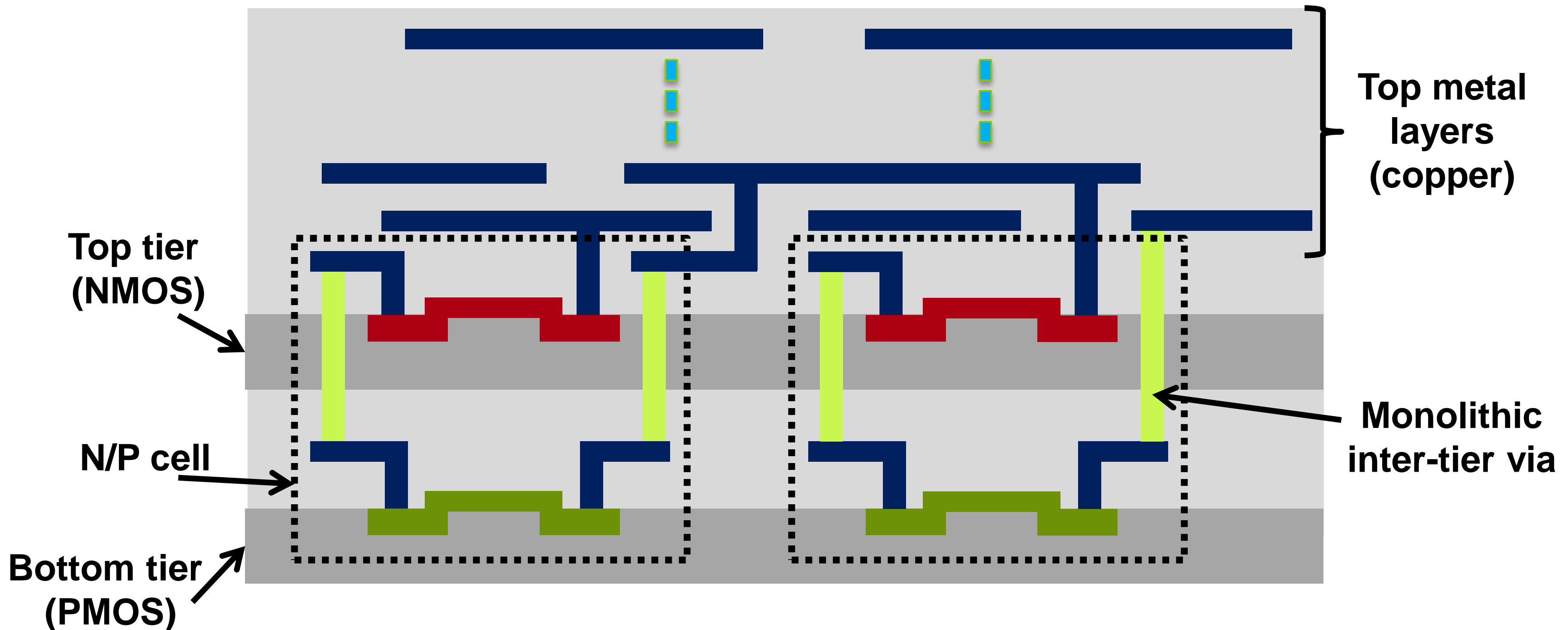
1. Gate-level approach (Cell-on-Cell)



+ Using 2D CMOS standard cells.
- Incompatible with the conventional 2D design flow.

Previous 3DMI Approaches (2/2)

2. Transistor-level Integration (NMOS/PMOS)



\+ Compatible with the conventional 2D design flow.

\- 3D NMOS-over-PMOS (N/P) cells are needed.

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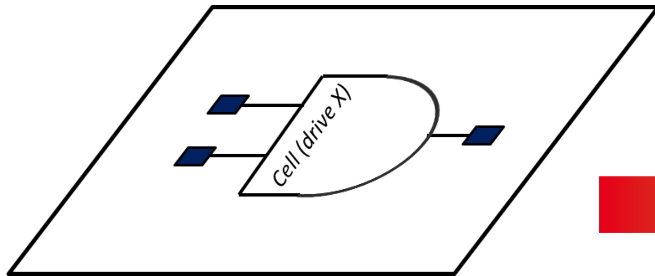
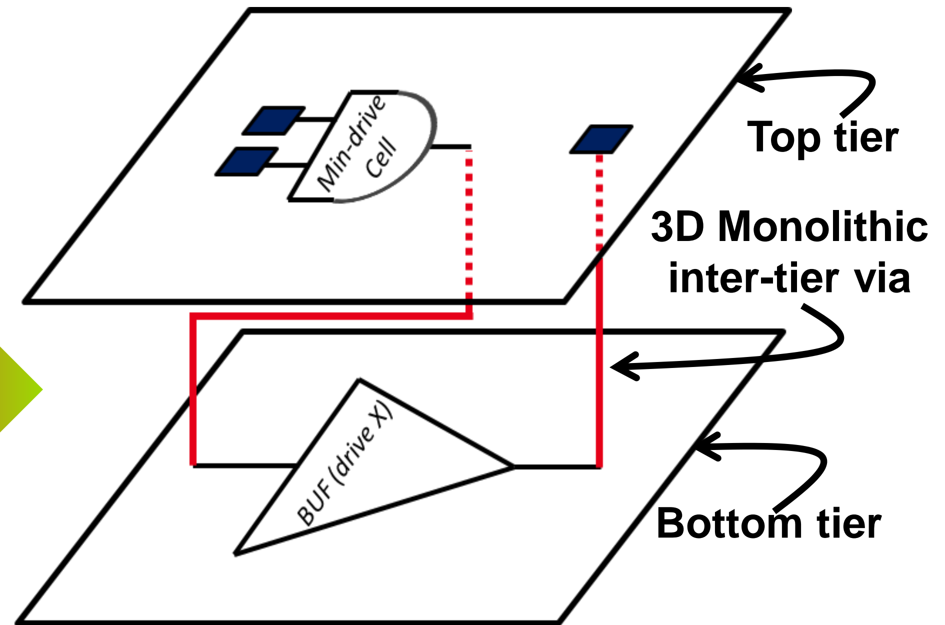
Proposed Approach: "3D Cell-on-Buffer"

- Split non-minimum drive cells into 2 tiers:
  - Min drive logic cell in top tier.
  - Driving buffer into bottom tier.

2D Non-MIN Drive Cell



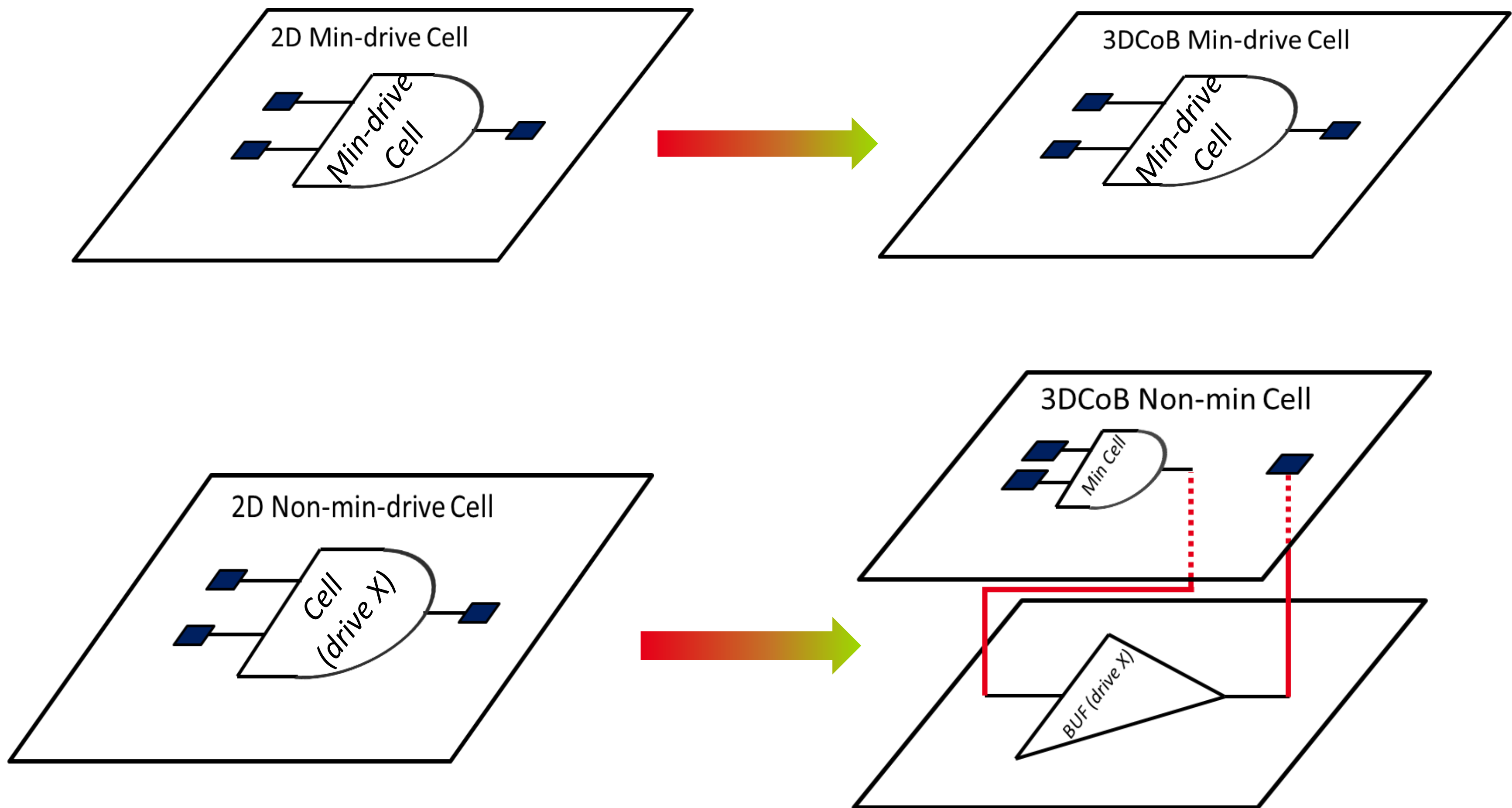
3DCoB Non-MIN Drive Cell



- Min drive cells are still in 2D (planar).

Proposed Approach: “3D Cell-on-Buffer”

- Consequently the 3DCoB set of cells will be:



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Comparison with other approaches

"3D Cell-on-Buffer (3DCoB)" vs. "Cell-on-Cell" vs. "N/P"

	N/P	Cell-on-Cell	**3DCoB (our work)**
2D Design flow compatibility	Yes	No	**Yes**
Using 2D standard cells	No	Yes	**Yes**
Using inter-tier routing metal layers	No	Yes	**No**
Usage of inter-tier vias	In every cell	Between cells (if req.)	**Only in the 3D cells**

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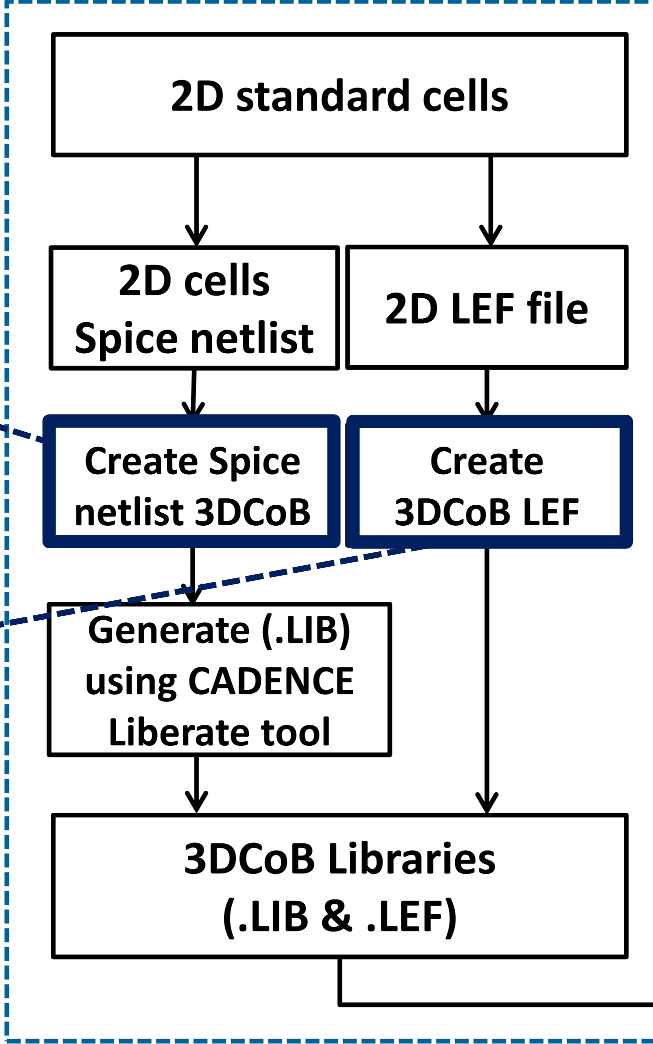
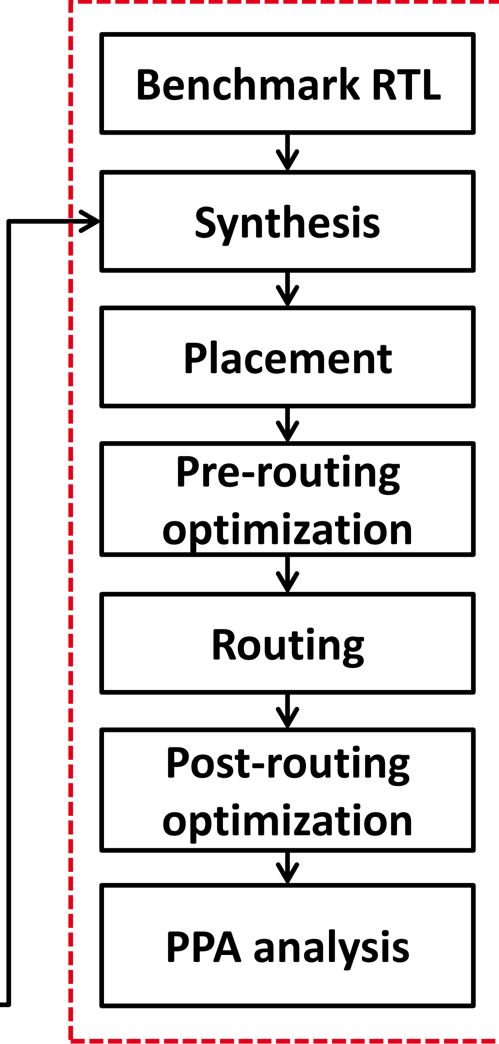
3DCoB Design Flow

By connecting in series “the min-drive cell of the same type” with “the equivalent-drive buffer”

By determining the area of the 3DCoB cells



3DCOB Libraries generation



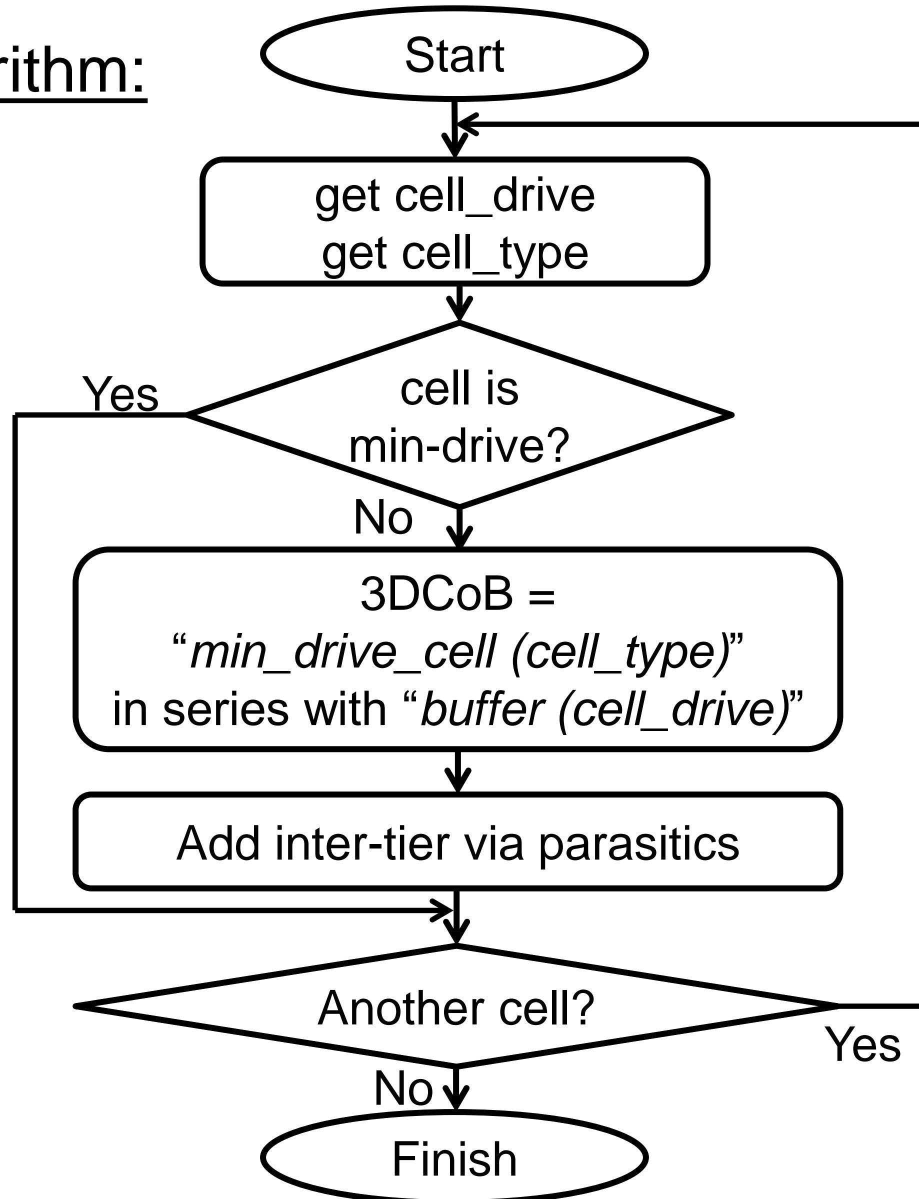
Conventional 2D implementation flow (CADENCE tool)

3DCoB Design Flow : LIB generation

- 3DCoB Cells generation algorithm:

Example: "**AND2x33**" ➔
- The type is 2-input AND gate "**AND2x**"
- Cell drive = "**33**"
- The min-drive cell of the 2-input AND is "***AND2x8***"
- The equivalent-drive buffer is "***BUFx33***"

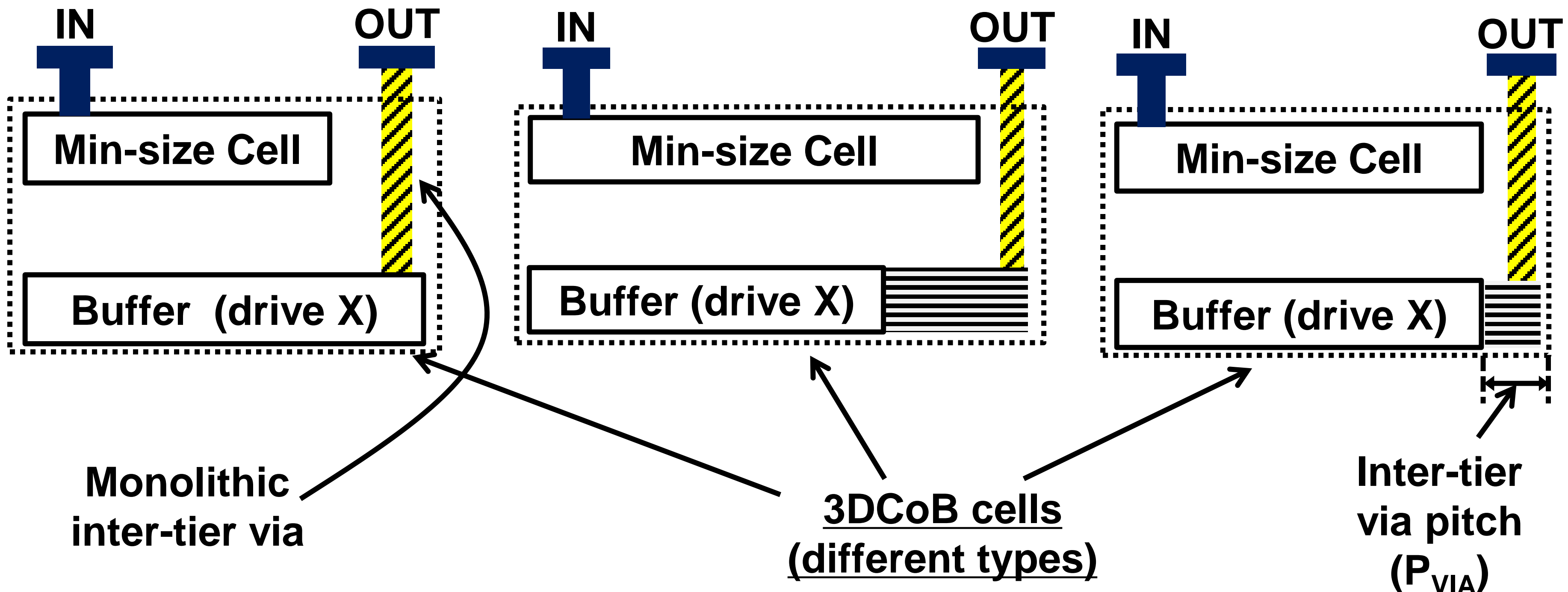
3DCoB cell for AND2x33 is:
"***AND2x8***" in series "***BUFx33***"



3DCoB Design Flow: LEF generation

- Area of 3D Cell-on-Buffer Cells depends on:
  1. Area of the buffer (A_{BUF}) compared to the min-drive cell ($A_{MIN\text{-}CELL}$).
  2. Inter-tier Via pitch (P_{VIA})

$$Area_{3DCoB} = \begin{cases} A_{BUF}, & (A_{MIN-CELL} + P_{VIA}) < A_{BUF} \\ \max(A_{MIN-CELL}, A_{BUF}) + P_{VIA}, & (A_{MIN-CELL} + P_{VIA}) \geq A_{BUF} \end{cases}$$



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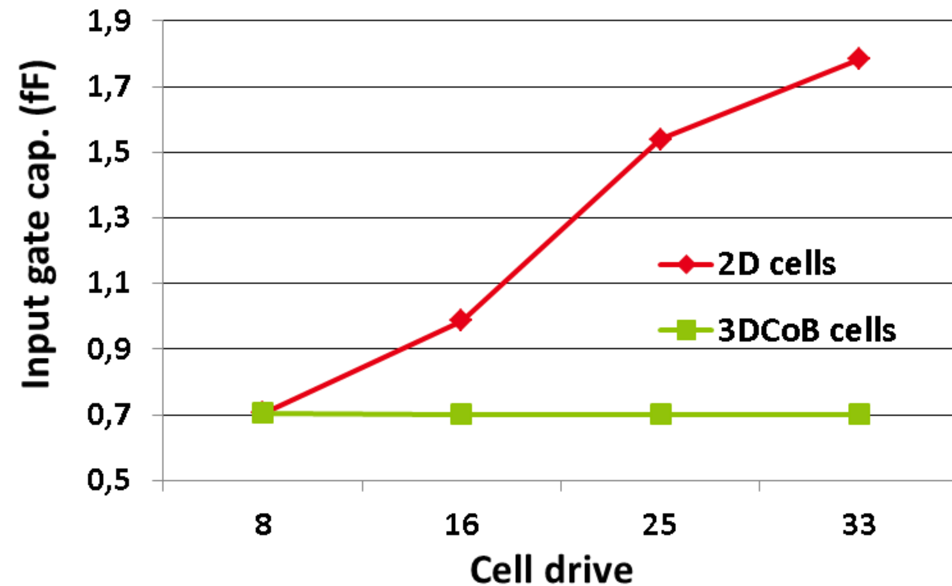
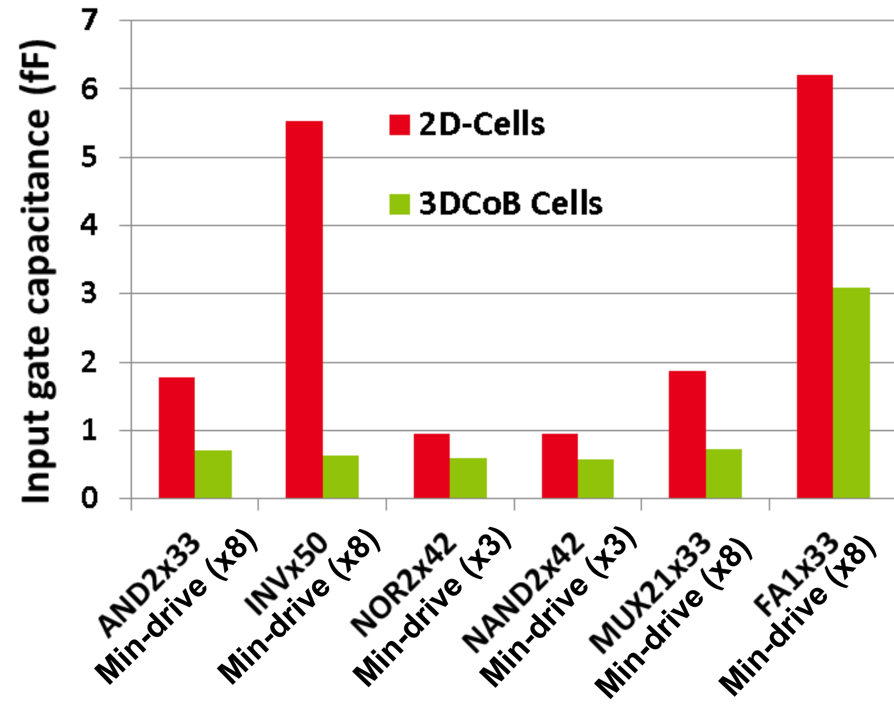
Results: 3DCoB Input Capacitance



2-input AND gate at different drives



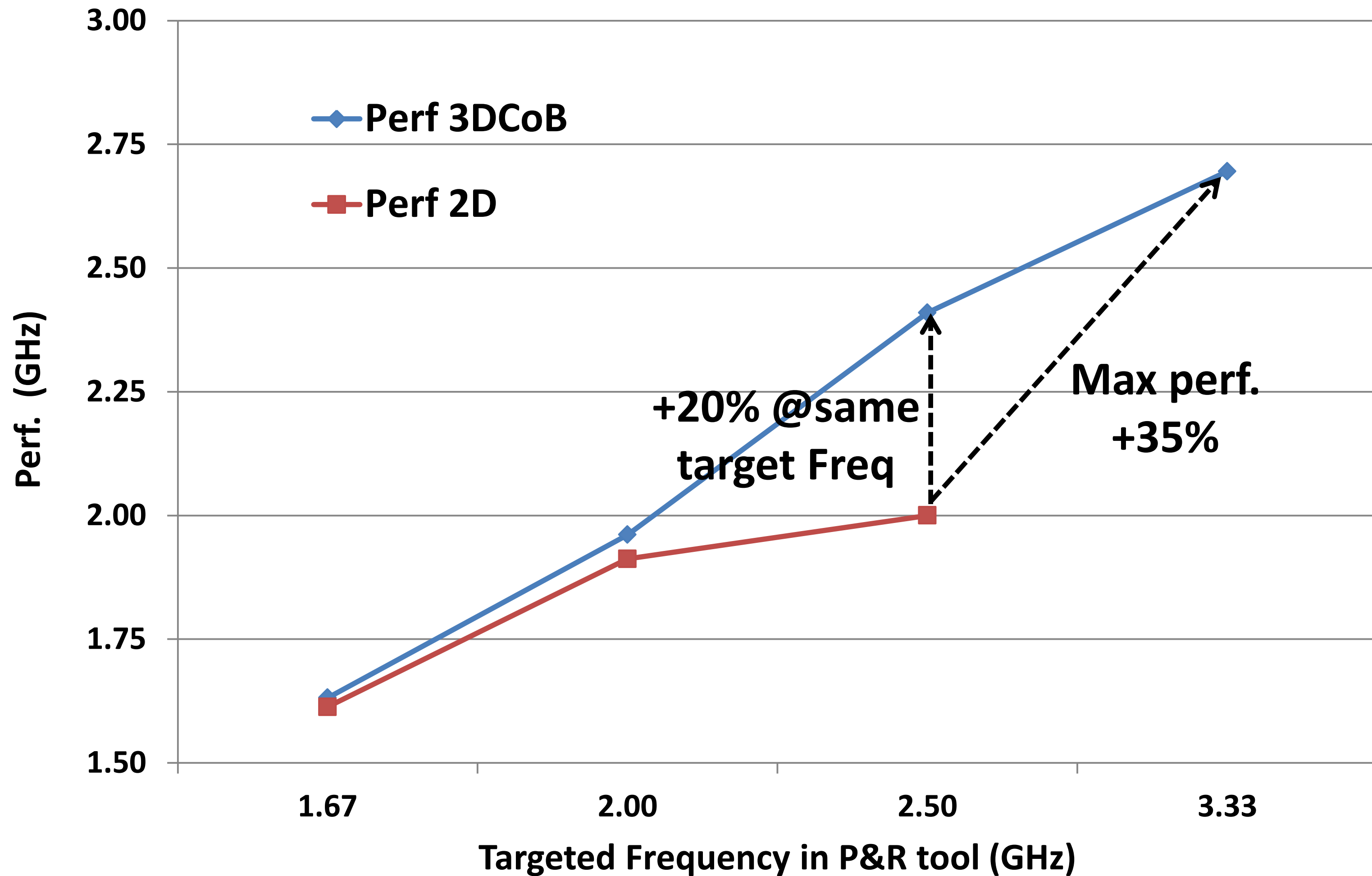
Results: FFT & AES blocks in 28nm FDSOI

		# Std Cells	Cell Density	Perf[1] (GHz)	Perf[1] Gain (%)	Power[2] (mW)	Power[2] Loss (%)
FFT Target freq=1.67GHz Area=0.027mm^2	2D	24771	95%	1.33	--	36.001	--
	3DCoB	26210	93%	1.51	13.53%	37.452	-4.03%
AES Target freq=2.55GHz Area= 0.119mm^2	2D	164174	89%	2.00	--	249.774	--
	3DCoB	166749	90%	2.41	20.5%	263.165	-5.36%

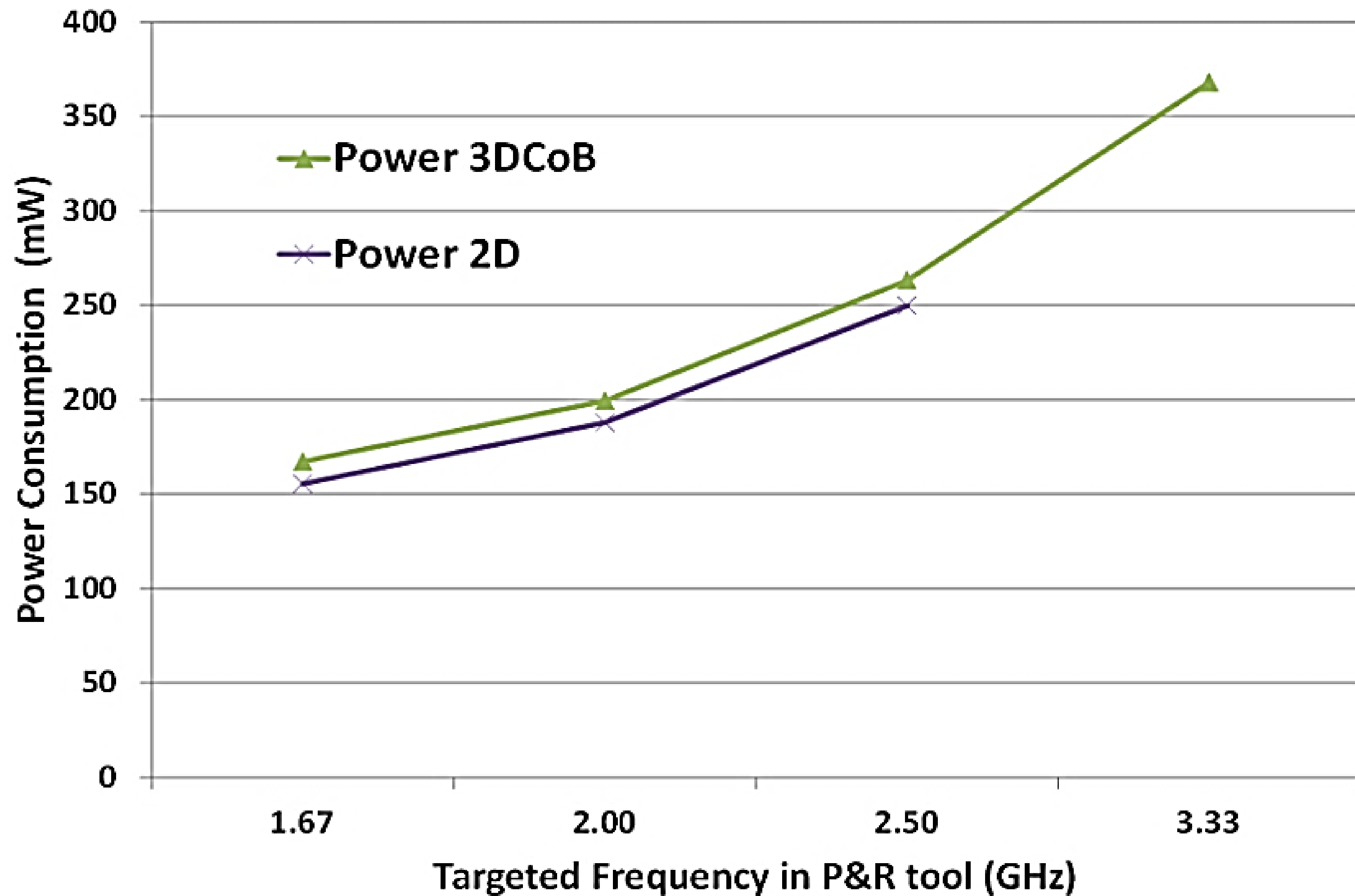
[1] Performance is measured as the effective clock frequency (target clock period without slack time)

[2] Power is calculated with activity factor (0.15) using SoC Encounter power reports

Results: Performance of AES-128 block



Results: Power of AES-128 block



Conclusions

- 3D Cell-on-Buffer (3DCoB) architecture shows:
  - **Improvement in performances (~ 20 to 35%)**
  - **Compatible design flow with 2D EDA tools.**
  - Limited impact on power consumption.
  - No need for inter-tier routing metal layer in the bottom tier.
  - No clock synchronization issue between the two tiers.
- Thermal impact needs to be studied as well !
  - Targeted low-power applications will limit this issue

Thank You
Questions ?

leti
Centre de Grenoble
17 rue des Martyrs
38054 Grenoble Cedex

list
Centre de Saclay
Nano-Innov PC 172
91191 Gif sur Yvette Cedex

leti

Centre de Grenoble
17 rue des Martyrs
38054 Grenoble Cedex

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