Semi-Analytical Current Source Modeling of FinFET Devices Operating in Near/Sub-Threshold Regime with Independent Gate Control and Considering Process Variation

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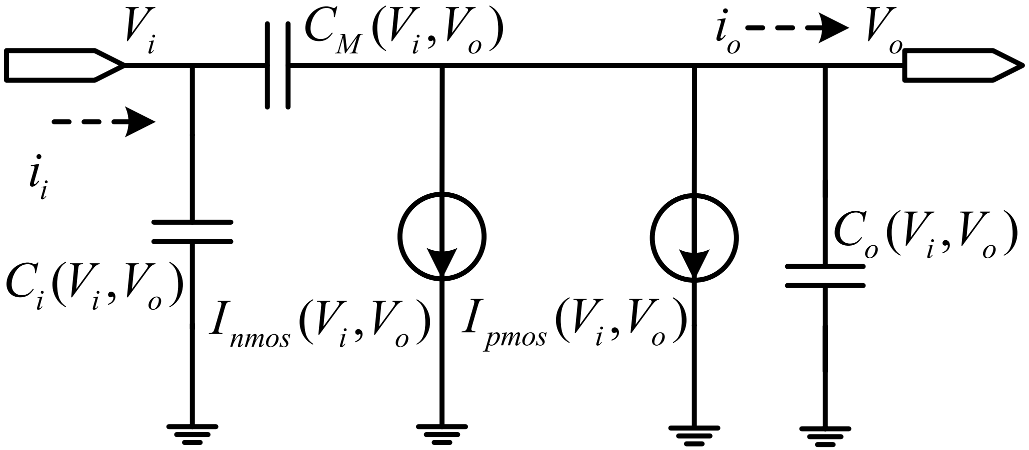
System Power Otimization and Regulation Technology

Outlines

- Introduction
  - Motivation
  - Extend CSM to FinFET Devices
- Characteristics of FinFET Devices
  - Independent Gate Control in FinFET
  - Process Variations in FinFET
- Semi-Analytical CSM for FinFET Devices
  - The Impact on the Threshold Voltage
  - Driving Current Modeling
  - Parasitic Capacitance Modeling
  - CSM LUT Construction
- Experimental Results

Motivation

- **Standard timing models and static timing analysis (STA) methods can not provide sufficient accuracy.**
- **Current Source Model (CSM) is an alternative approach that is much more effective in dealing with noise and variability in today's designs.**



Equivalent CSM for a CMOS inverter

Extend CSM to FinFET Devices

- Nanoscale FinFET devices are emerging as the transistor of choice in 14nm CMOS technologies and beyond.
- The needs to reduce power consumption in VLSI circuits are driving the push toward ultra-voltage scaled CMOS designs.
- We extend the CSM approach to handle VLSI circuits comprised of FinFET devices with independent gate control operating in the near/sub-threshold voltage regime and subject to process variations.
- *Method*: combine non-linear analytical models and low-dimensional CSM lookup tables to simultaneously achieve high modeling accuracy and time/space efficiency.

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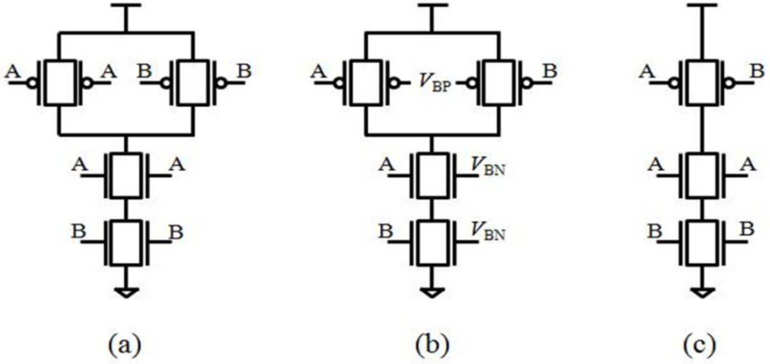
Independent Gate Control for FinFET Devices

- **The FinFET structure allows for fabrication of separate front and back gates.**
- **Each fin is essentially a parallel connection of the front-gate-controlled FET and the back-gate-controlled FET.**
- **The front and back gates can be tied to the same or different control signals, which allows for more feasible designs.**



Different FinFET-based NAND gate designs

- **The threshold voltage of the front-gate-controlled FET ($V_{th,F}$) varies in response to the back-gate voltage (V_{BN}), and vice versa.**

Process Variations in FinFET Devices

- **Two major sources of process variation in a FinFET transistor:**
  - ***Line-Edge Roughness*** **(LER): causes variation of the effective channel length, denoted by ΔL.**
  - ***Gate Work-Function Variation (*****WFV*****):*** **causes variation of the intrinsic threshold voltage, denoted by ΔV_{th0}.**
- **Build equivalent CSM for FinFET deivces considering these characteristics**
  - **Solution1: extend the standard CSM LUTs to high dimensions. (result in an unacceptable memory space requirement)**
  - **Solution2: store the LUTs when $\Delta V_{th0} = 0$ and $\Delta L = 0$, and apply polynomial corrections for process variations. (turn out to be both inaccurate and cost-ineffective)**
  - **Our solution: Semi-Analytical CSM**

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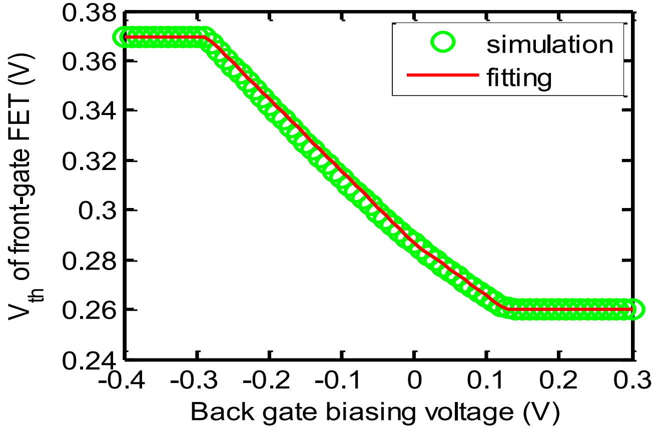
The Impact on the Threshold Voltage

- **Decreasing the back-gate voltage of the N-type fin results in the increase of V_{th} of the front-gate-controlled N-type FET.**
- **We use a piecewise linear function to represent the impact of the back-gate voltage V_{BN} on the change of the threshold voltage $V_{th}(V_{BN})$:**

$$V_{th}(V_{BN}) = \begin{cases} V_{th,max}, & V_{BN} < V_{BN,min} \\ k_1 V_{BN}, & V_{BN,min} \le V_{BN} < 0 \\ k_2 V_{BN}, & 0 \le V_{BN} < V_{BN,max} \\ V_{th,min}, & V_{BN} \ge V_{BN,max} \end{cases}$$



Driving Current Modeling

- **Considering both the back-gate voltage and process variations, the threshold voltage of the front-gate-controlled FET is given by** $V_{th,F} = V_{th0} + \Delta V_{th}(V_{BN}) + \Delta V_{th0}$.
- **Similarly, the threshold voltage of the back-gate-controlled FET is** $V_{th,B} = V_{th0} + \Delta V_{th}(V_{FN}) + \Delta V_{th0}$.
- I_N **(or** I_P**) is the sum of the driving currents of the front gate and the back gate:** $I_N = I_{FN} + I_{BN}$.
- $L = L_0 + \Delta L$
- **We fit** I_{FN} **with respect to** ΔL **and** ΔV_{th0} **based on the transregional model by using the functional form**
- $I_{FN}(V_{FN}, V_{BN}, V_{ds}, \Delta L, \Delta V_{th0}) = \frac{C(V_{FN},V_{ds})}{L} \cdot e^{A(V_{FN},V_{ds}) \cdot V_{th,F}^2 + B(V_{FN},V_{ds}) \cdot V_{th,F}}$
- $A(V_{FN}, V_{ds})$ **,** $B(V_{FN}, V_{ds})$**, and** $C(V_{FN}, V_{ds})$ **are some fitting parameters.**

Parasitic Capacitance Modeling

- **Generate similar analytical equations for parasitic capacitances associated with a FinFET gate in terms of the sources of variation and store corresponding regression coefficients.**

- **Linear curve fitting is able to capture the dependency of the equivalent capacitances on the above-mentioned parameters.**

CSM LUT Construction

- In the characterization phase:
  - Perform characterization as well as curve fitting as mentioned earlier and record the coefficient into the LUTs with index of interested voltage levels.
- In the evaluation phase:
  - Use the coefficient LUTs to construct the customized CSM LUTs including I_o, C_M, C_i and C_o under every voltage pair (V_i, V_o), under different corners of process variation parameters and bias voltage levels, e.g., ΔL, ΔV_{th0} and V_{BN}(or V_{FN}).
- The constructed CSM LUTs can be used to calculate the exact output waveform given the waveform of the input voltage.

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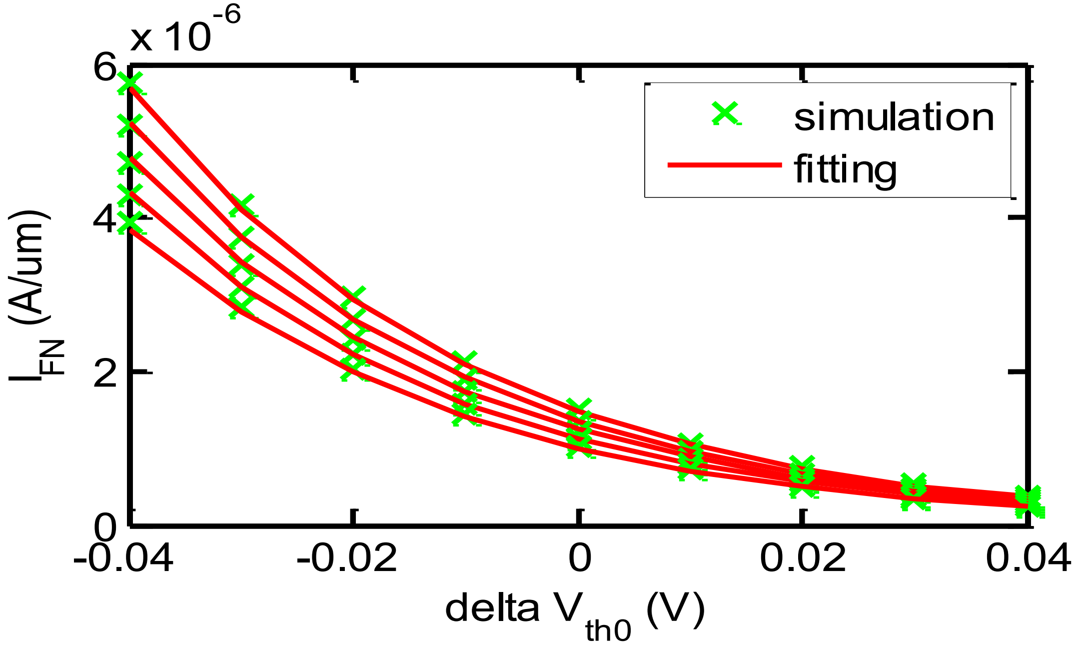
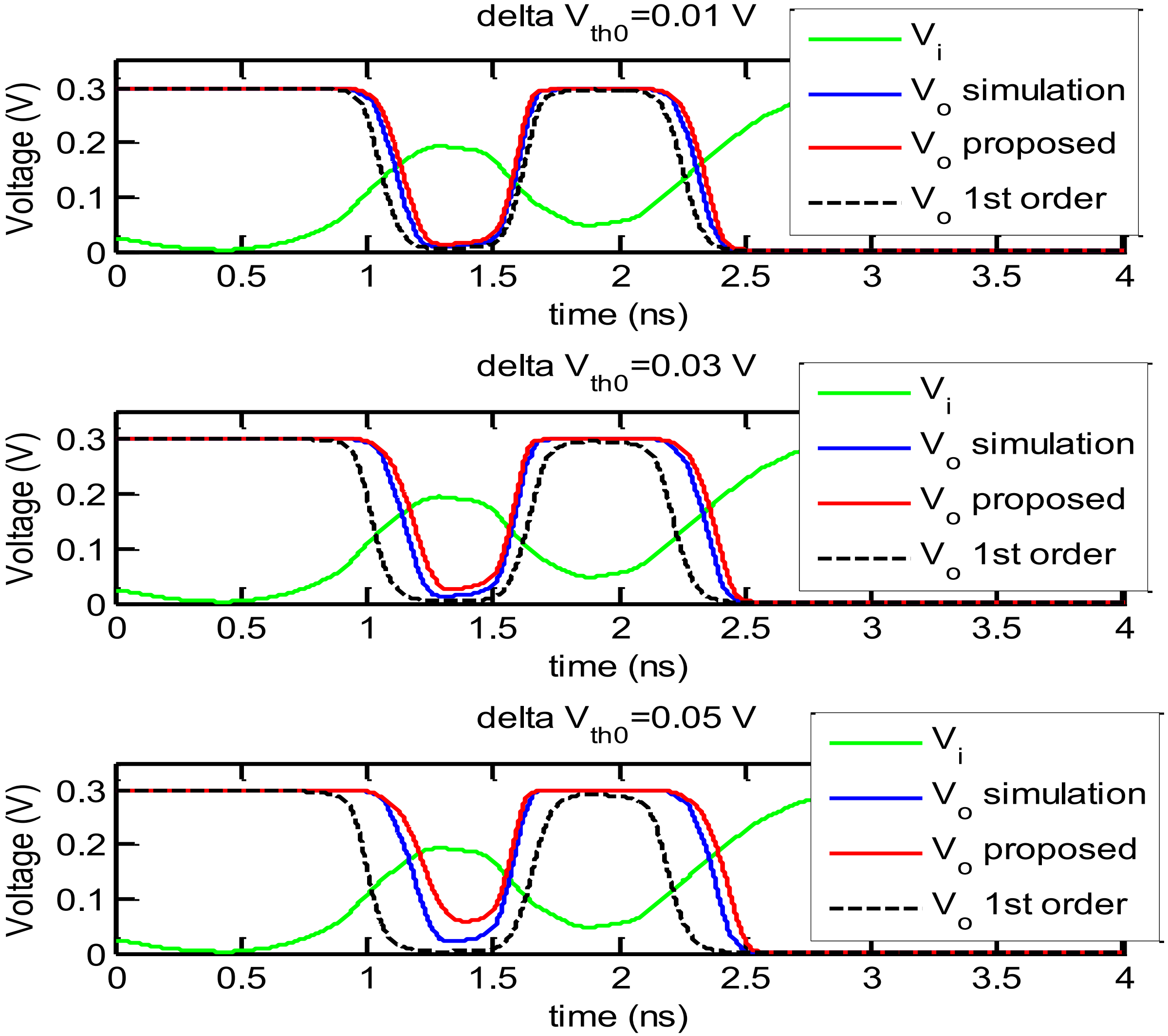
Fitting result of driving current

- **Our proposed method achieves very good fitting quality with an average error of 0.81%. The fittings of the driving currents are performed for every point (V_{FN}, V_{ds}).**



Curve fitting of N-type FET driving current under different corners of process variation

Output waveform under noisy input



Output waveforms for different CSM variation handing techniques under a noise input at different threshold voltage variation levels

Thank you

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