

# Time-domain Bound Analysis for Analog Circuits and Interconnect Circuits



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# Outline



- Background and motivation
- Review of graph based symbolic analysis
- Proposed performance bound analysis method
- Experimental results
- Summary

# Introduction



## Background

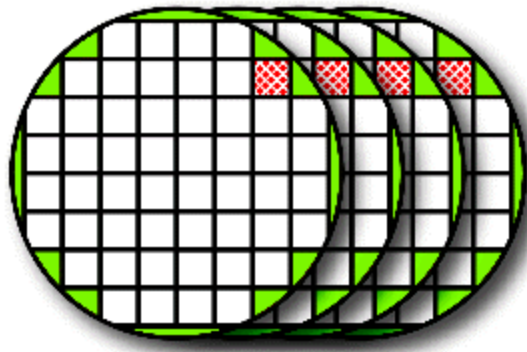
- In nanometer regime, such as 45 nm technology, process variations have huge impacts on circuit performance, yield, and reliability.
- Analog and mixed signal circuits are not only sensitive to process variations, but also suffer severely from mismatch influences, due to the inverse square root law.
- Mismatch of CMOS devices doubles for each process generation below 90 nm.

300mm wafer

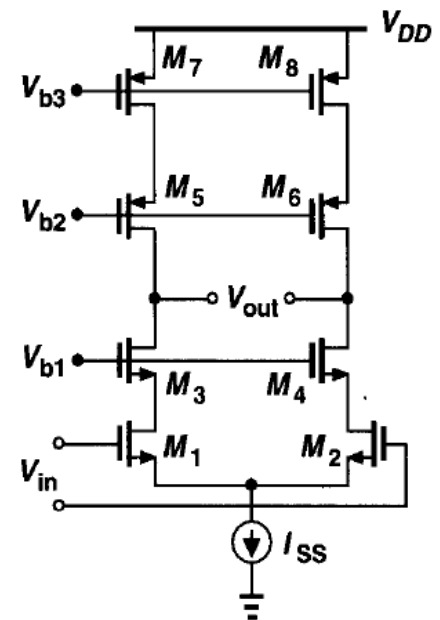
Wafer A, Wafer B, Wafer C...



(a) Site-to-site variation



(b) Wafer-to-wafer variation



# Existing approaches



- At the nanometer scale, circuit parameters are no longer truly deterministic and present themselves as **probability distributions**.
  - Designers must consider these effects to ensure robustness.
- Traditional **corner based** verification:
  - not accurate enough or too expensive to cover all the corners.
- **Monte-Carlo based** simulation and yield estimation: general and accurate; but expensive and slow.
  - Especially not efficient for high sigma and rare event analysis problems.
  - 3 sigma leads to 370 samples, but 5 sigma requires 1.75million samples.
- **Fast Monte Carlo** methods are proposed (by reducing variations or sampling discrepancy).
  - important sampling --- circuit specific (variation reduction).
  - Latin hypercube sampling --- doesn't work for all circuits (sampling discrepancy reduction).
  - Quasi Monte Carlo --- suffers the high-dim problems (sampling discrepancy reduction).

# Review of existing non-MC performance bound analysis

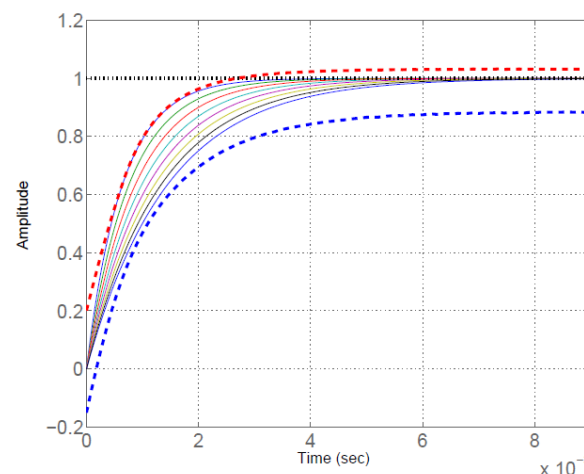


- Performance **bound analysis** methods emerged as attractive techniques for statistical analysis and yield estimation.
  - Has potential to more effectively deal with high dimensional and sigma problems.
- Recently some non-MC performance bound methods were proposed
  - [Qian, ICSICT'10] applies a control-based method to compute the bounds of the transfer function in frequency domain.
  - [Hao, DAC'11] applies graph-based symbolic analysis, control-method and affine interval methods to compute the bounds in frequency domain.
    - However, it uses affine interval method to compute variational transfer functions, which leads to over-conservative results.
  - [Saibua, ICVSOC'11] directly uses an optimization based method to get time domain performance bound.
    - Use whole circuits equations as constrains. Very expensive to enforce constrains.

# Review of existing non-MC performance bound analysis (cont'd)



- Recently some non-MC performance bound methods were proposed
  - [Liu, ASPDAC'12] compute the time-domain performance bound by first getting the bound in frequency domain and then convert it into time domain.
    - But the relaxation in signal can lead to issues in DC and steady state responses (TIDBA).
  - [Liu, ASPDAC'13] proposed optimization based method with symbolic analysis method to compute the performance bounds in frequency domain.
    - More accurate and can deal with device correlation issues.
    - But only work for frequency domain



We may have divergent steady state response for TIDBA

# Contribution



- We present a new non MC yield estimation method based on performance bound analysis in **time domain**.
- The exact transfer functions of linearized analog circuits are derived via a graph-based **symbolic analysis**.
- The time domain responses at every time step are obtained by **nonlinear constrained optimization**.
  - It ensures accurate bounds and also resolve the device correlation issues seen in the previous methods.
- Detailed studies for the high sigma analysis using the proposed bound analysis against MC method.
- Experimental results show that the proposed method can achieve one to two orders of magnitudes speedup over HSPICE's MC on benchmark analog circuits.

# Illustration by an example

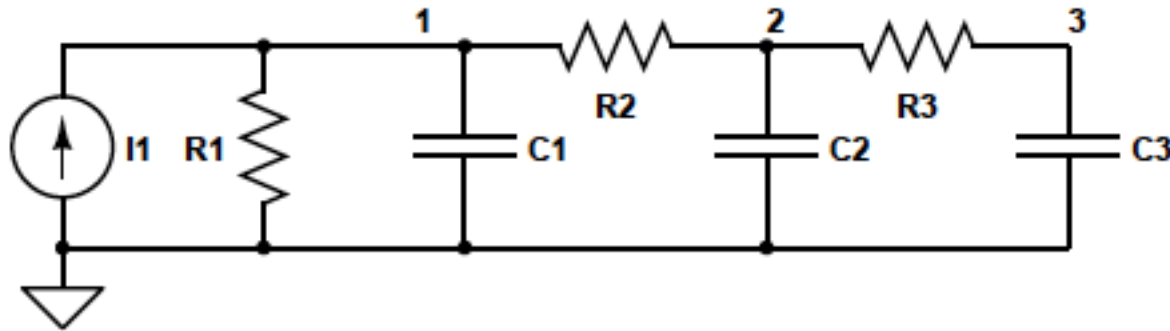


Fig. 1: RC ladder circuit

By MNA, we have

$$Y\vec{v}(n+1) = \vec{i}(n+1)$$

$$\begin{bmatrix} \frac{1}{R_1} + \frac{1}{R_{c1}} & -\frac{1}{R_2} & 0 \\ -\frac{1}{R_2} & \frac{1}{R_2} + \frac{1}{R_{c2}} + \frac{1}{R_3} & -\frac{1}{R_3} \\ 0 & -\frac{1}{R_3} & \frac{1}{R_3} + \frac{1}{R_{c3}} \end{bmatrix} \vec{v}(n+1) = \begin{bmatrix} v_1(n+1) \\ v_2(n+1) \\ v_3(n+1) \end{bmatrix}$$

where  $R_{c1} = \frac{C_1}{\Delta t}$ ,  $R_{c2} = \frac{C_2}{\Delta t}$ ,  $R_{c3} = \frac{C_3}{\Delta t}$ ,  $i_{c1}(n) = \frac{v_1(n) * C_1}{\Delta t}$ ,  $i_{c2}(n) = \frac{v_2(n) * C_2}{\Delta t}$ ,  $i_{c3}(n) = \frac{v_3(n) * C_3}{\Delta t}$  and  $\Delta t$  is the time step size.

# Illustration by an example



By the Cramer's rule, we have

$$v_i(n+1) = \frac{\det(Y_i(n+1))}{\det(Y)}$$

Where  $Y_i(n+1)$  is formed by replacing its  $i$ th column by  $i(n+1)$ ,  
As a result, we have

$$v_i(n+1) = \frac{f_{n,i}(C1, C2, C3, R1, R2, R3, v_1(n), v_2(n), v_3(n))}{f_{d,i}(C1, C2, C3, R1, R2, R3, v_1(n), v_2(n), v_3(n))}$$

In general, we have the following general performance expressions  
in terms of circuit parameters

$$v_i(n+1) = \frac{f_i(p_1, \dots, p_m, v_1(n), \dots, v_k(n))}{f_{d,i}(p_1, \dots, p_m)}$$

# Finding the performance bound

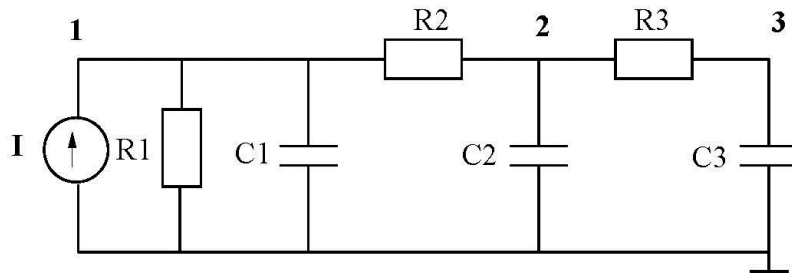


The we find the bound by the non-linear constrained optimization at each time step  $n$

$$\begin{array}{ll} \text{minimize} & v_i(n+1)(\mathbf{x}) = f_i(\mathbf{x}) \\ \text{subject to} & \mathbf{x}_{\text{lower}} \leq \mathbf{x} \leq \mathbf{x}_{\text{upper}}, \end{array}$$

Where  $\mathbf{x} = [\mathbf{p}, \mathbf{v}]$  and  $\mathbf{p} = [p_1, p_2, \dots, p_m]$ ,  $\mathbf{v} [v_1(n), v_2(n), \dots, v_k(n)]$

# Determinant Decision Diagram



MNA

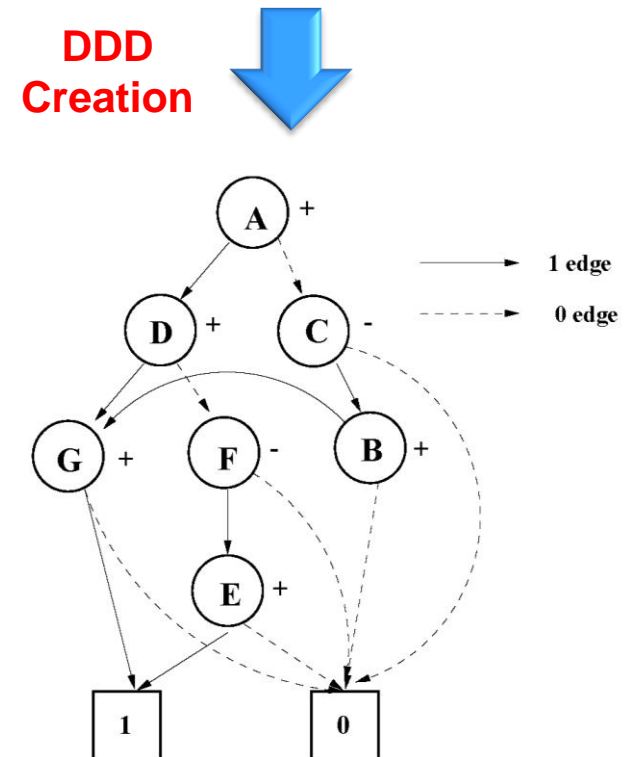


$$\begin{bmatrix} A & B & 0 \\ C & D & E \\ 0 & F & G \end{bmatrix} \begin{bmatrix} H \\ I \\ J \end{bmatrix} = \begin{bmatrix} K \\ 0 \\ 0 \end{bmatrix}$$

Symbolic transfer function

$$H(s) = \frac{N(s)}{D(s)} = \frac{\sum_{i=0}^m \hat{a}_i s^i}{\sum_{j=0}^n \hat{b}_j s^j}$$

DDD  
Expansion



- Parametric frequency response
- Good for interactive design aid
- DDD is efficient dealing with exponential symbol complexity

# Proposed performance bound analysis method in a nutshell



- Time-domain symbolic modified nodal analysis equations of the circuit at a time step are formed.
- Closed-form expressions of interested performance with respect to varying parameters are derived via a graph-based **symbolic analysis**.
- The lower bound and upper bound of interested performance of circuits with respect to variational parameters are obtained by **nonlinear constrained optimization** at each time step.
  - Much more accurate and less conservative than the previous methods.
  - But still finding the bounds by optimization at each step is a still relaxation to the state reachability reaching analysis.
- Detailed study for the proposed method for high-sigma analysis
  - For MC method, the time complexity increases rapidly (almost exponentially) as sigma increases.
  - For proposed method, run time to compute high-sigma bounds remains the same as it just uses different parameter bounds.

# Proposed performance bound analysis method



$$Gx(t) + C \frac{dx(t)}{dt} = BU(t)$$



1

$$Gx(t_n) + C \frac{x(t_n) - x(t_{n-1})}{\Delta t} = BU(t_n)$$



2

$$x(t_n) = f(C, G, B, \Delta t, U(t_n), x(t_{n-1}))$$



6

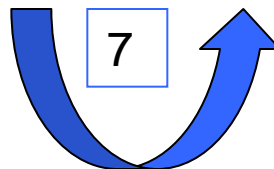
$$\text{Max/Min: } x(t_n) = f(C, G, B, \Delta t, U(t_n), x(t_{n-1}))$$

Subject to

$$G_{ij}^{lower} \leq G_{ij} \leq G_{ij}^{upper}$$

$$C_{ij}^{lower} \leq C_{ij} \leq C_{ij}^{upper}$$

4



7

$$x_i^{lower}(t_{n-1}) \leq x_i(t_{n-1}) \leq x_i^{upper}(t_{n-1})$$

5

**Input:** Circuit netlist, bounds of selected parameters.

**Output:** Conservative performance bound of interests

- 1: Convert the circuit C and L elements into companion models
- 2: Generate symbolic expression of closed form expressions for interesting nodes
- 3: **for** each time step **do**     *// Perform transient analysis*
- 4:     Set bounds on process variational parameters.
- 5:     Set bounds on the voltage or current states from results of optimization of last time step.
- 6:     Run nonlinear constrained optimization (9) which uses closed form function as the objective. to find upper bound and lower bound.
- 7:     Save bound information for the optimization of next time step.
- 8: **end for**
- 9: Output the bound of voltage or current on every time step.

# Active-set based optimization for computing freq domain bounds



- Solutions to constrained nonlinear optimization problems
  - Active-set method, Interior point method, trust region method
  - Iterative approaches starting with initial guess
- Active set method:
  - Two-phase iterative method
  - First phase, the objective function is ignored while a feasible point is found.
  - Second phase, objective is minimized while feasibility is maintained by method like quadratic programming.
  - But still a localized search method.

Active set is the set of constraints that are satisfied with equality

# Numerical Result



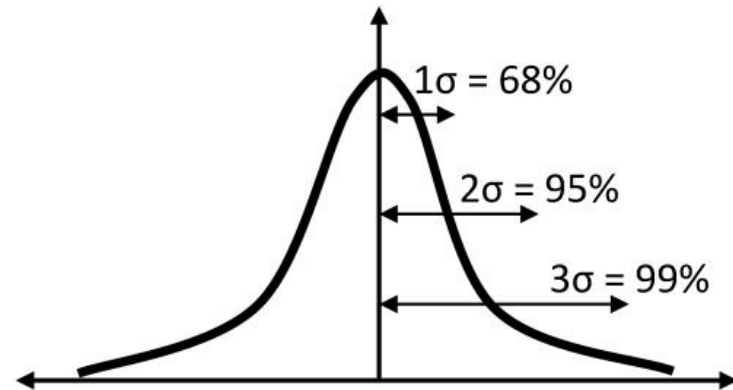
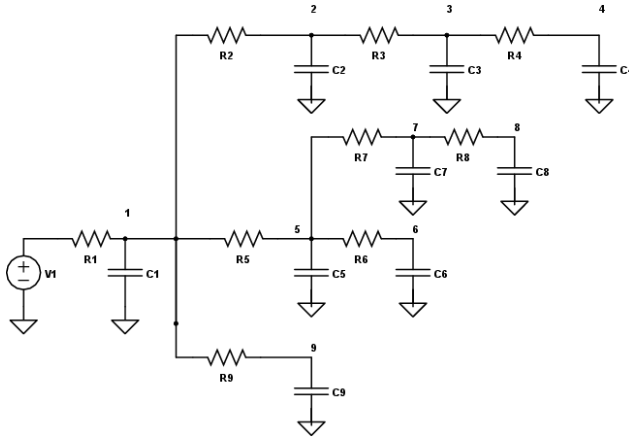
## ● Experiment Setup

- DDD symbolic tool (C++ language) generates the exact transfer function expressions first.
- All the follow-up optimization based bound analysis is done in MATLAB.
- The nonlinear constrained optimization is solved by fmincon function in Matlab.
- All running time are sampled from a Linux server with a 2.4 GHz Intel Xeon Quad-Core CPU and 36GB memory.
- We compare proposed method with Monte-Carlo method.

# RC tree circuit



- An RC tree circuit



- Interested performance is the voltage of node 8

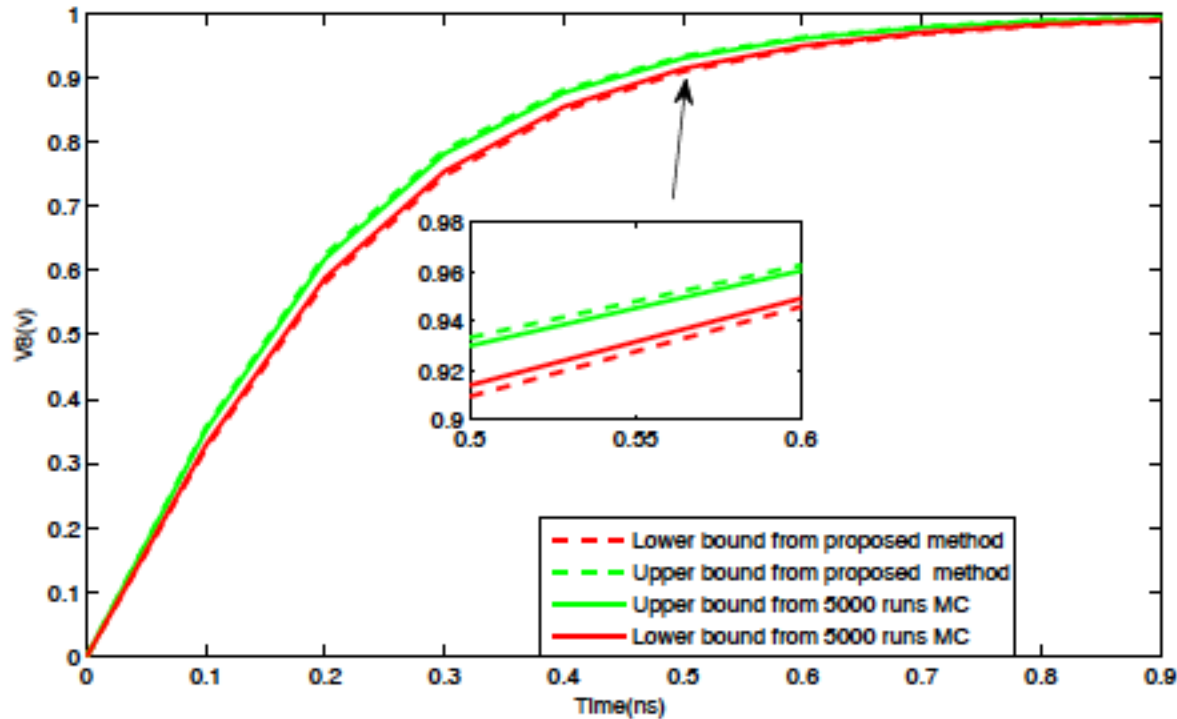
- Variational Parameters are:

$$R_i = 0.1\Omega$$

$$C_i = 0.1pf$$

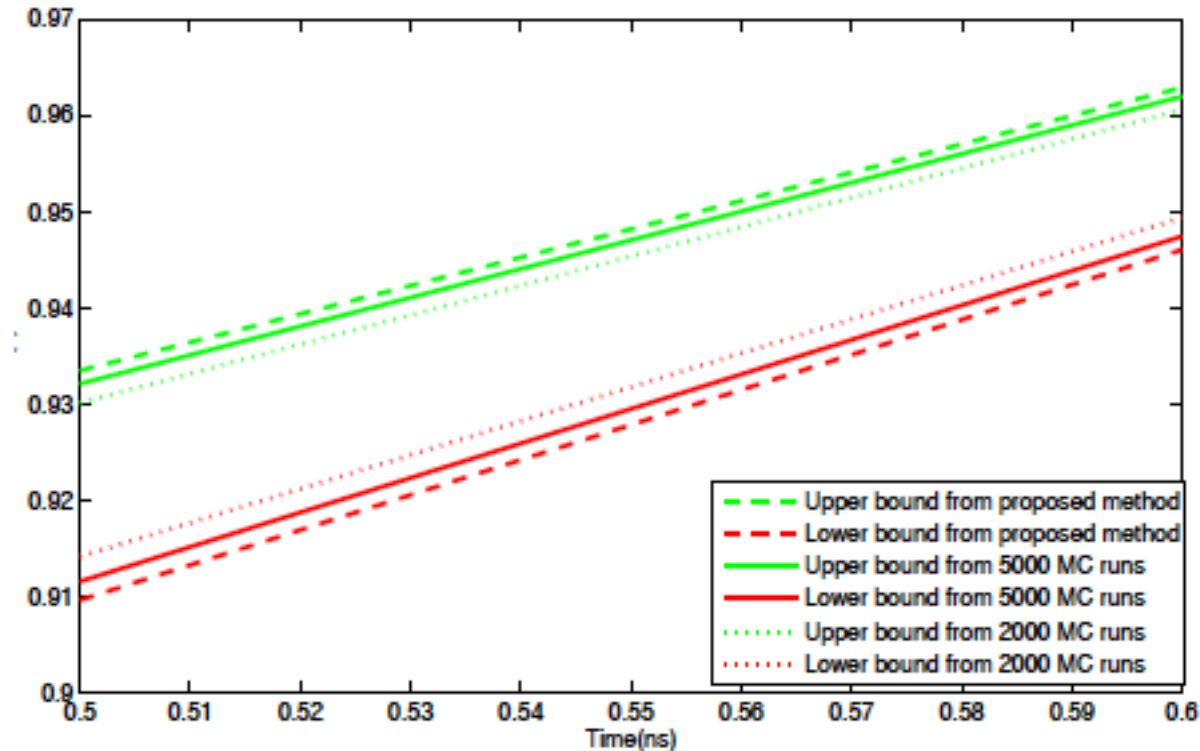
- $R_i, i=1,2,3$   $C_i, i=1,2,3$
- All variational parameters are in Gaussian Distribution.
- 3-sigma bound is used for parameters first
  - For proposed method, variational bound for a specific variational parameter is  $[\mu - 3\sigma, \mu + 3\sigma]$

# Results against 5000 MC runs



The bounds of  $V_8$  node obtained from 5000 MC run and the proposed method On the RC tree circuit. The proposed bound the MC runs.

# The comparison between different MC runs



The comparison of bounds of V8 node from 2000 MC runs, 5000 MC runs and the proposed method. As with more MC runs, the difference becomes smaller

# Error and speedup studies



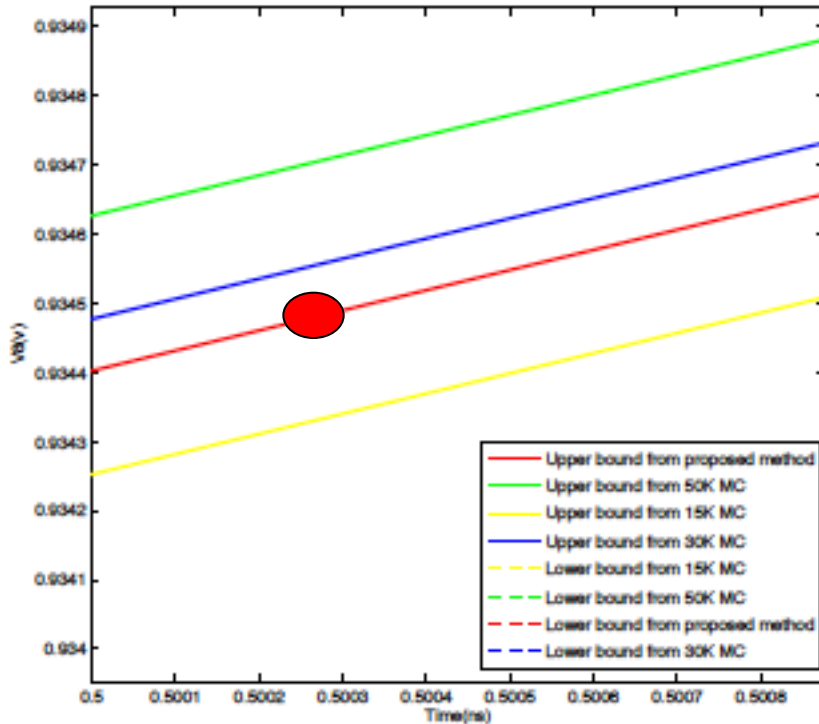
Method	Sampling #	CPU (sec)	Voltage (v)	%Difference
Monte Carlo	2000	573.38	0.915	0.55
Monte Carlo	5000	1490.79	0.912	0.22
Proposed	1	180.43	0.910	N/A

The comparison for low bounds of V8 at  $t = 0.5\text{ns}$  for the RC tree circuit

# More study for MC runs

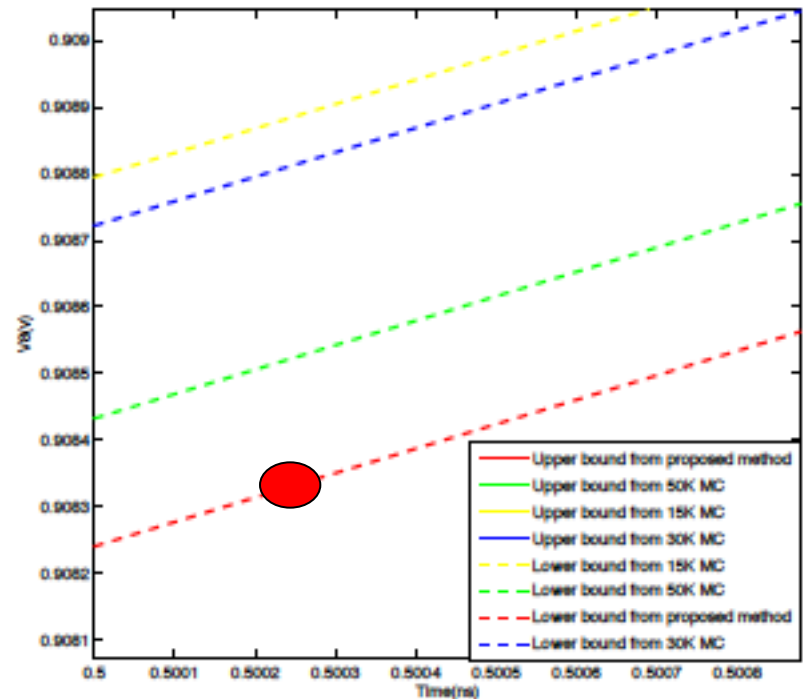


Comparison of 3 sigma bound of V8 from proposed method and that from 15K, 30K and 50K MC runs.



Upper Bound

The performance bound is not monotonic functions of some parameters.



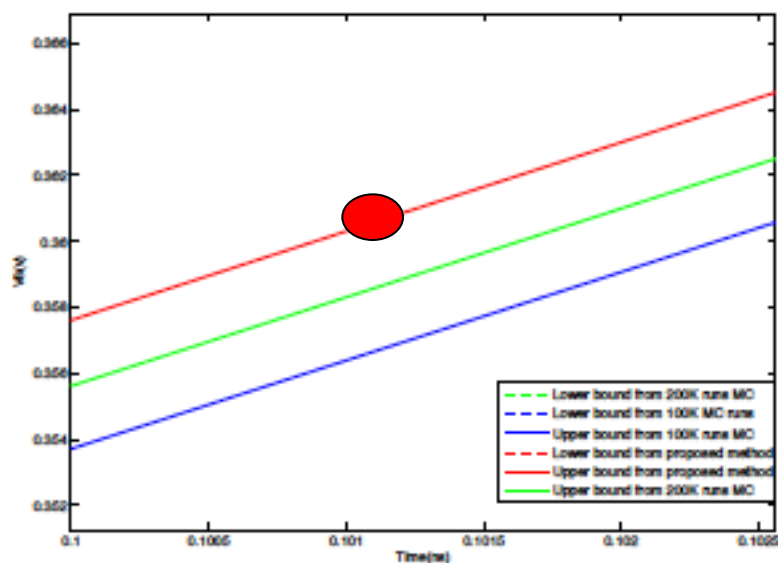
Lower Bound

Minimum is achieved when most of variational parameters are at edge of Gaussian distribution

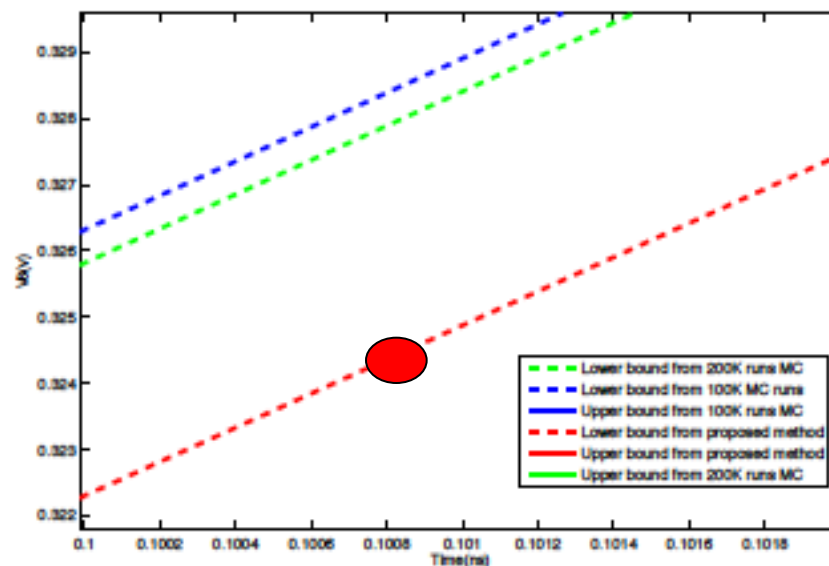
# High sigma bound results



- 4-sigma bound: The constrained range for variational parameters used in proposed method is  $[\mu - 4\sigma, \mu + 4\sigma]$
- Comparison of 4 sigma bound of V8 from proposed method and that of from 100K, 200K Monte-Carlo runs.



(a) Upper bounds

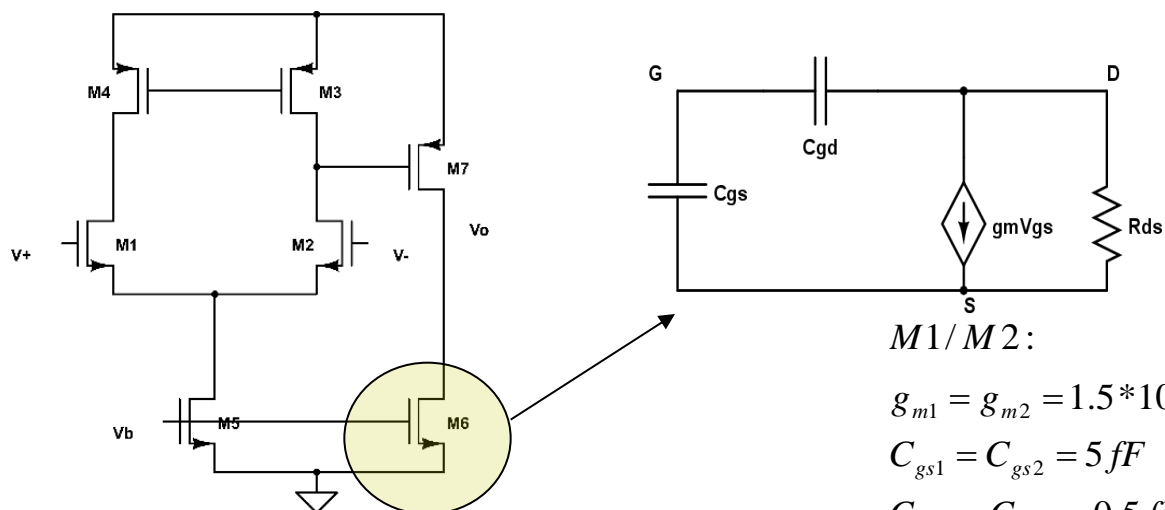


(b) Low bounds

# An amplifier circuit example



- Amplifier Circuit



$M1/M2:$

$$g_{m1} = g_{m2} = 1.5 \times 10^{-5} \Omega^{-1}$$

$$C_{gs1} = C_{gs2} = 5 \text{ fF}$$

$$C_{gd1} = C_{gd2} = 0.5 \text{ fF}$$

$M5/M6:$

$$r_{ds5} = r_{ds6} = 5 \times 10^7 \Omega$$

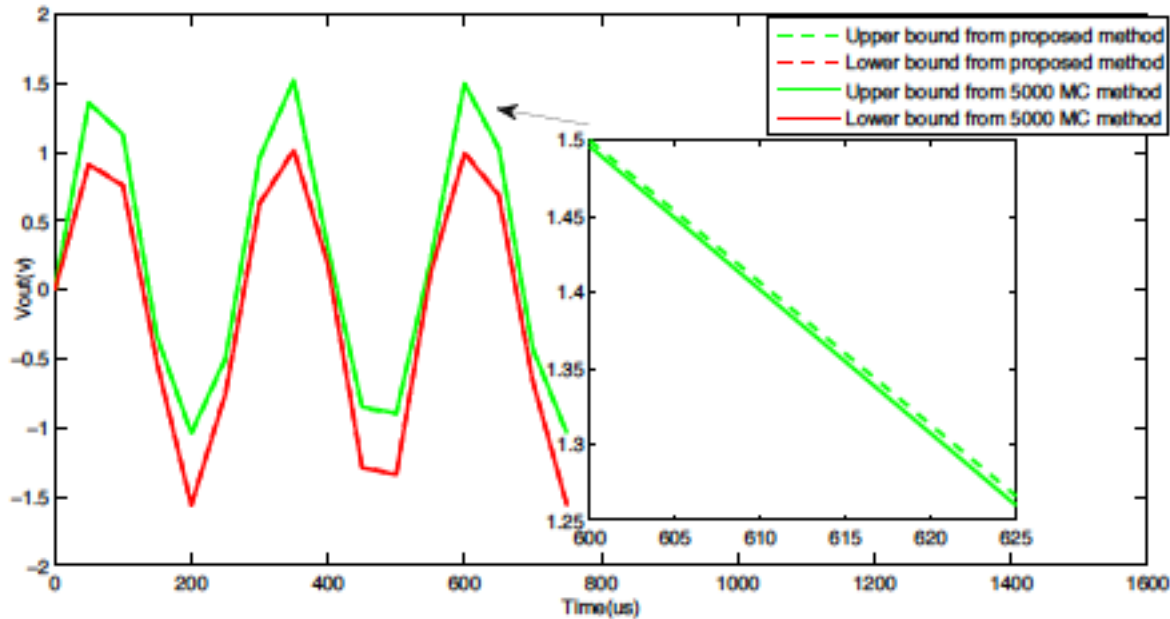
- The interested performance is  $V_o$ .

- The variational parameters are:

- M1:  $g_m, C_{gd}, C_{gs}$  M2:  $g_m, C_{gd}, C_{gs}$  M5:  $r_{ds}$  M6:  $r_{ds}$
- All variational parameters have Gaussian Distribution.
- For proposed method, variational bound for a specific variational parameter we choose is

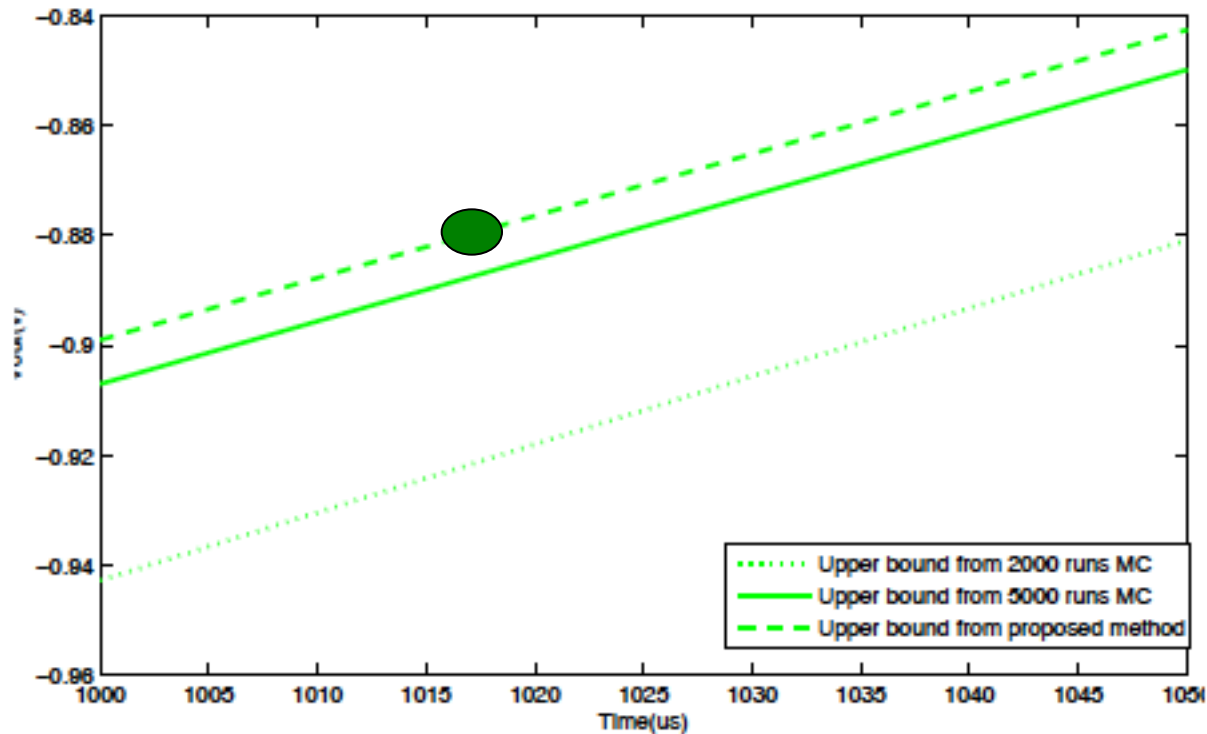
$$[\mu - 3\sigma, \mu + 3\sigma]$$

# Results for 5000 MC runs



The bounds from 5000 MC runs and the proposed method for the amplifier circuit. The two funds are almost same.

# More detailed analysis



The comparison of upper bounds of  $V_{out}$  from 2000 MC, 5000 MC runs  
Between the MC and proposed method on the amplifier circuit.

The proposed method contains all the MC runs.

# Error and speedup studies



Method	Sampling#	CPU (sec)	Voltage (v)	%Difference
Monte Carlo	2000	412.07	-0.942	3.7
Monte Carlo	5000	1112.59	-0.906	0.79
Proposed	1	105.46	-0.899	N/A

# Summary and future works



## ● Summery

- Proposed a new non-Monte-Carlo based performance bound analysis method.
- New method is based on symbolic analysis and nonlinear optimization techniques.
- More amenable for statistical analysis for high dimensional and computing high sigma bounds.

## ● Future Work

- Need to extend the method to nonlinear analog circuits.
- Need to try hierarchical DDD analysis methods to deal with large analog circuits.
- Need to further study the high sigma bound properties of the proposed method

# Some references



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