Routability-Driven Bump Assignment for Chip-Package Co-Design

2014/4/11

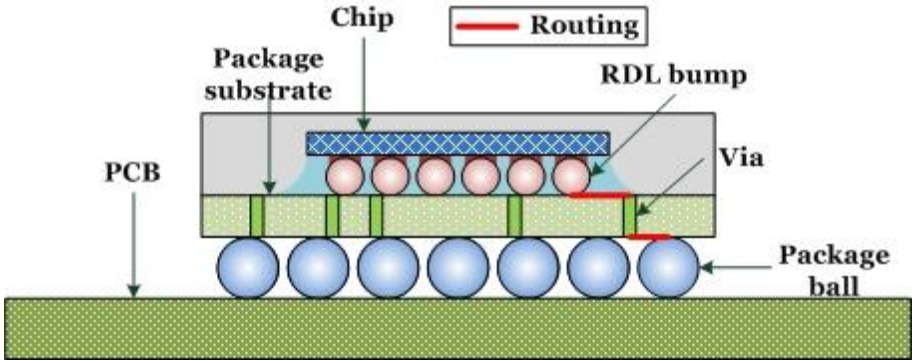
Presenter: Hung-Ming Chen

Outline

- **Introduction**
  - **Motivation**
  - **Previous works**
  - **Our contributions**
- Preliminary
- Problem formulation
- Bump assignment and package planning
- Experimental results
- Conclusions

Motivation

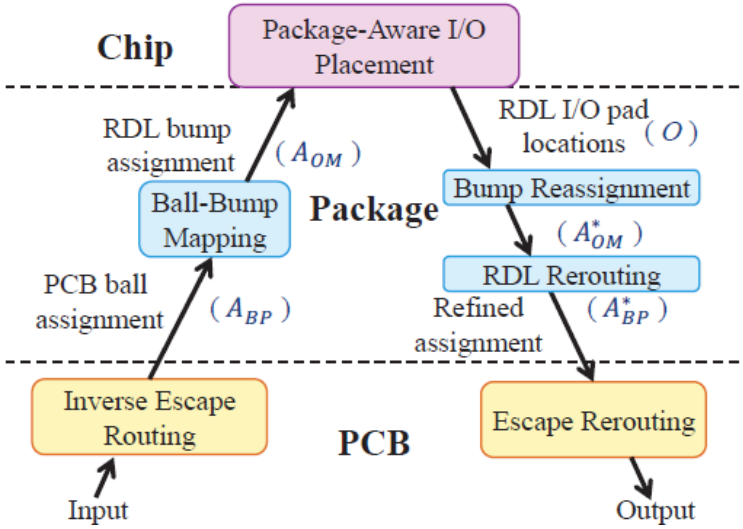
- Chip-package co-design problem



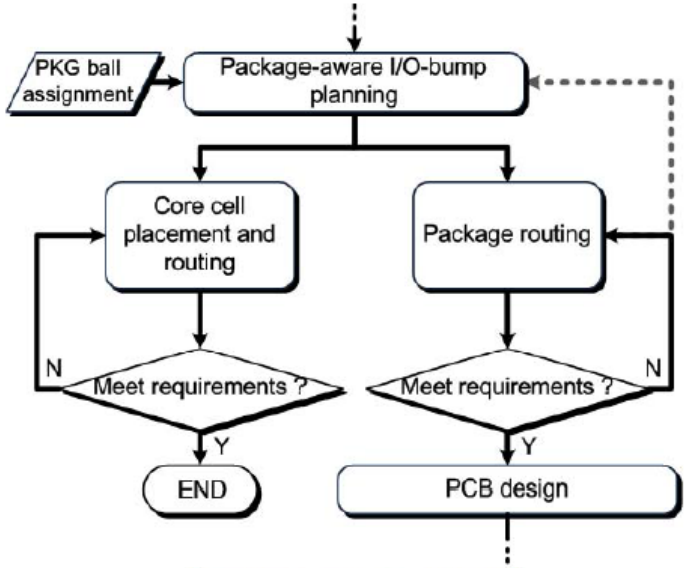
- It is a bottleneck to simultaneously optimize both pin assignment and pin routing for different design domains (chip, package, and board).
  - Huge manual efforts
  - Multiple design iterations

Previous Works

- Cross-domain co-design methodology
  - A board-driven Λ-shaped co-design flow [1]
  - A concurrent design flow [2]



[1] H. C. Lee and Y. W. Chang, "A chip-package-board co-design methodology," in *Proc. of ACM/IEEE Design Automation Conference, pp. 1082-1087, 2012.*



[2] R. J. Lee and H. M. Chen, "A study of row-based area-array I/O design planning in concurrent chip-package design flow," in *Proc. of ACM Trans. on Design Automation of Electronic Systems, vol. 18, no. 2, pp. 1-19, 2013.*

Our Contributions

- A fast heuristic for chip-package co-design
  - **A bump assignment** which introduces high routability both in RDL routing and substrate routing (100% in our real case).
  - **A practical RDL layout**.
  - **A routing order** that guides designers to easily finish net connection **on package**.
- A simulator: improper I/O-ball mapping can be fixed in the early stage.

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- **Preliminary**
  - **Pseudo single redistribution layer**
  - **Substrate routing**
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Pseudo Single RDL

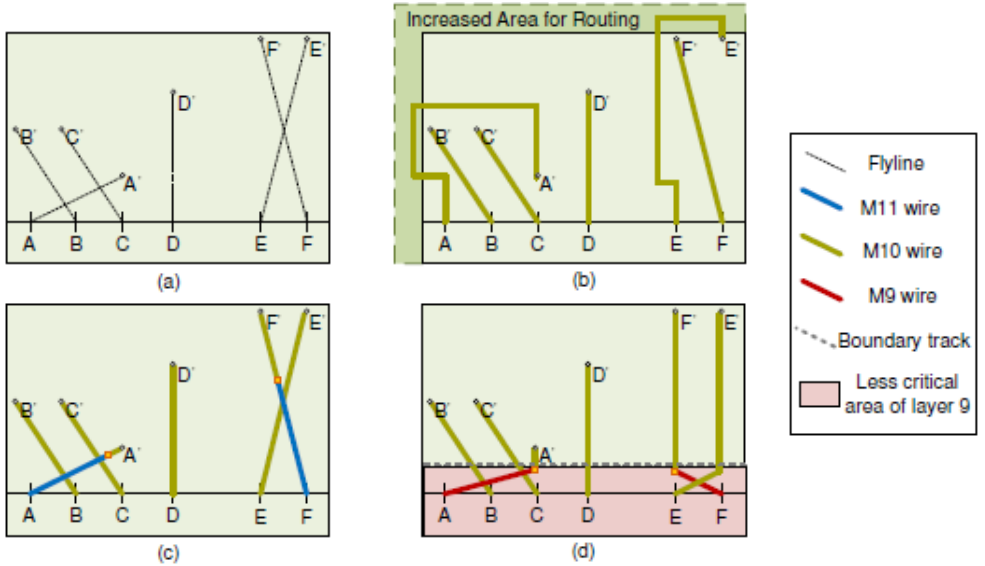
a) Congested RDL

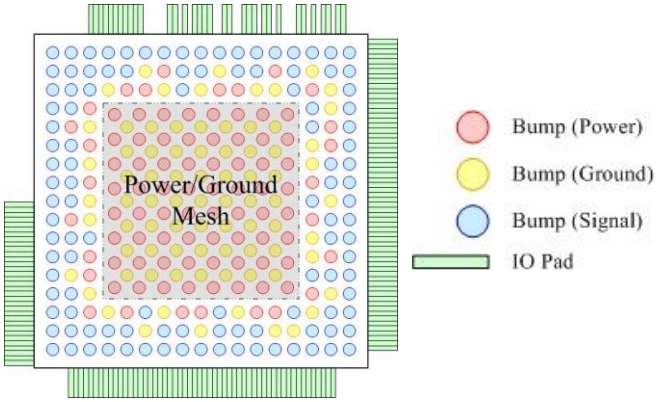
b) Extra routing area

c) Extra metal layer

d) Pseudo single-layer [3]

- M9 is mainly for PG
  - Use less critical area
  - Avoid additional layers
- Cost-effective
- Existing style in manual routing

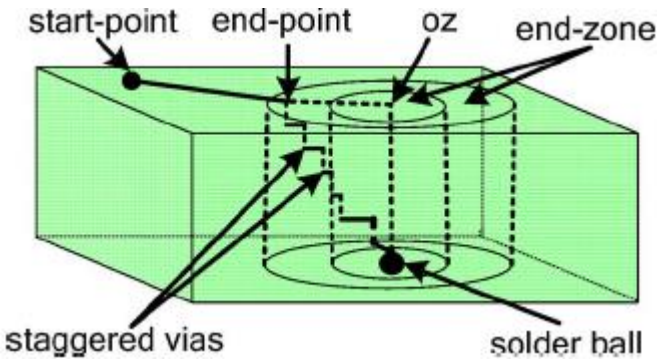


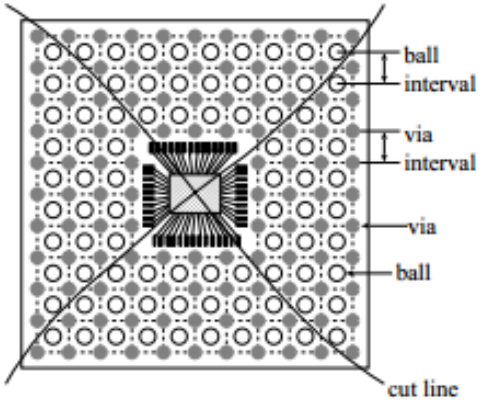


[3] H. W. Hsu, M. L. Chen, H. M. Chen, H. C. Li, and S. H. Chen, "On effective flip-chip routing via pseudo single redistribution layer," in Proc. of Design, Automation and Test in Europe Conference and Exhibition, pp. 1597-1602, 2012.

Substrate Routing

- Substrate routing is preferred to be **planar**, even though multiple routing layers are available [4].
  - The signal vias are allowed in very limited locations due to **manufacturability**, leaving space for P/G vias.
  - Vertical detour introduce extra vias, which may destroy the **signal integrity** for high-speed differential signals.





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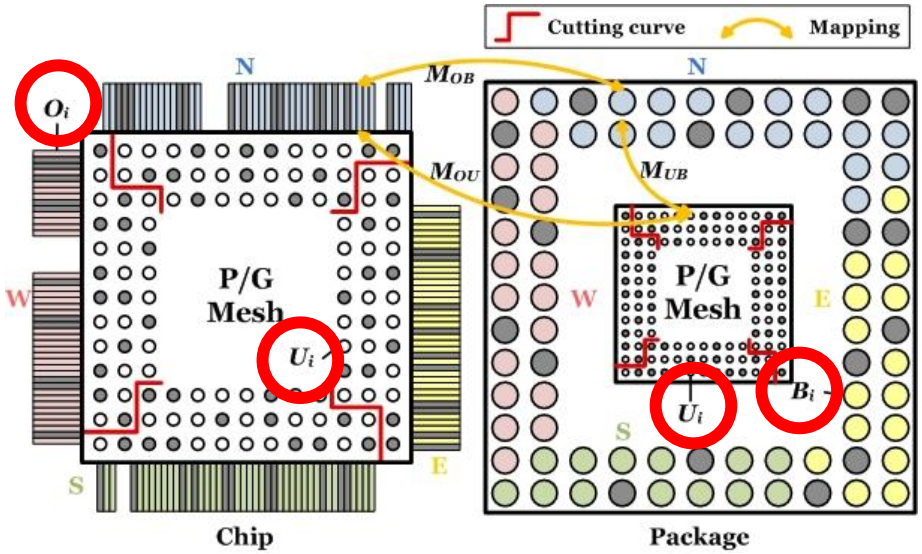
Problem Formulation

- Input
  - I/O pin sequence ***O***.
  - Ball matrix ***B***.
- Output
  - Bump assignment ***U***.
  - Physical RDL layout.
  - An illustration of planar substrate routing.



- Objective
  - Chip: maximize routability in RDL routing and minimize routing area borrowed from another existing metal layer.
  - Package: maximize routability in substrate routing.

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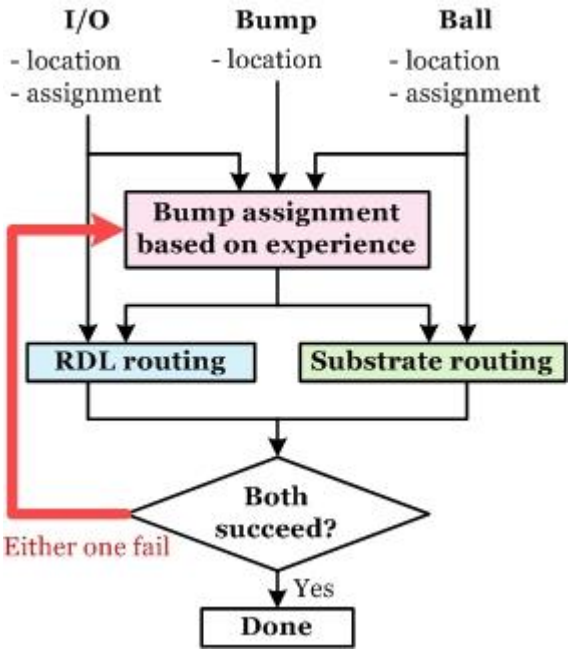
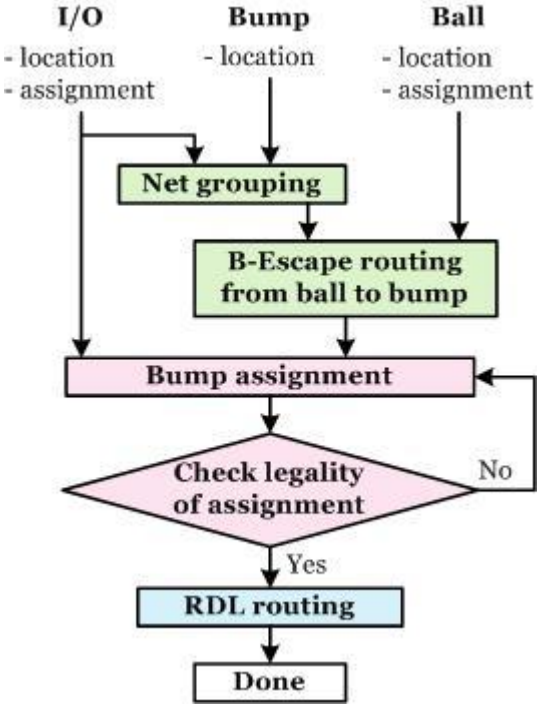
Design Flow

- Traditional flow costs more human resource and time because of the **iteration**.



- We propose a **straightforward** co-design flow to automatically solve the problem in a short time.



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- **Bump assignment and package planning**
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  - **Substrate routing**
    - **B-Escape routing**
    - **Net grouping**
  - Bump assignment
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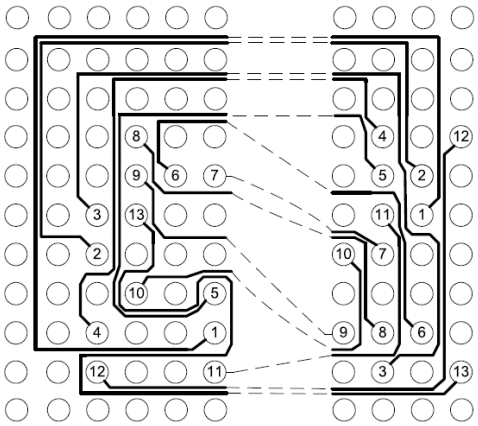
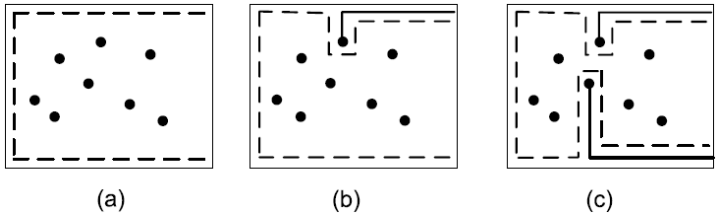
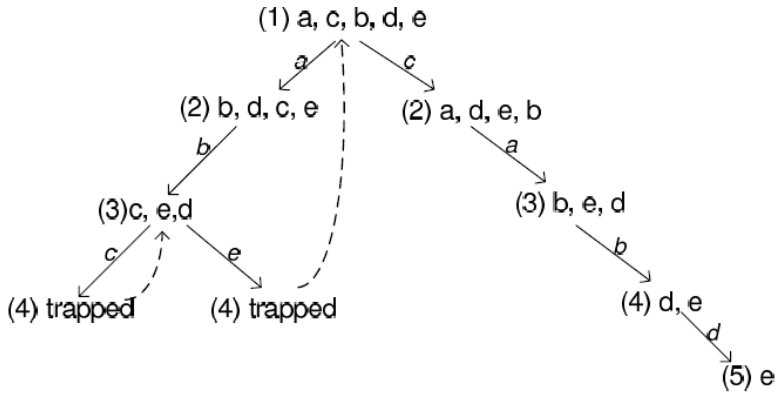
B-Escape Routing Algorithm

- A **simultaneous escape** is to find planar escape solutions in both components so that they are honoring the same escape ordering.
- Two major techniques:
  - Boundary routing
  - Dynamic net ordering



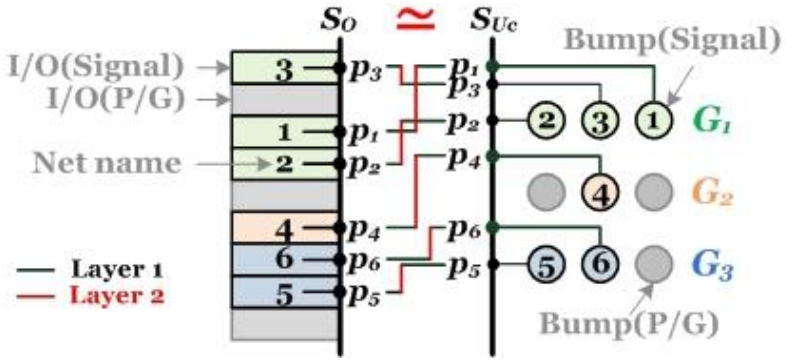


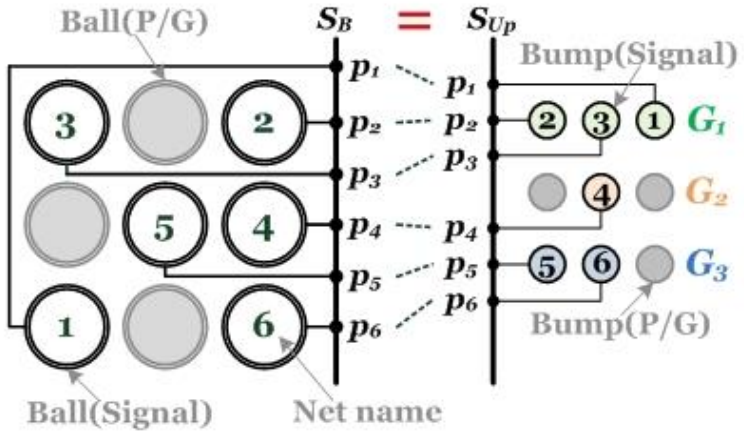


[5] L. Luo, T. Yan, Q. Ma, M. D. F. Wong, and T. Shibuya, "B-escape: a simultaneous escape routing algorithm based on boundary routing," in *Proc. of International Symposium on Physical Design, pp. 19-25, 2010.*

Detailed Structure

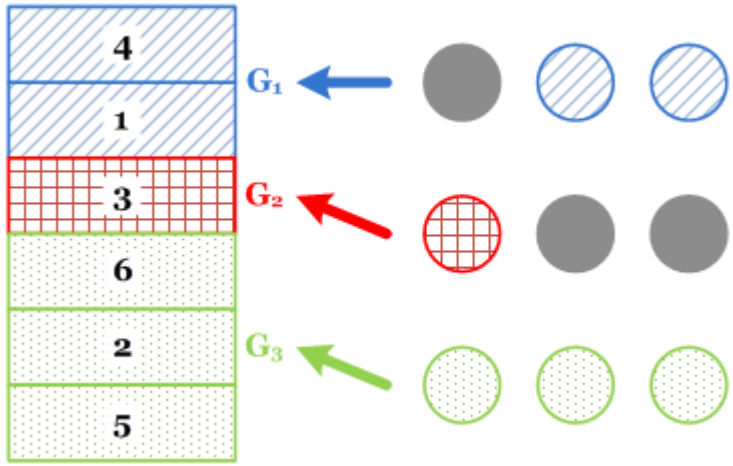
- Four pin sequences specify the relations among I/O, bump, and ball: $S_O \simeq S_{Uc} \simeq S_{Up} = S_B$
  - S_O: I/O pin sequence.
  - S_{Uc}: a row-based projection of bump matrix on chip.
  - S_{Up}: a row-based projection of bump matrix on package.
  - S_B: the escape pin order of ball.





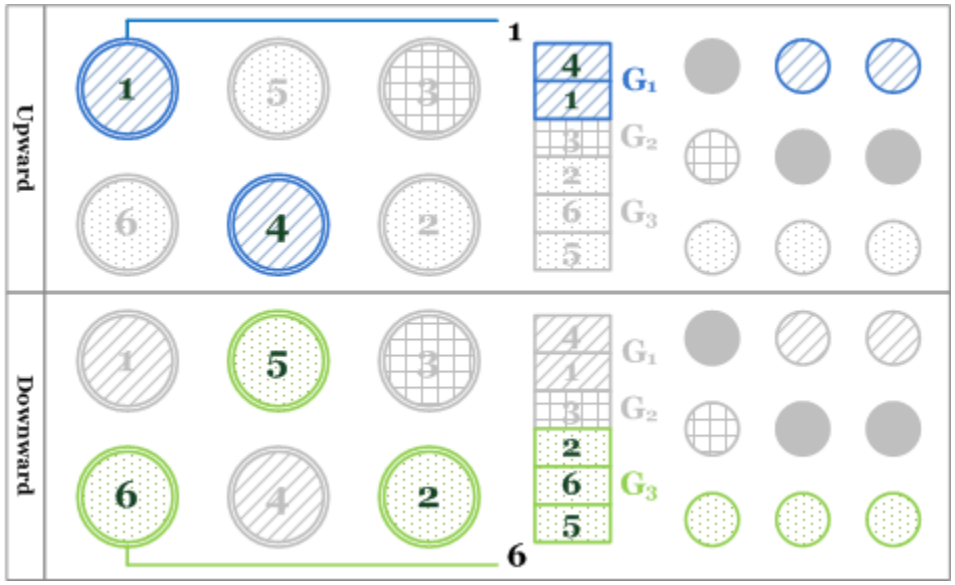
Net Grouping

- We introduce I/O information into B-Escape routing algorithm by net grouping technique.
  - To simultaneously achieve high routability in both RDL routing and substrate routing.
  - Group nets based on:
    - I/O pin sequence
    - # bumps in a row
  - Cost: $(\alpha, \beta) \rightarrow (\alpha, \beta, \gamma)$
    - α: *trapped*
    - β: *blocked*
    - γ is the group of net.



Cost Ordering

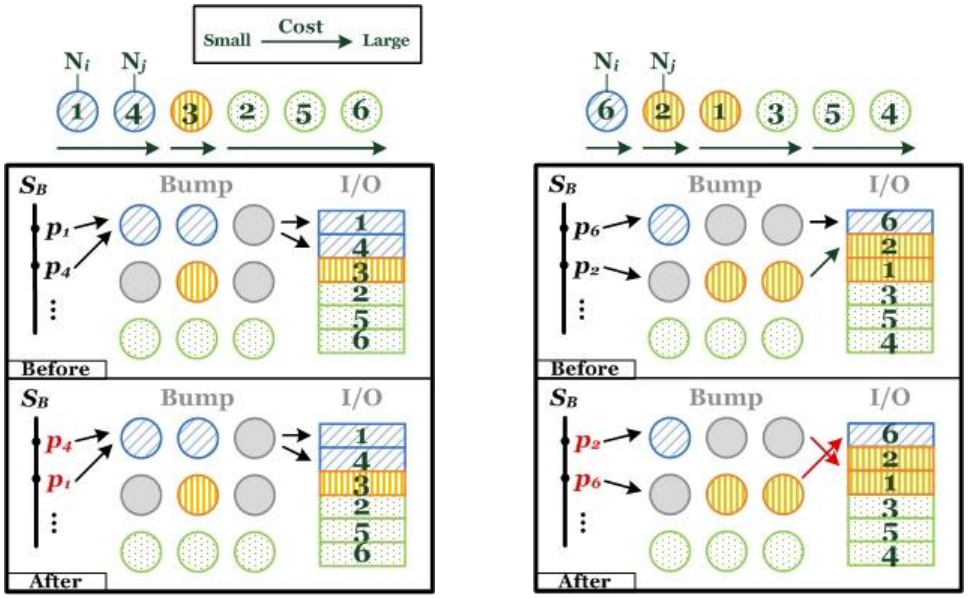
- Inside group: non-decreasing order based on $\boldsymbol{\alpha}$ and $\boldsymbol{\beta}$.
- Between groups: based on $\boldsymbol{\gamma}$.
  - Upward mode: $G_1, G_2, G_3, \ldots, G_n$
  - Downward mode: $G_n, \ldots, G_3, G_2, G_1$



Backtrack and Reorder

- While backtracking:
  - N_i and N_j are in the same group **(higher priority)**
  - N_i and N_j are in different groups

  where N_i is the chosen net and N_j is the next candidate net



Reformation of B-Escape

- **Step1**: calculate routing cost of each net
- **Step2**: sort net costs
- **Step3**: route the first net or backtrack

Algorithm 1 Reformation of B-Escape routing algorithm

```
1:  for each of the six routing mode do
2:      for each unrouted net N_i do
3:          route net N_i from ball B_i to escape boundary S_B
4:          calculate the cost vector for net N_i
5:          clear the route generated for net N_i
6:      end for
7:      if upward mode then
8:          sort all net costs by group in non-decreasing order
9:      else
10:         sort all net costs by group in non-increasing order
11:     end if
12:     for each group do
13:         sort net costs by α and β in non-decreasing order
14:     end for
15:     choose the first net N_j
16:     if net N_j traps other nets then
17:         backtrack and reorder
18:     else
19:         route net N_j from ball B_j to escape boundary S_B
20:         remove net N_j from net cost order
21:     end if
22:     until all nets are routed or exceed the backtrack limit
23:     store the solution for this routing mode
24: end for
25: output the solution with the best routability
```

- Between groups
- Inside group

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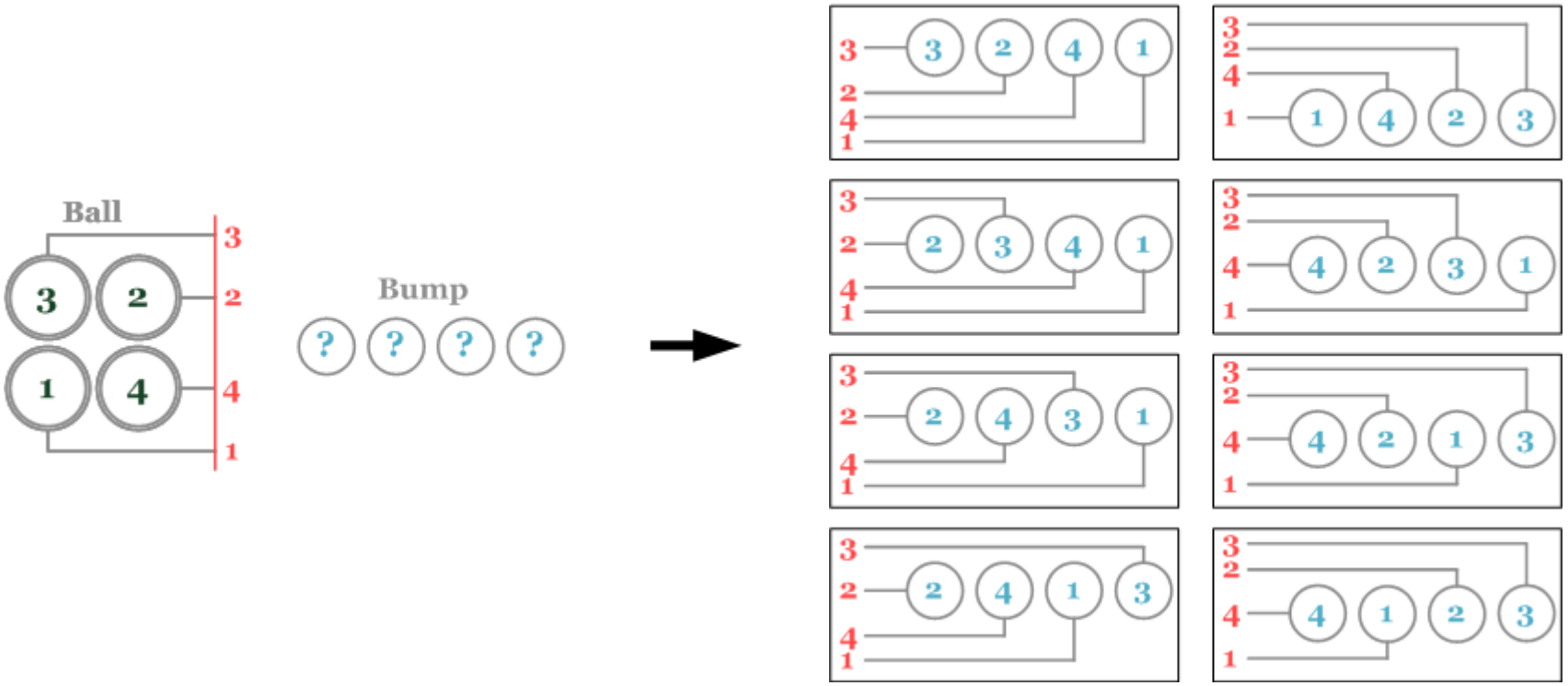
Global Bump Assignment

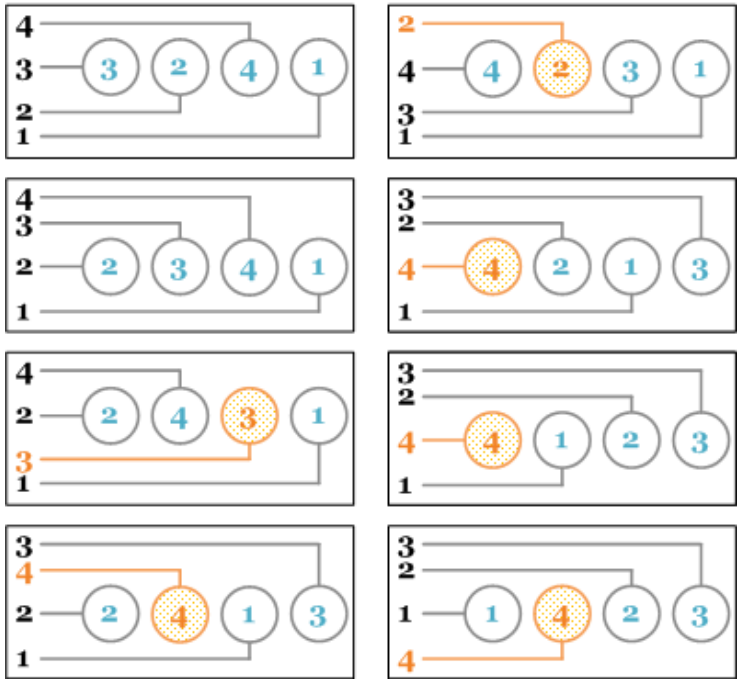
- Find bump assignment set according to the package escape routing result.



Detailed Bump Assignment

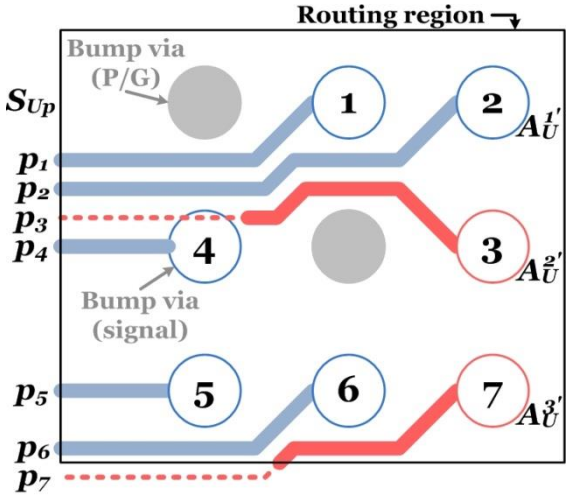
- Choosing a solution from bump assignment set to make the difference between bump pin order and I/O pin order is minimum.

I/O
4
3
2
1

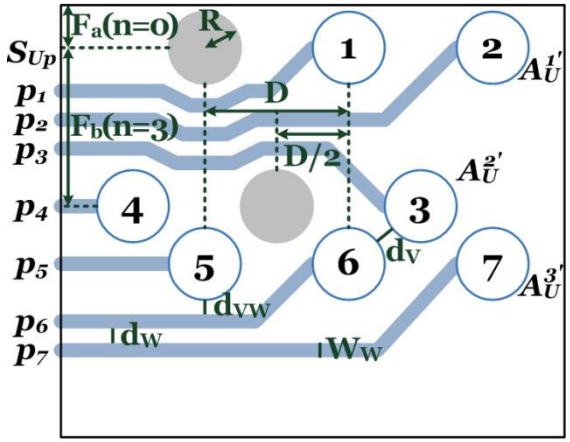


Verification of Practicality in Our Model

- Via staggering and compaction
  - Inspired by the **flexible via-staggering technique** [4].
  - Based on DRC rules.



(1) Grid via



(2) Stagger via

$$F_a(n) = \begin{cases} \frac{max(d_v, d_{vw})}{2} + R & , n = 0 \\ \frac{max(d_w, d_{vw})}{2} + nW_w + (n-1)d_w + d_{vw} + R & , n \geq 1 \end{cases}$$

$$F_b(n) = \begin{cases} \sqrt{(2R + d_v)^2 - (\frac{D}{2})^2} & , n = 0 \\ \sqrt{(2R + 2d_{vw} + nW_w + (n-1)d_w)^2 - (\frac{D}{2})^2} & , n \geq 1 \end{cases}$$

Notations:

- n: the number of wires.
- D: the distance between two adjacent bump vias.
- R: the radius of a bump via.
- d_v: the minimum spacing between two adjacent vias.
- d_w: the minimum spacing between two adjacent wires.
- d_{vw}: the minimum spacing between a via and a wire.
- W_w: the minimum wire width in bump area of package.

[4] S. Liu, G. Chen, T. T. Jing, L. He, T. Zhang, R. Dutta, and X. L. Hong, "Substrate topological routing for high-density packages," in *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 28, no. 2, pp. 207-216, Feb. 2009.*

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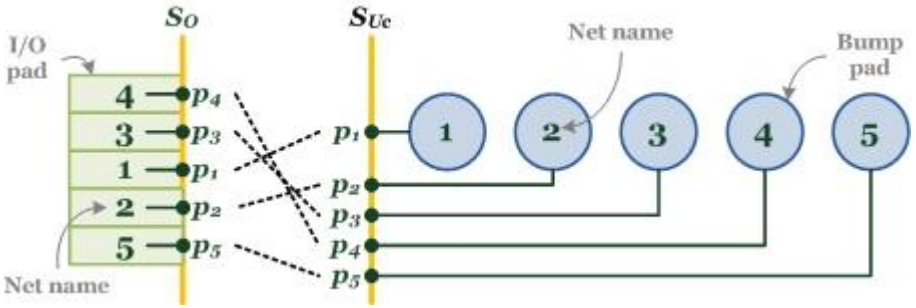
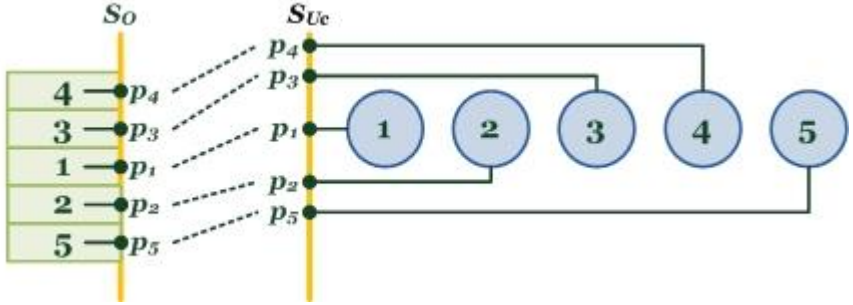
Projection Method

- Original projection method [3]
  - One direction
  - Cost more routing tracks



- Reformation
  - Two directions
  - Reduce # routing tracks



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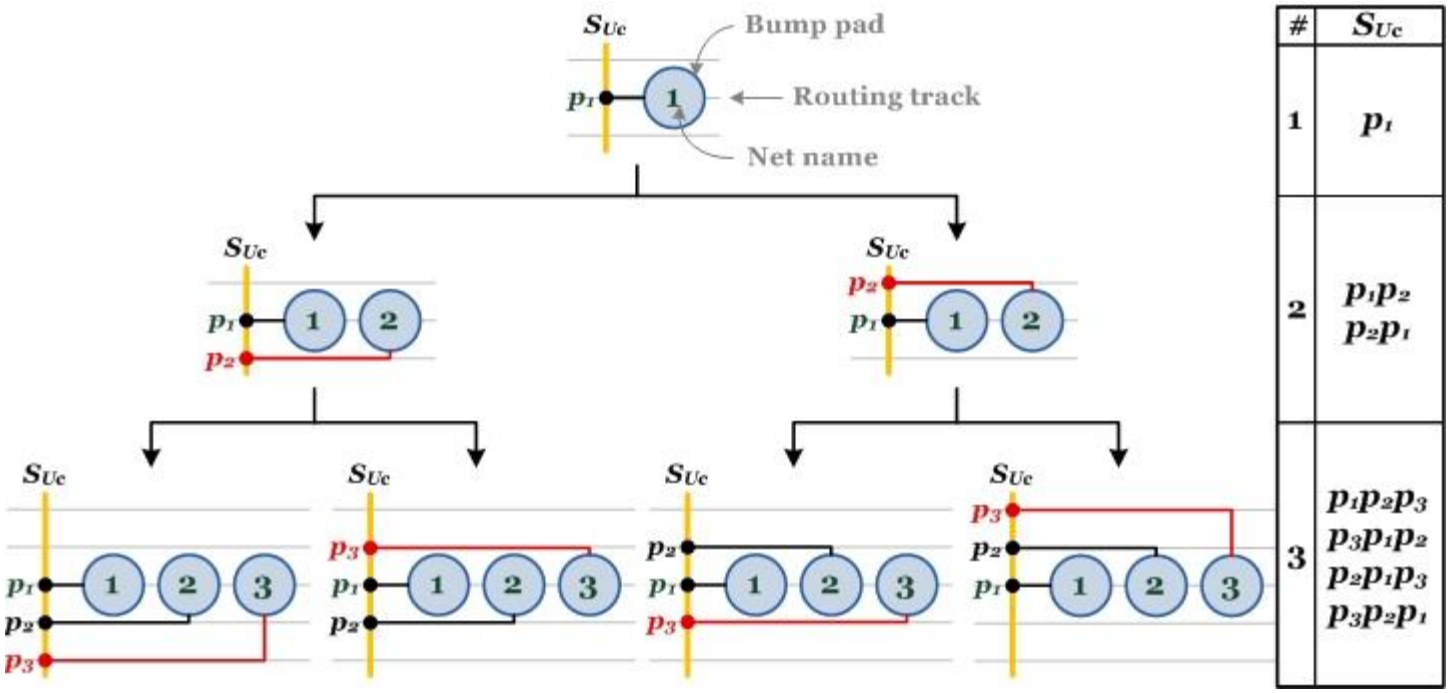
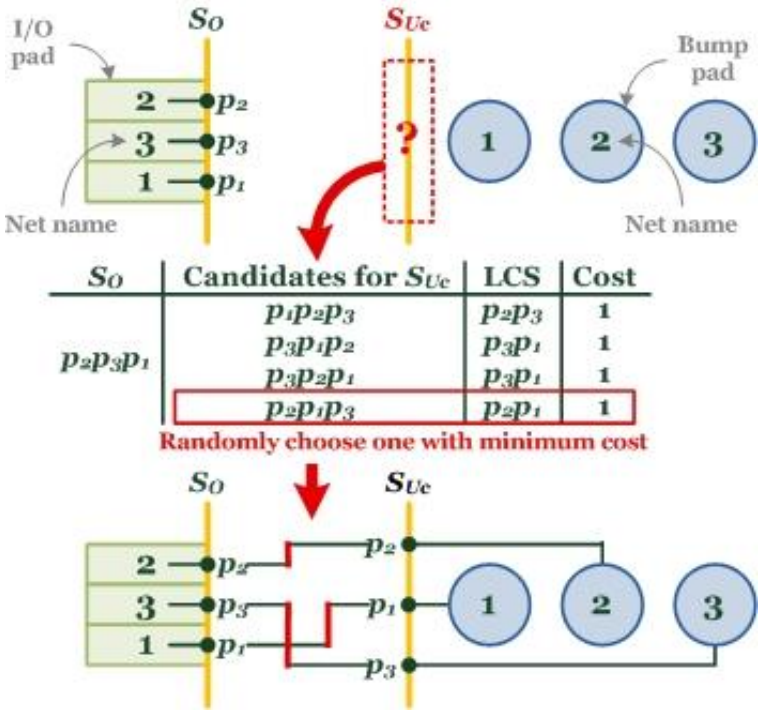
List of Bump Pin Track



RDL Routing

- Step1: consider I/O pads as a pin track S_O.
- Step2: perform projection method on bump matrix to build a virtual pin track S_{Uc}.
- Step3: channel routing on pseudo-single layer [3].



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Experimental Results

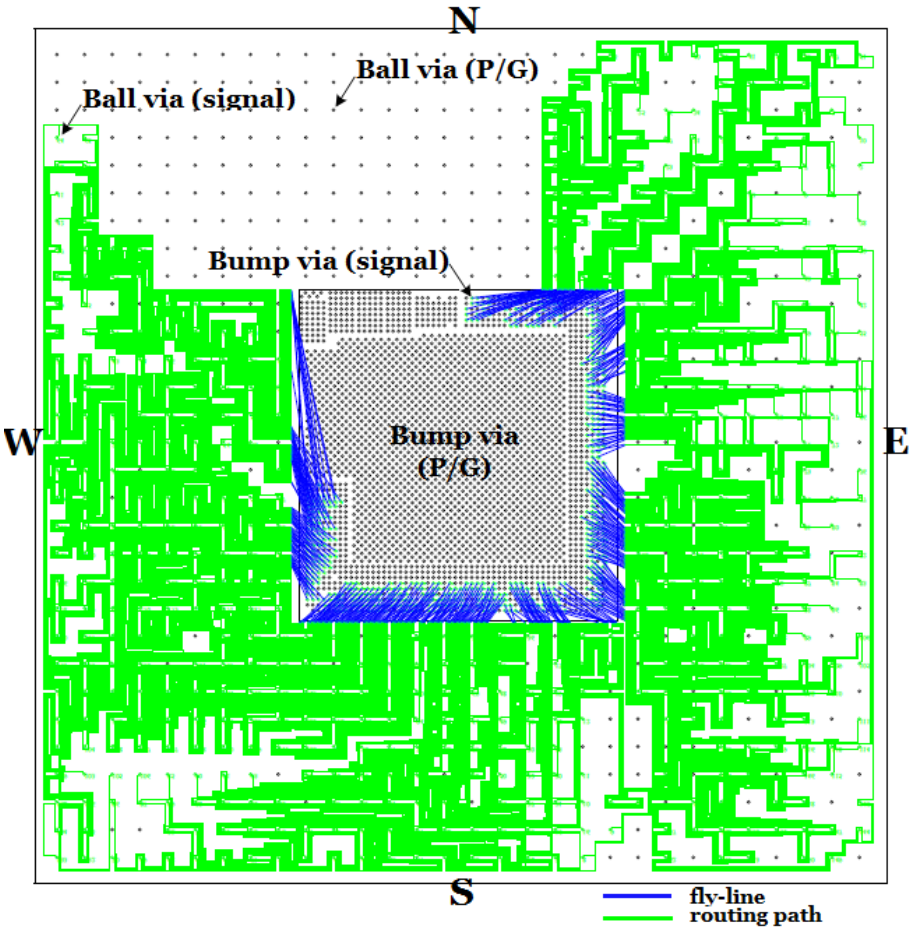
- Compared with traditional co-design flow, our work
  - costs less routing resource.
  - reduces design time.
  - saves manual effort.
    (automatically completes the whole process.)

Method	Substrate routing		
	# routed nets	Rout.	Time
Ours	507/507 in 2^{nd} layer	100%	909.52 (sec.)
Traditional	449/507 in 2^{nd} layer 58/507 in 3^{rd} layer	100%	a few months

Method	RDL routing		
	# routed nets	Rout.	Time
Ours	507/507 in pseudo single-layer	100%	$<$ 1 minute
Traditional	507/507 in two layers	100%	$>$ 2 weeks

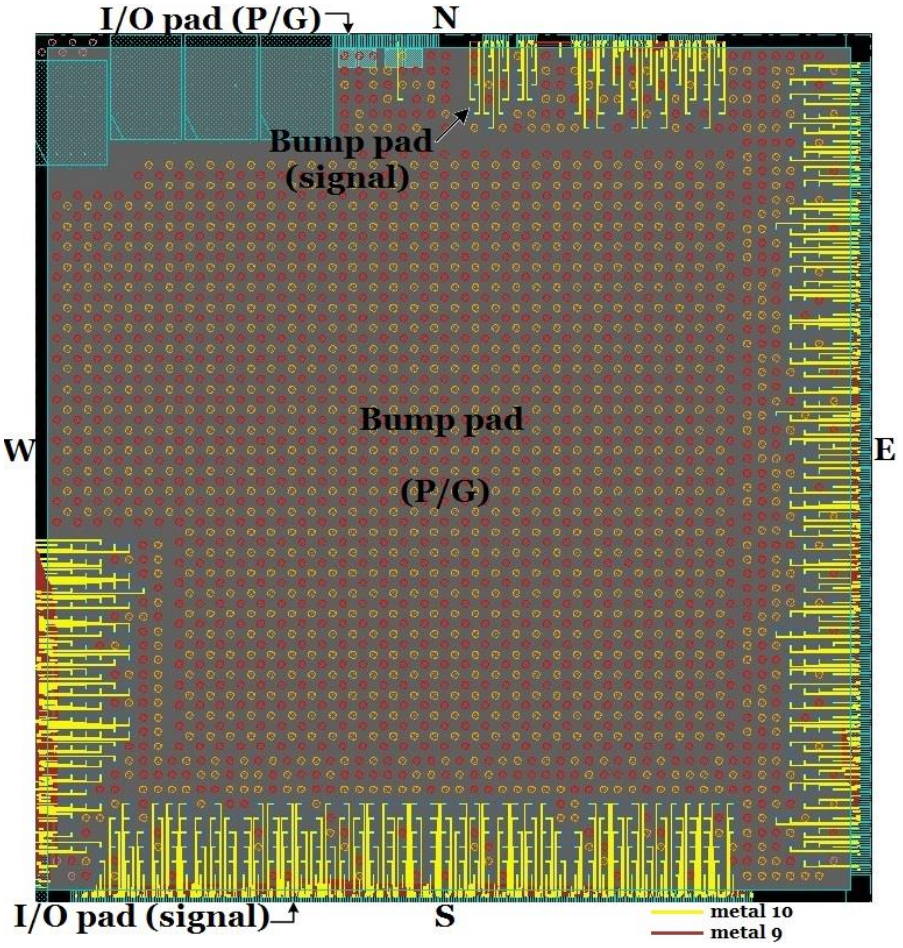
Package Routability

- Green path:
  the escape routing result.
- Blue fly-line:
  bump-ball assignment.



RDL Routability

- Based on our bump assignment, we can achieve 100% routability in RDL routing by [3].



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Conclusions

- We propose a straightforward chip-package co-design flow with routability-driven bump assignment based on:
  - Pseudo-single layer RDL routing [3].
  - B-Escape routing [5].
- Net grouping offers information interactions between chip and package to avoid the iterative revise of bump assignment in traditional design flow.
- Experimental results show that our work automatically completes the whole design process in a short time.

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