FUJITSU

A Volume Diagnosis Method for Identifying Systematic Faults in Lower-yield Wafer Occurring during Mass Production

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Outline

- Motivation
  - Lower-yield wafer
- Proposed method
  - Likelihood selection
- Experimental results
- Summary & future work

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Lower-yield Wafer Problem

- Even after yield is ramped up to a mature level, it may still vary as lower-yield (excursion) wafers occur.
  - In worse cases, we have to stop fabrication until the root causes are detected.
  - With increasing IC fabrication complexity, analyzing wafer and process histories becomes less effective.

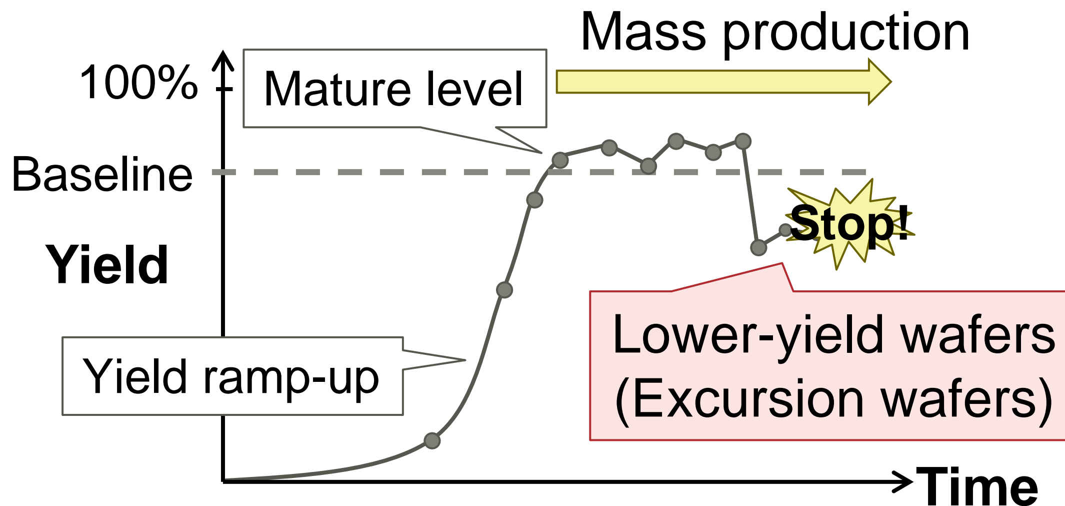
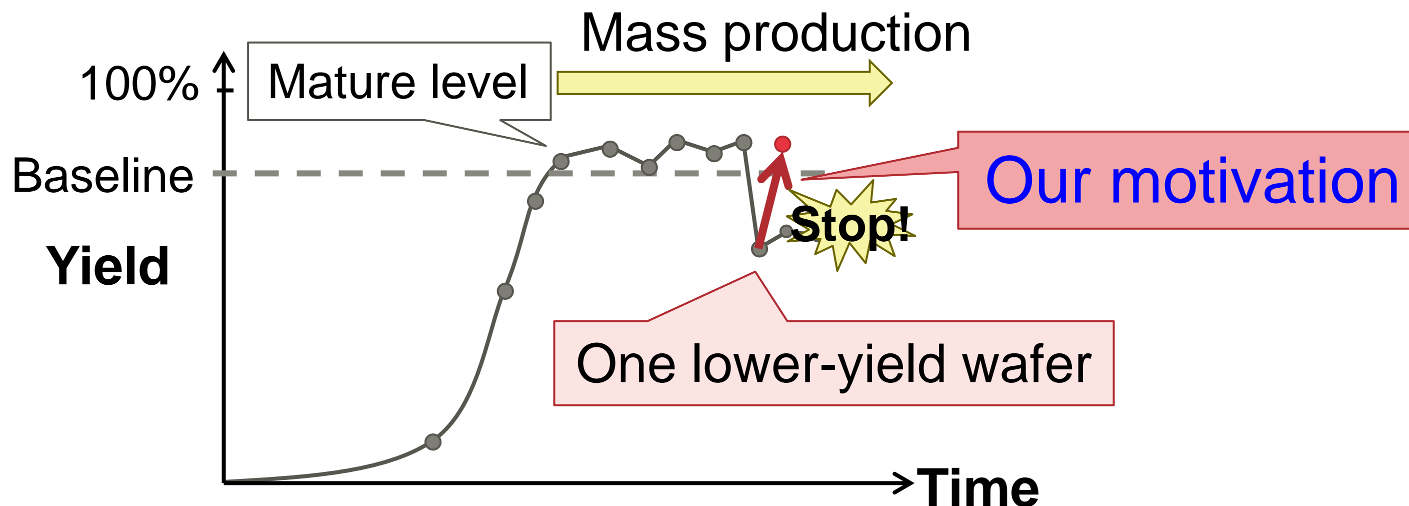


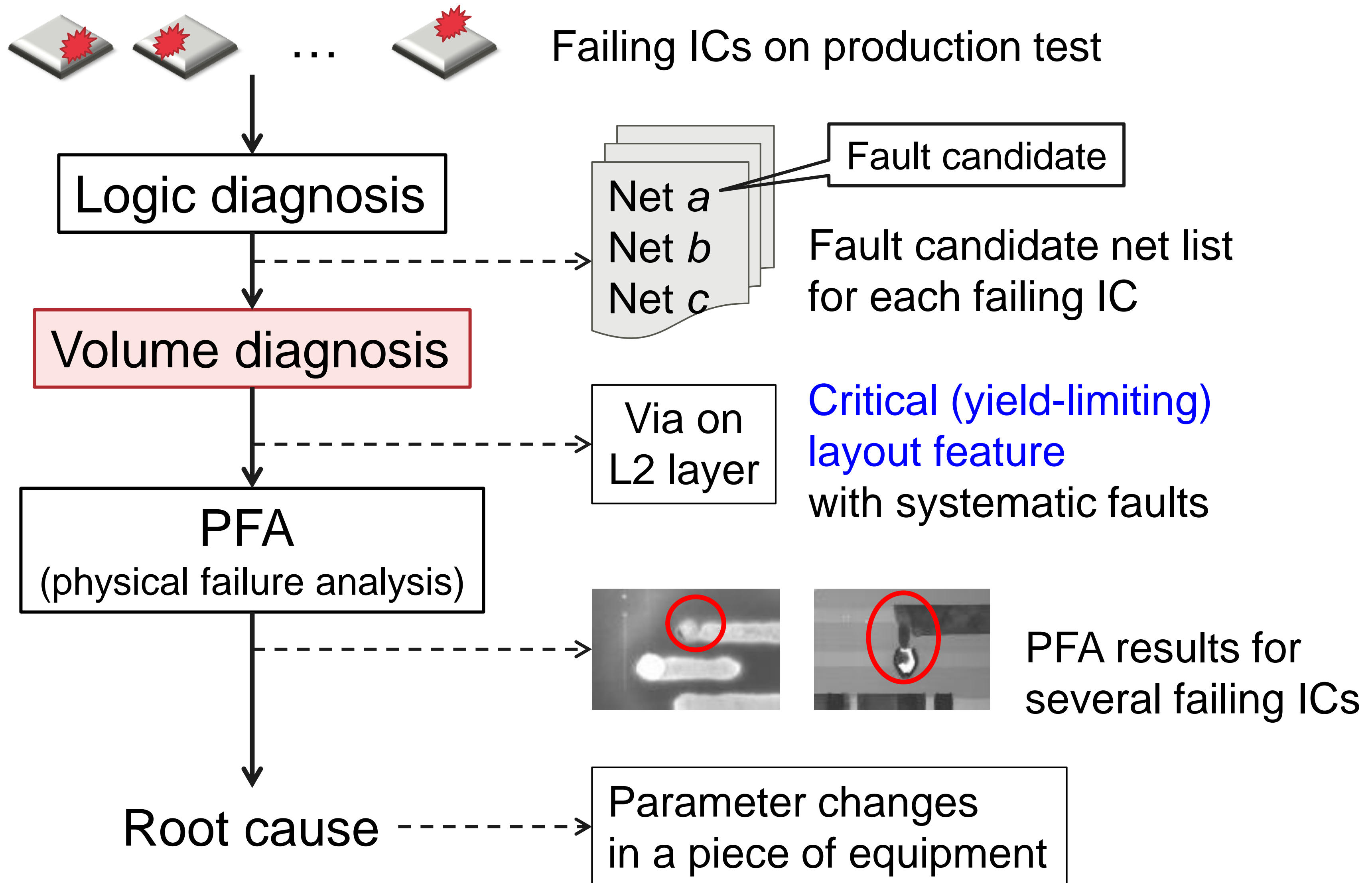
Fig. Image of yield transition of an IC product.

Motivation

- To identify the root cause using **one lower-yield wafer** for yield improvement.
  - In mature level, one lower-yield wafer sometimes occurs singly in a lot.
    - For example, due to failure of single-wafer processing equipment.



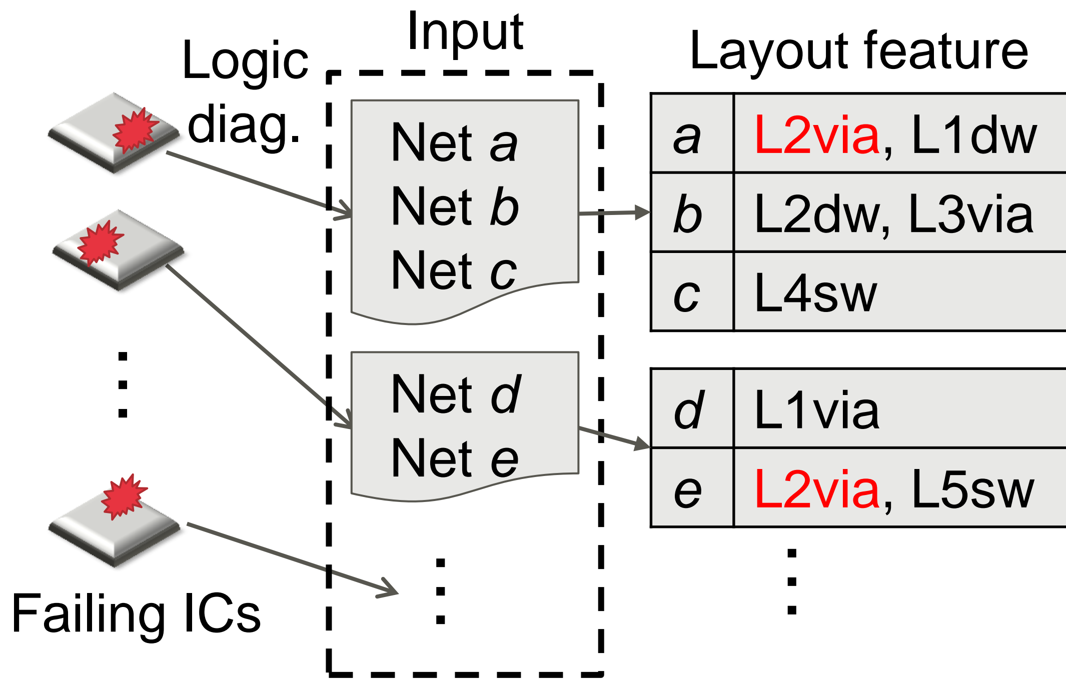
Process of Identifying Root Cause

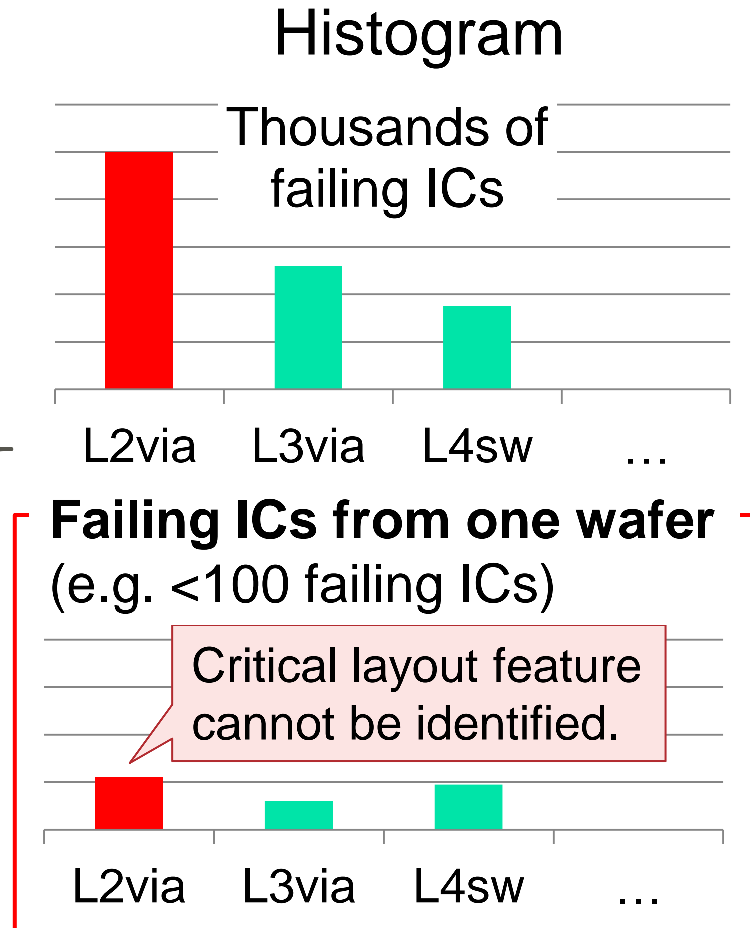


Why Conventional Volume Diagnosis* Doesn't Work for One Lower-yield Wafer?

- Not enough input data to analyze statistically.

*[C. Hora, *et al.*, ITC2002]
[H. Tang, *et al.*, ETS2007]





L$x$via: via on Lx layer
L$x$dw: dense-wiring pattern on Lx layer
L$x$sw: sparse-wiring pattern on Lx layer

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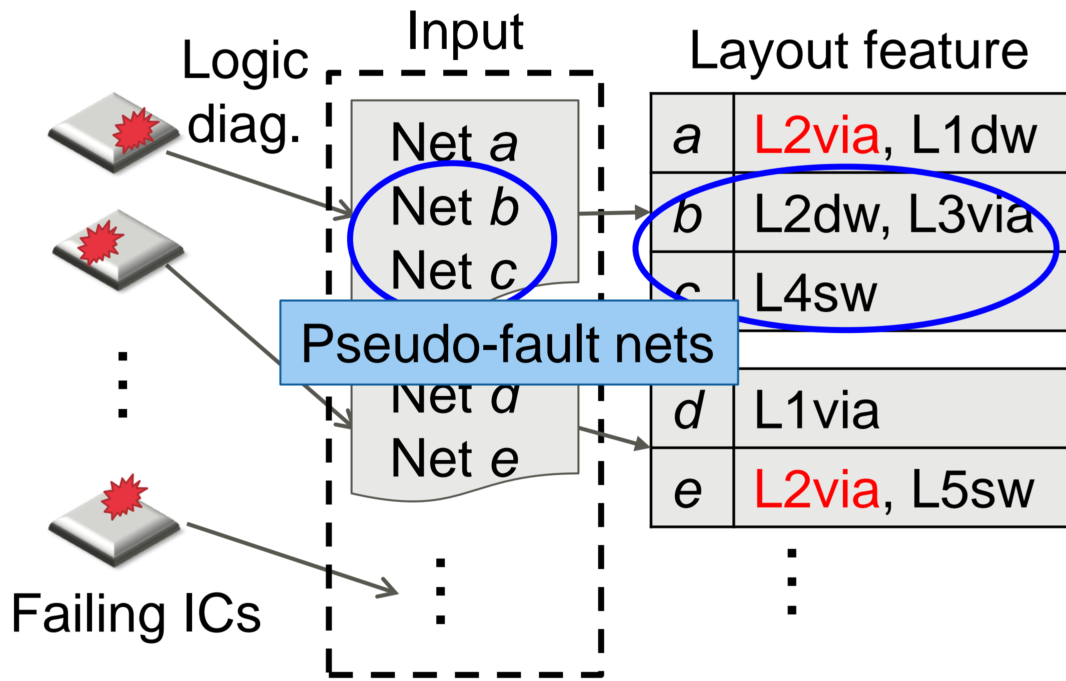

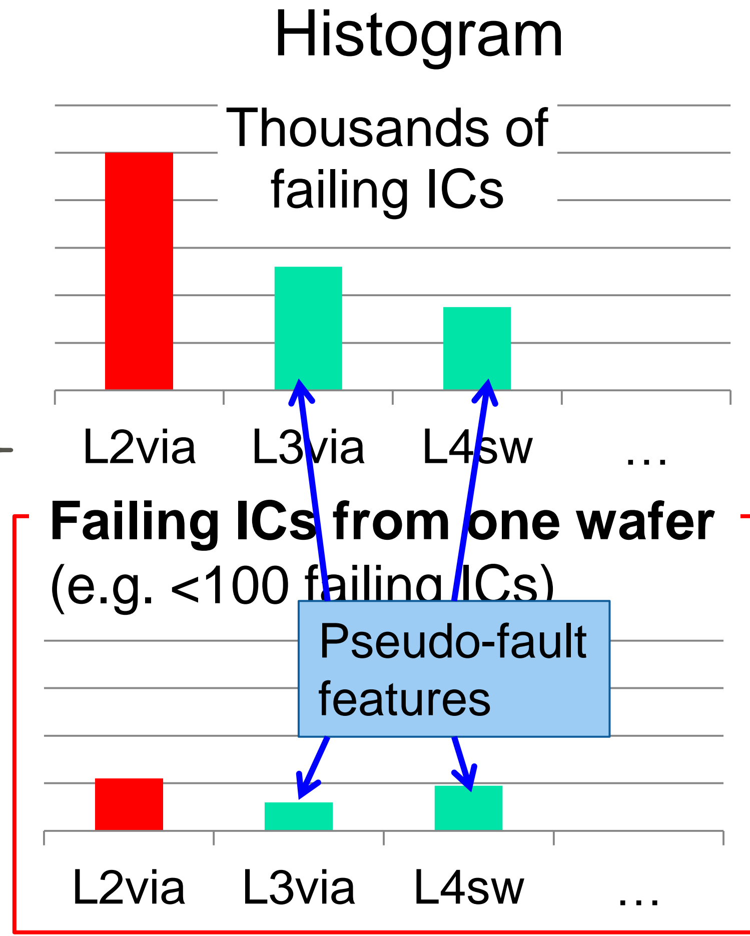

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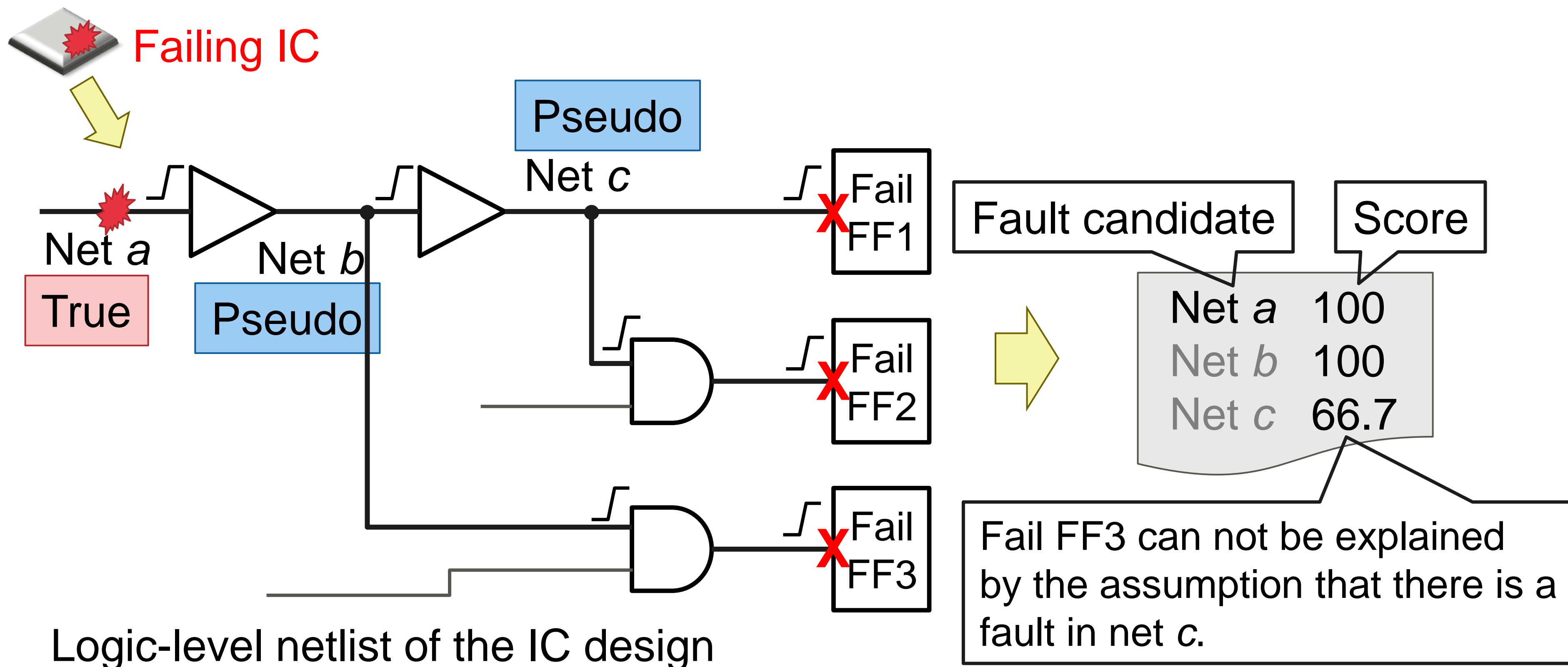
Why Pseudo-fault Nets Are Reported As Fault Candidate Nets?

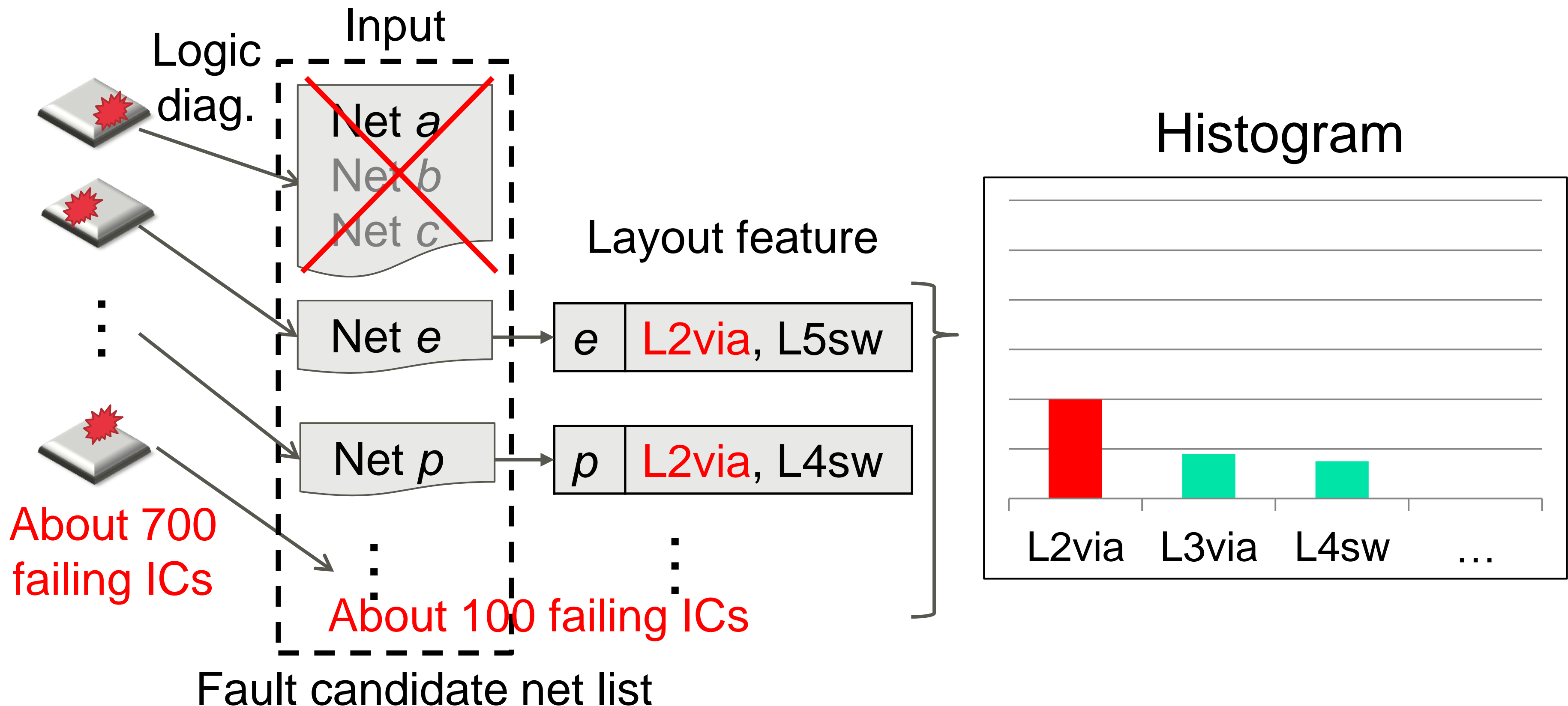
- Logic diagnosis cannot identify true fault nets definitely due to logic equivalency and lack of layout information.
  - But each fault candidate net can be ranked (e.g. score).



Previous Work

How to Avoid the Effect of Pseudo-fault Nets?

- W. C. Tam, *et al*., ITC 2010
  - They used the failing ICs in which there is only one fault candidate net in the experiment.



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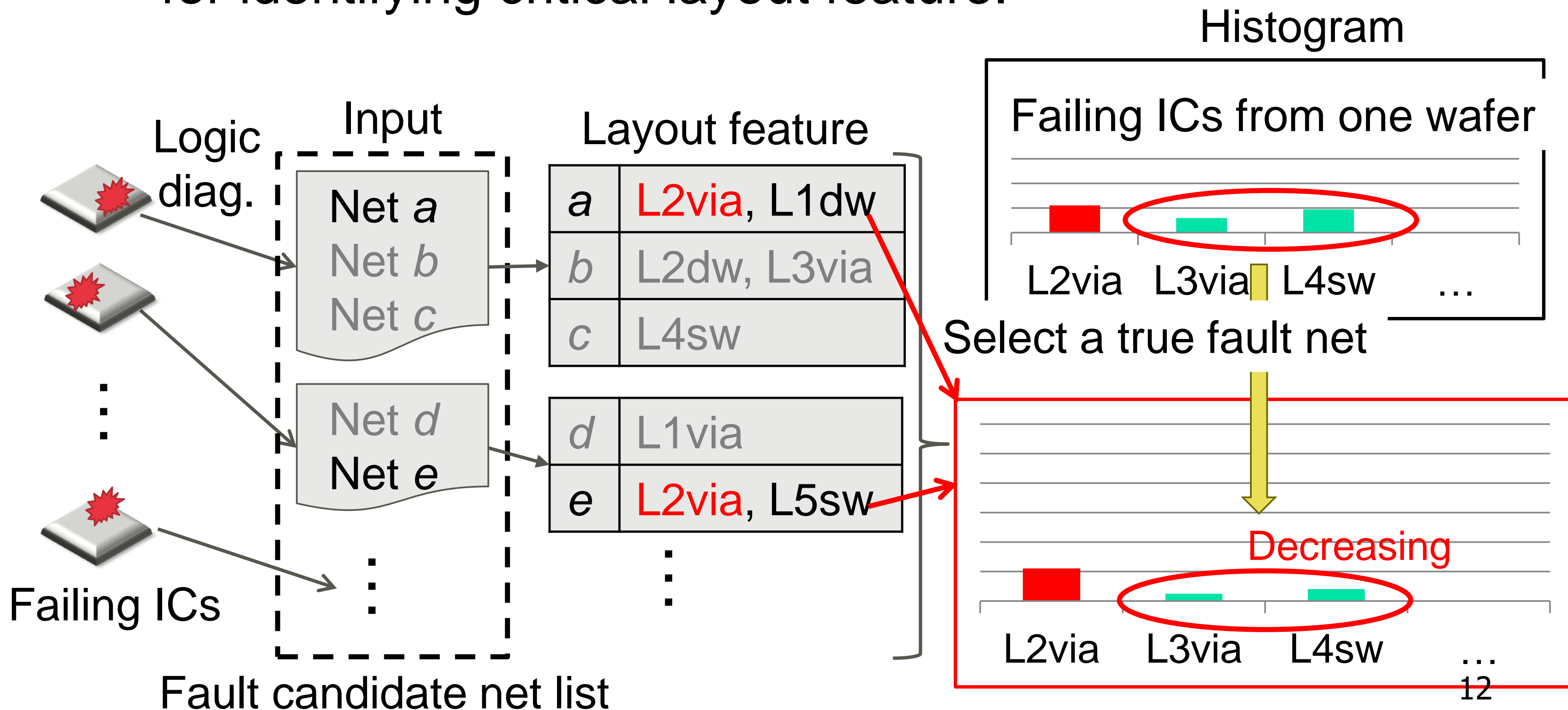
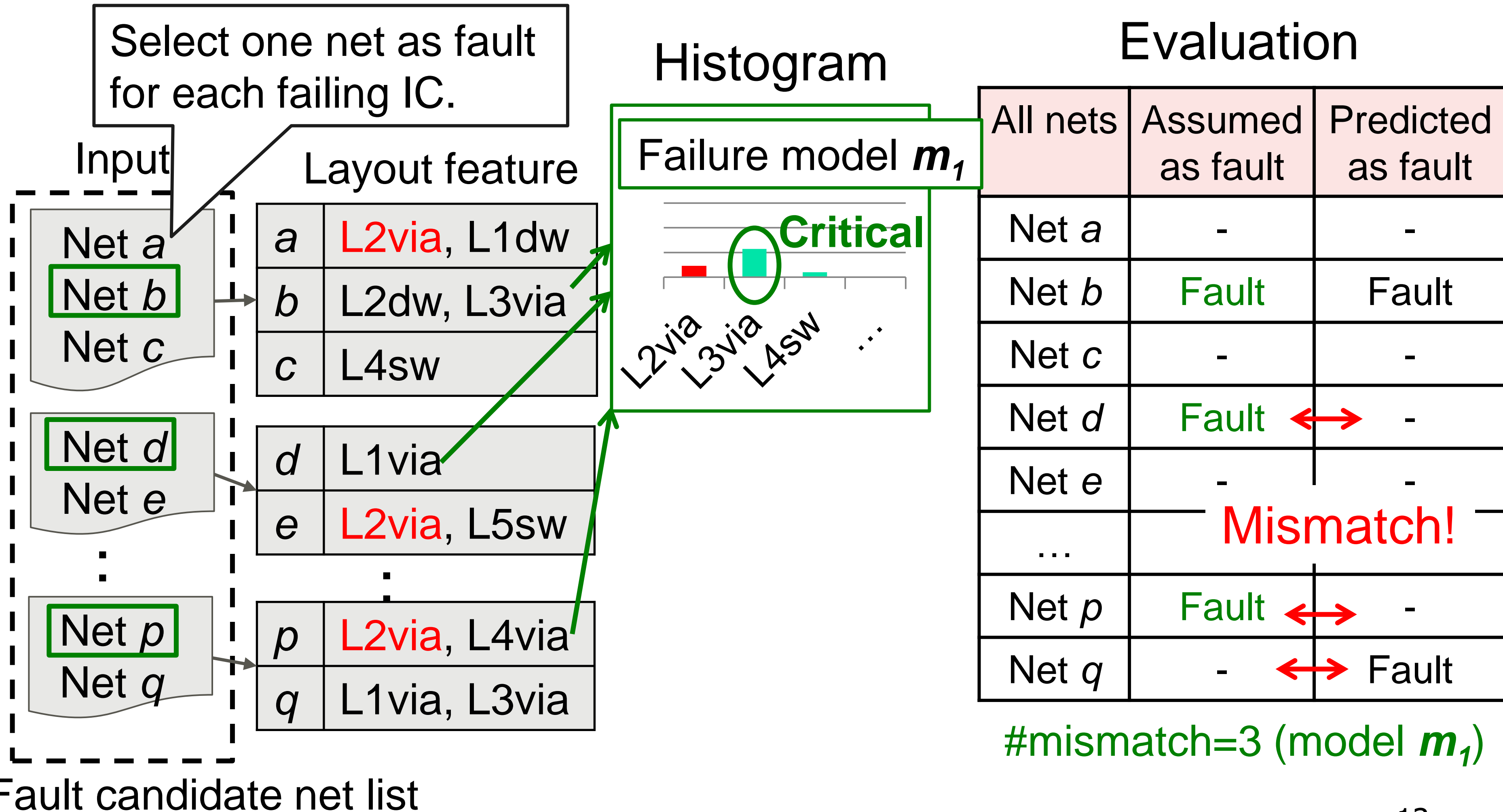
Our Main Contribution

- We proposed a new volume diagnosis method:
  - For each failing IC, a true fault net can be selected by a key technique (we call it **"likelihood selection"**).
  - One lower-yield wafer (e.g. <100 failing ICs) is enough for identifying critical layout feature.



Key Idea

- To find fault candidate nets of which failure model can predict whether each net is assumed as fault or not correctly.



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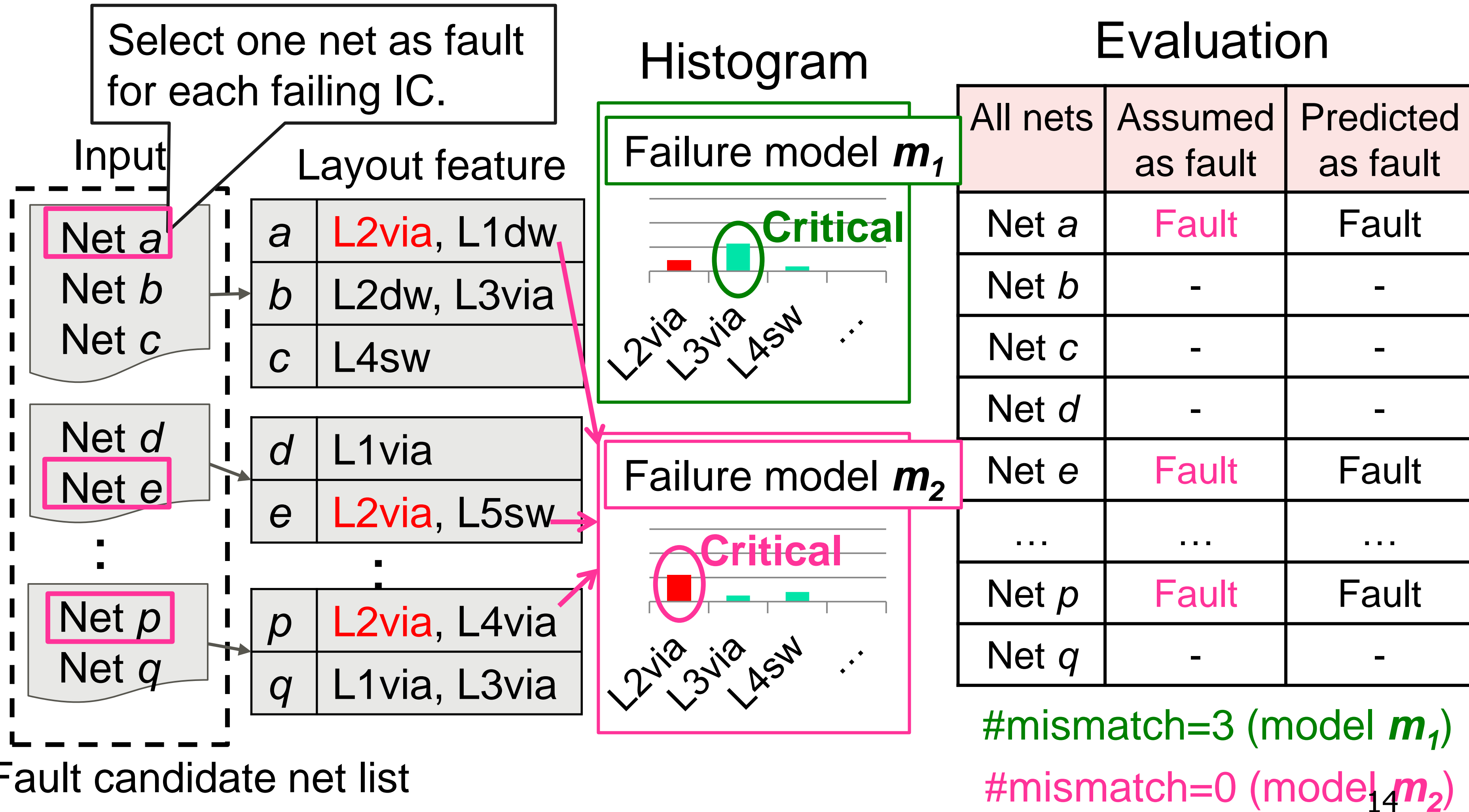
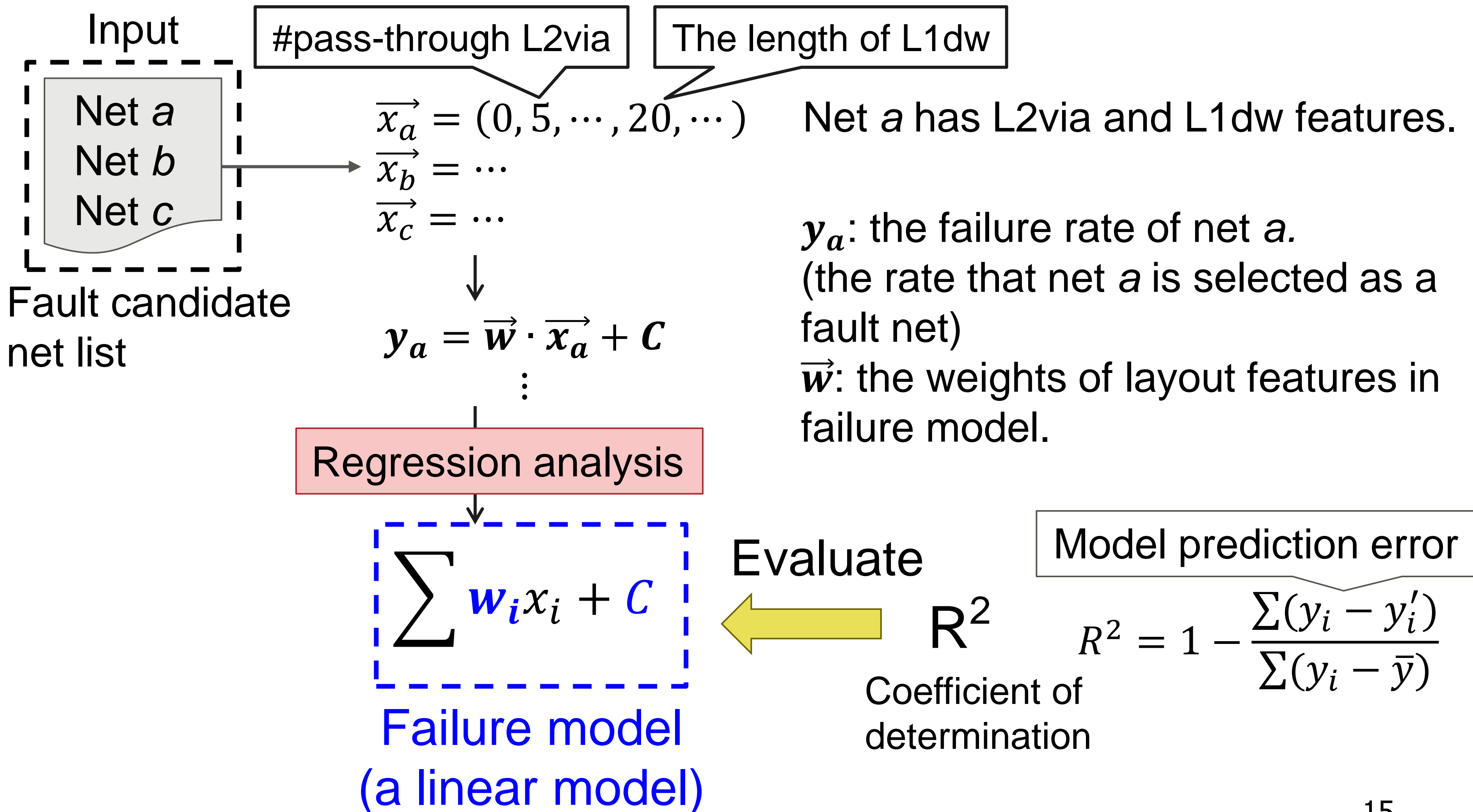


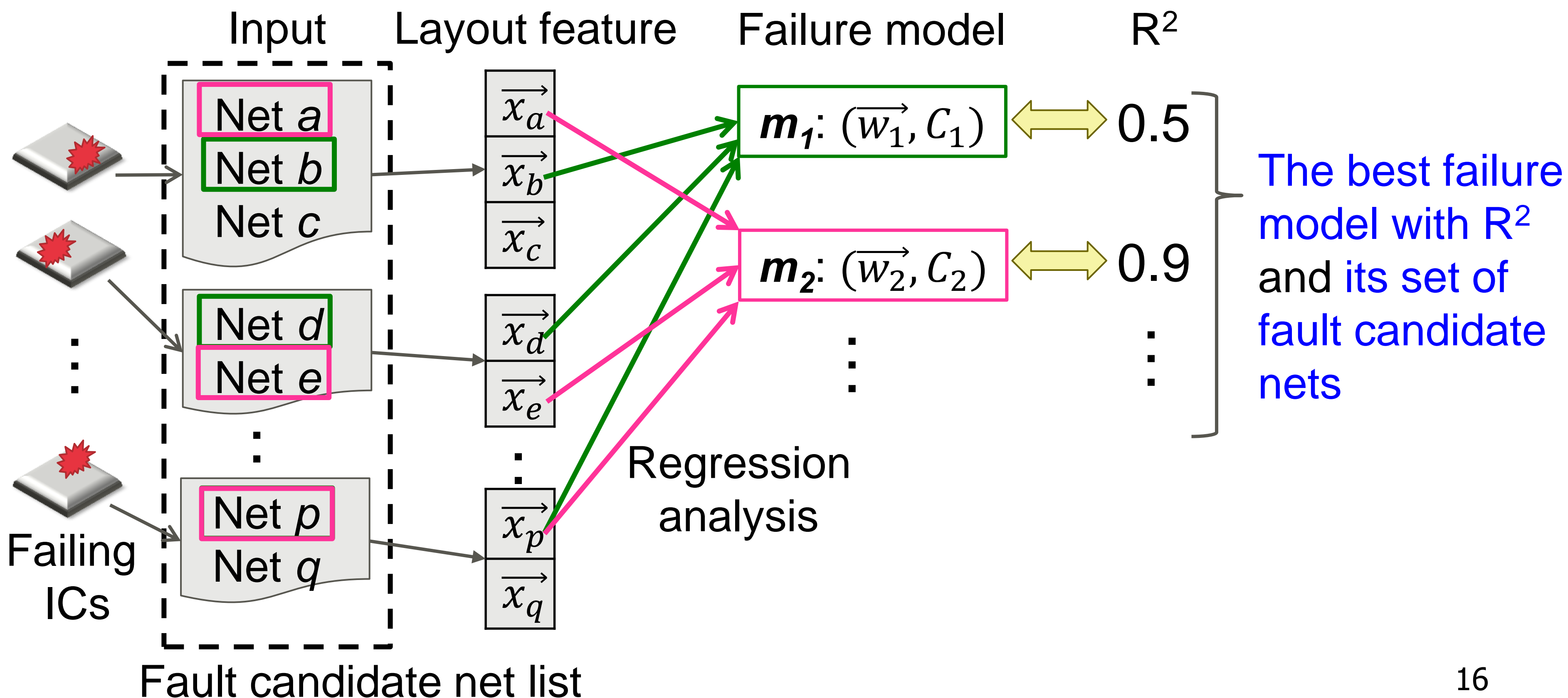
Details of Failure Model

- Failure model is a linear model.



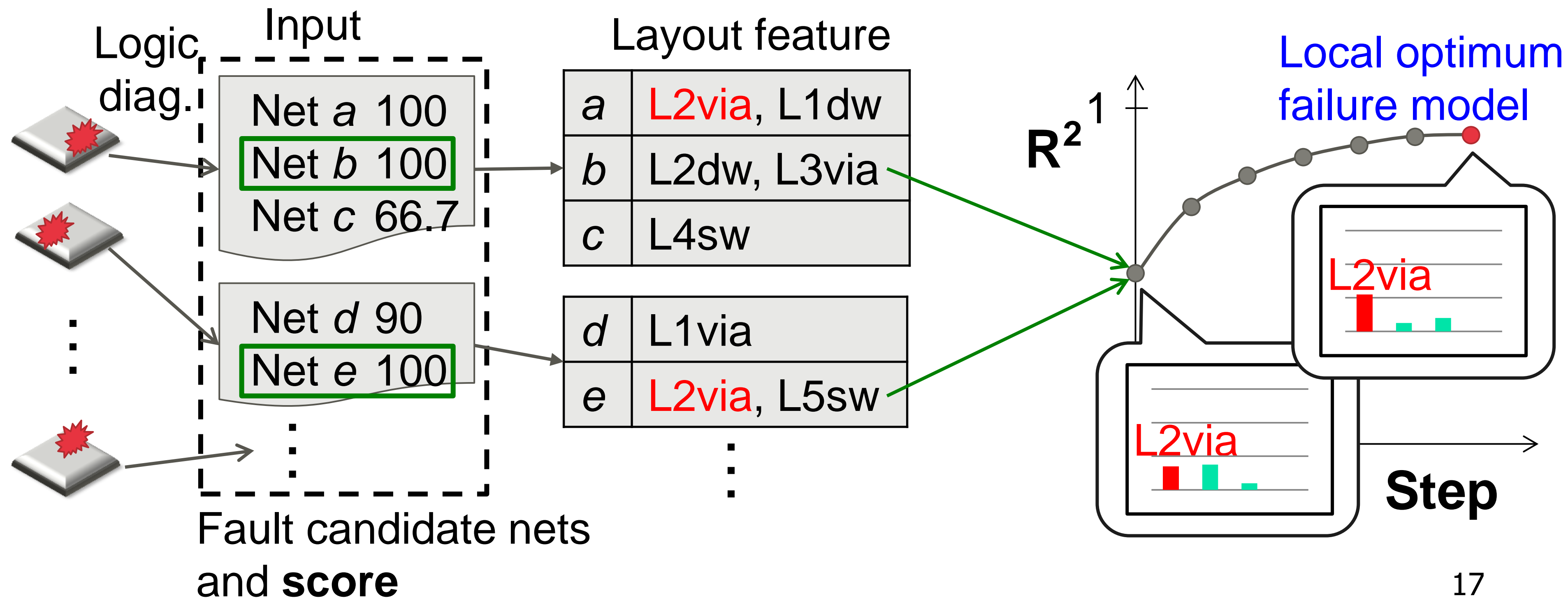
A Combinatorial Optimization Problem

- To find the set of fault candidate nets of which failure model's R^2 comes close to 1.
  - Combinatorial optimization is used to implement the key idea.

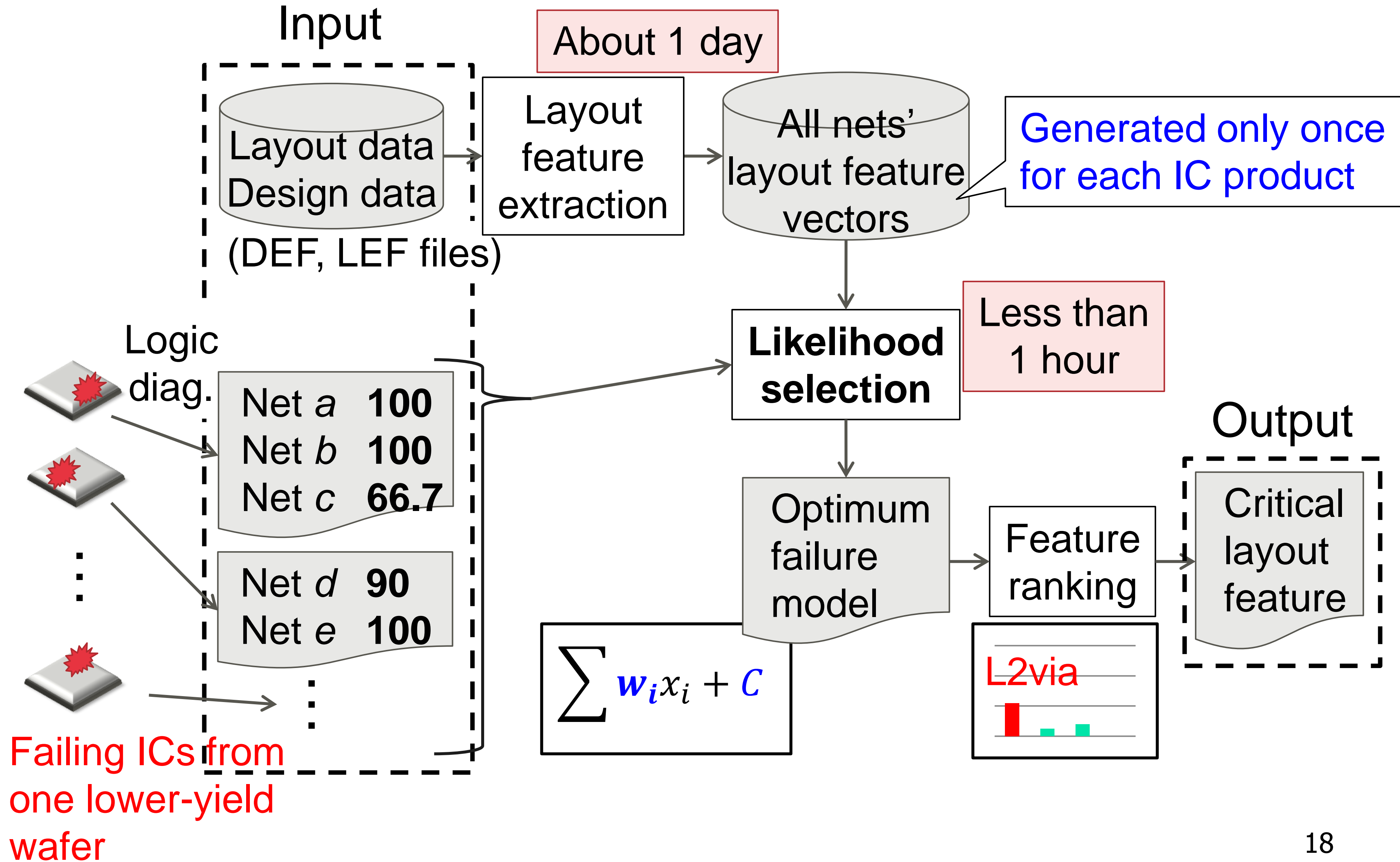


Likelihood Selection: A Combinatorial Optimization Process

- Hill climbing can obtain the failure model which identifies the critical layout feature correctly.
  - Because initial fault nets which are pretty close to true fault nets are extracted using indices (e.g. score) with logic diag.
  - We call this comb. opt. process **“likelihood selection.”**



Overall Flow



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Experiments & Results

- Practical IC product B
  - Process: 65nm CMOS
  - Gates: about 10 million
  - Layers: L1 – L6
- Dataset

Identified using equipment history

Dataset	#Failing ICs	Damaged layer
B-lot1-wf2	60	L4 layer
B-lot2-wf2	73	L2 layer
…	…	…

21 datasets are collected.

- Each dataset consists of failing ICs which are successfully diagnosed by in-house logic diag. tool in one lower-yield wafer.

- Capability of the proposed method
  - For 19 datasets, the proposed method could identify the damaged layer correctly.

Experiments & Results

- Practical IC product A
  - Process: 28nm CMOS
  - Gates: about 60 million
  - Layers: L1 – L9
- Dataset

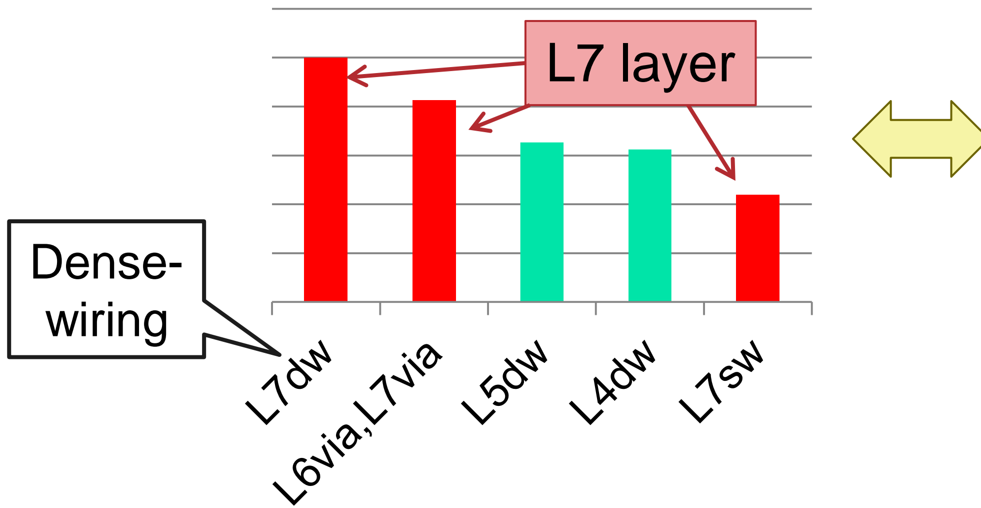
Identified by PFA

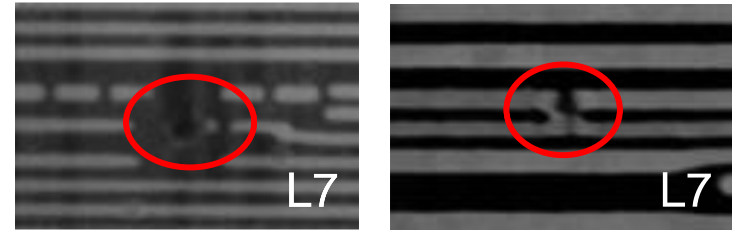
Dataset	#Failing ICs	Critical layout feature
I (A-lot1-wf1)	35	L7dw
II (new)	29	L7via

- Capability of the proposed method
  - For both datasets, the proposed method could identify its own critical layout feature correctly.

Details of Experimental Results with Product A

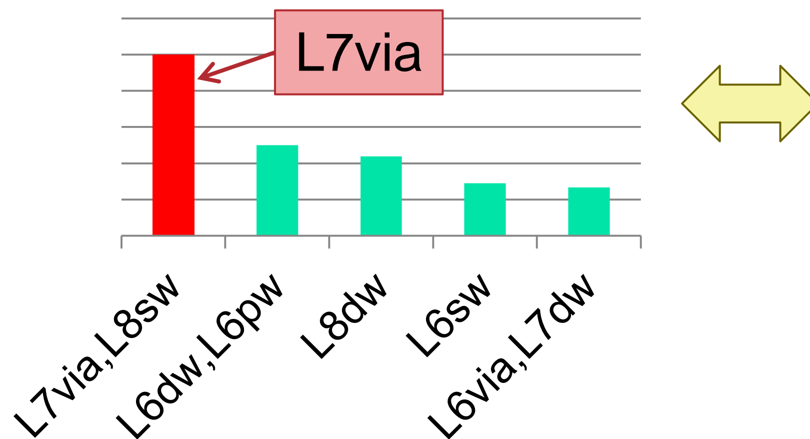
I. 35 failing ICs with Lot-1

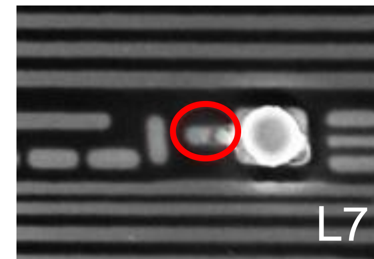




L7 layer is damaged.

II. 29 failing ICs with Lot-2

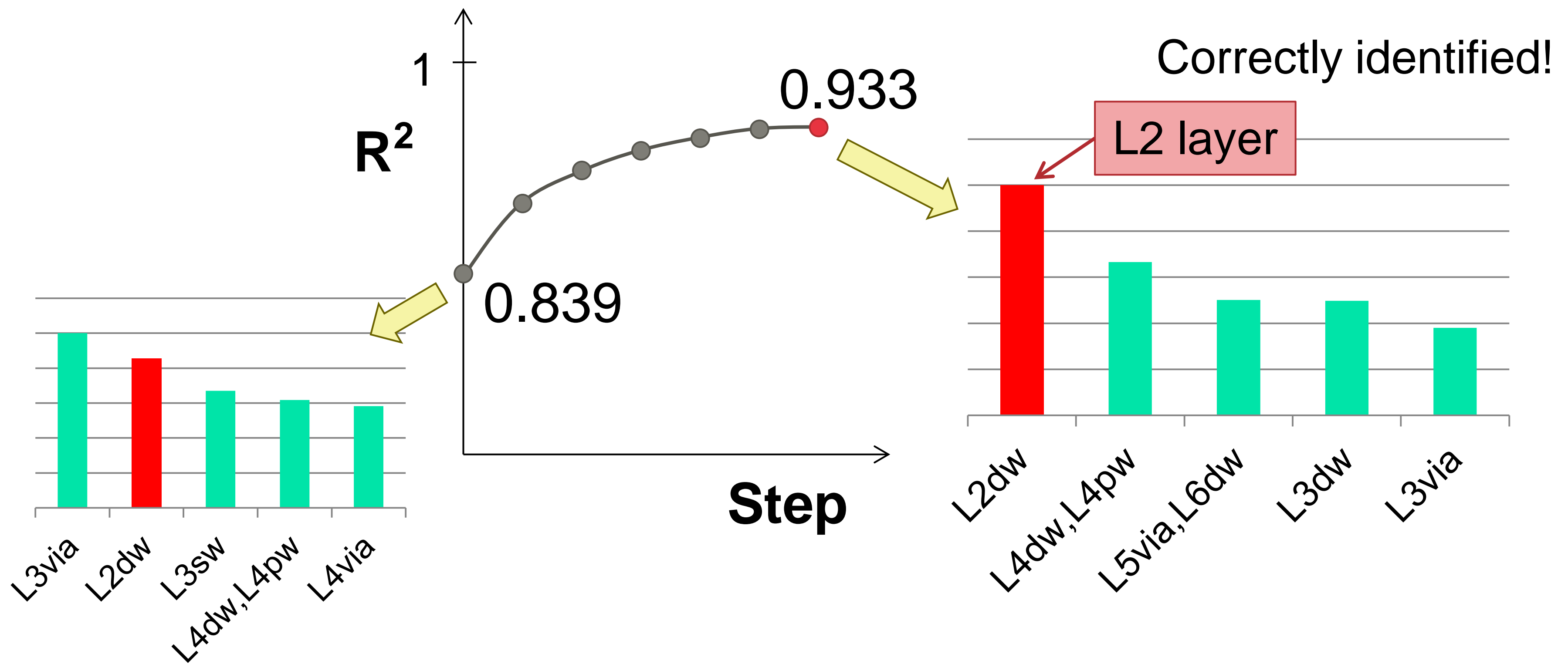




A wire connected to a via is opened on L7 layer.

Effectiveness of Likelihood Selection

- A typical example (a dataset of product B) which shows the effectiveness of likelihood selection.
  - In likelihood selection, the initial fault net is replaced in 28 of 66 failing ICs.



Summary and Future Work

- We presented a volume diagnosis method for identifying critical layout feature with systematic faults in one lower-yield wafer.
  - Likelihood selection:
    - A kind of combinatorial optimization process.
    - A technique which can select true fault nets from among fault candidate nets including pseudo-fault nets.
  - Net grouping, ε-SVR (Details are described in our paper)

- Future work
  - To rank fault location candidates in failing ICs using the fault nets and the critical layout feature obtained by the proposed method.
  - To evaluate existing DFM rules based on the dominant root causes with lower-yield wafers.

Thank you!