Fast Vectorless Power Grid Verification using Maximum Voltage Drop Location Estimation

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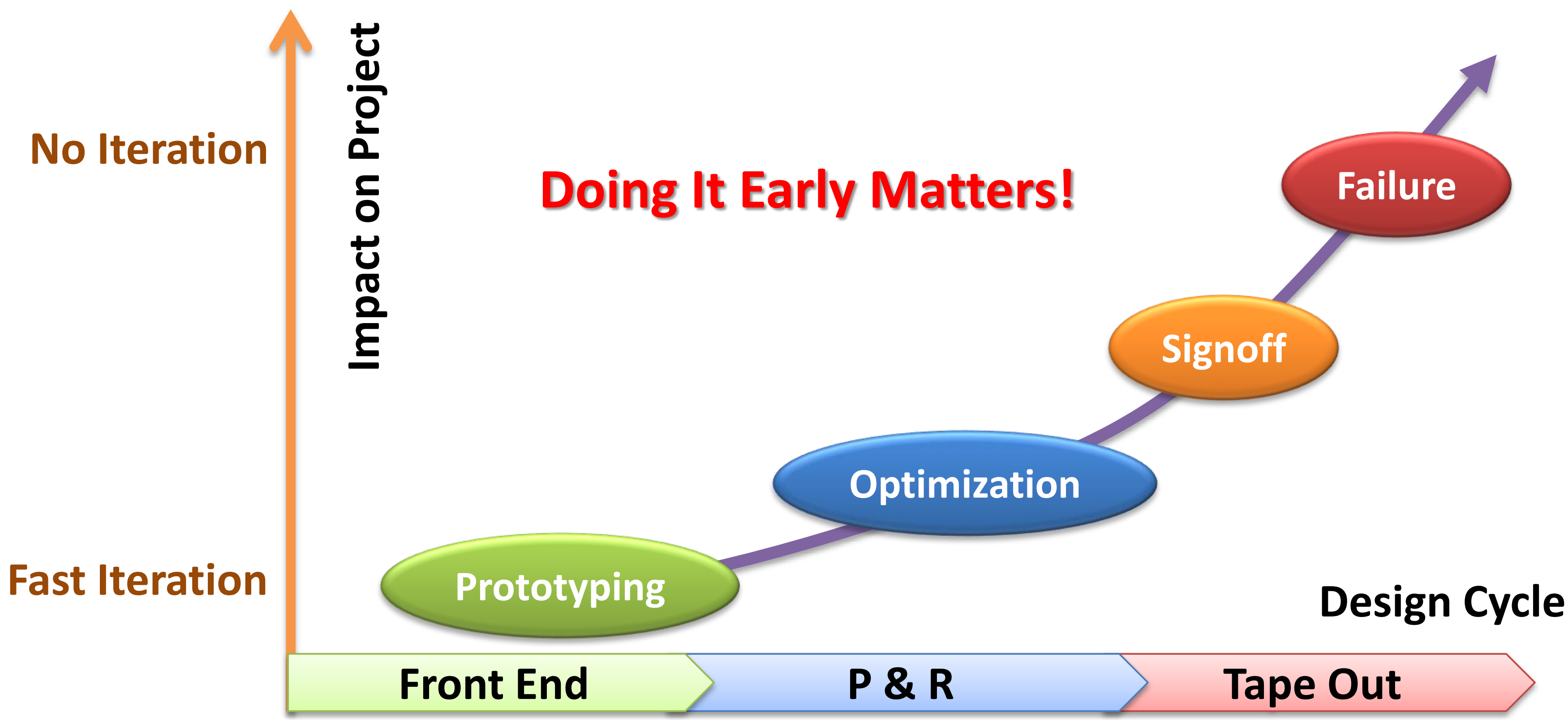
Outline

- Introduction to Vectorless Verification
- Proposed Approach
  - Worst case location estimation
  - Group-wise verification
- Experimental Results & Summary

Power Grid Verification

- Design Challenge
  - Billion-transistors VLSI design
  - Early stage power grid safety check

Simulation is not enough!



Simulation vs. Vectorless

$$G\,\mathbf{v} = \mathbf{i}$$

$$\mathbf{v} = G^{-1}\,\mathbf{i}$$

- Simulation approach
  - Input current patterns are required
  - Solving liner equations to obtain voltage distribution
- Vectorless approach
  - Lack of knowledge of circuit details in early design stage
  - Current constraints are required according to circuit behavior with uncertainty working mode
  - Problem: Verify the grid voltages under all possible current waveforms that satisfy the current constraints
  - Provide a specification or budget based framework for the power grid prototyping

Problem Definition

- **Current Constraints**
  - **Local constraints: upper bound on individual current sources** $\mathbf{0} \le \mathbf{i} \le \boldsymbol{I_L}$
  - **Global constraints: bounds on sums of groups of currents**

$$\boldsymbol{U}\mathbf{i} \le \boldsymbol{I_G}$$

- **Obtain the worst case of the grid voltage**
  - **To estimate the worst-case voltage fluctuations by solving optimization problems**

$$\boldsymbol{v} = \boldsymbol{G}^{-1}\boldsymbol{i}$$

  - **Maximize voltage drops subject to current constraints**

maximize $\boldsymbol{v}$ **s.t.**

$\boldsymbol{Gv} = \boldsymbol{i}$, $\boldsymbol{Ui} \le \boldsymbol{I_G}$ **and** $\mathbf{0} \le \boldsymbol{i} \le \boldsymbol{I_L}$

Vectorless Power Grid Verification

- **The problem can be divided into two major tasks**
  - Let $\boldsymbol{c_i} \triangleq \boldsymbol{G^{-1} e_i}$

    where $\boldsymbol{e}_i$ is the $\boldsymbol{n} \times \boldsymbol{1}$ vector of all zeros except the i-*th* component being 1, it is to obtain the i-*th* column of $\boldsymbol{G}^{-1}$ by solving $\boldsymbol{Gx} = \boldsymbol{e}_i$
  - The voltage of the i-*th* node can be obtained by

    $$\boldsymbol{v_i = c_i^T i}$$

  - Task 1: compute $\boldsymbol{c_i}$ by solving $\boldsymbol{Gx = e_i}$
  - Task 2: maximize $\boldsymbol{v_i = c_i^T i}$ s.t.

    $$\boldsymbol{Ui \le I_G} \text{ and } \boldsymbol{0 \le i \le I_L}$$

Task 1: More than 80% computation cost!

- **Total cost to verify a power grid with $\boldsymbol{N}$ nodes**
  - Solving linear equations with $\boldsymbol{N}$ unknowns for $\boldsymbol{N}$ times
  - Solving LP problems for $\boldsymbol{N}$ times

Motivation

- **Prototype Vectorless Power Grid Verification**
  - **Element-wise verification**

1. For $k = 1$ to n
2. Maximize $v_k = (G^{-1}e_k)^T \mathbf{i}$ s.t. $\mathbf{i} \in \mathcal{L}$
3. Let $v_{max_k} = max\ v_k$
4. End For
5. Find $v_{max} = max\ \{v_{max_1}, v_{max_2}, \cdots, v_{max_n}\}$

- **Maximum voltage drop location estimation**
  - **Group-wise verification**

1. Maximize $f(\mathbf{i}) = f(v_{P_{j1}}, v_{P_{j2}}, \cdots, v_{P_{jk}})$ s.t. $\mathbf{i} \in \tilde{\mathcal{L}}$
2. Let $\mathbf{i}_j^* = argmax_{\mathbf{i} \in \tilde{\mathcal{L}}}\ f(\mathbf{i})$
3. Find

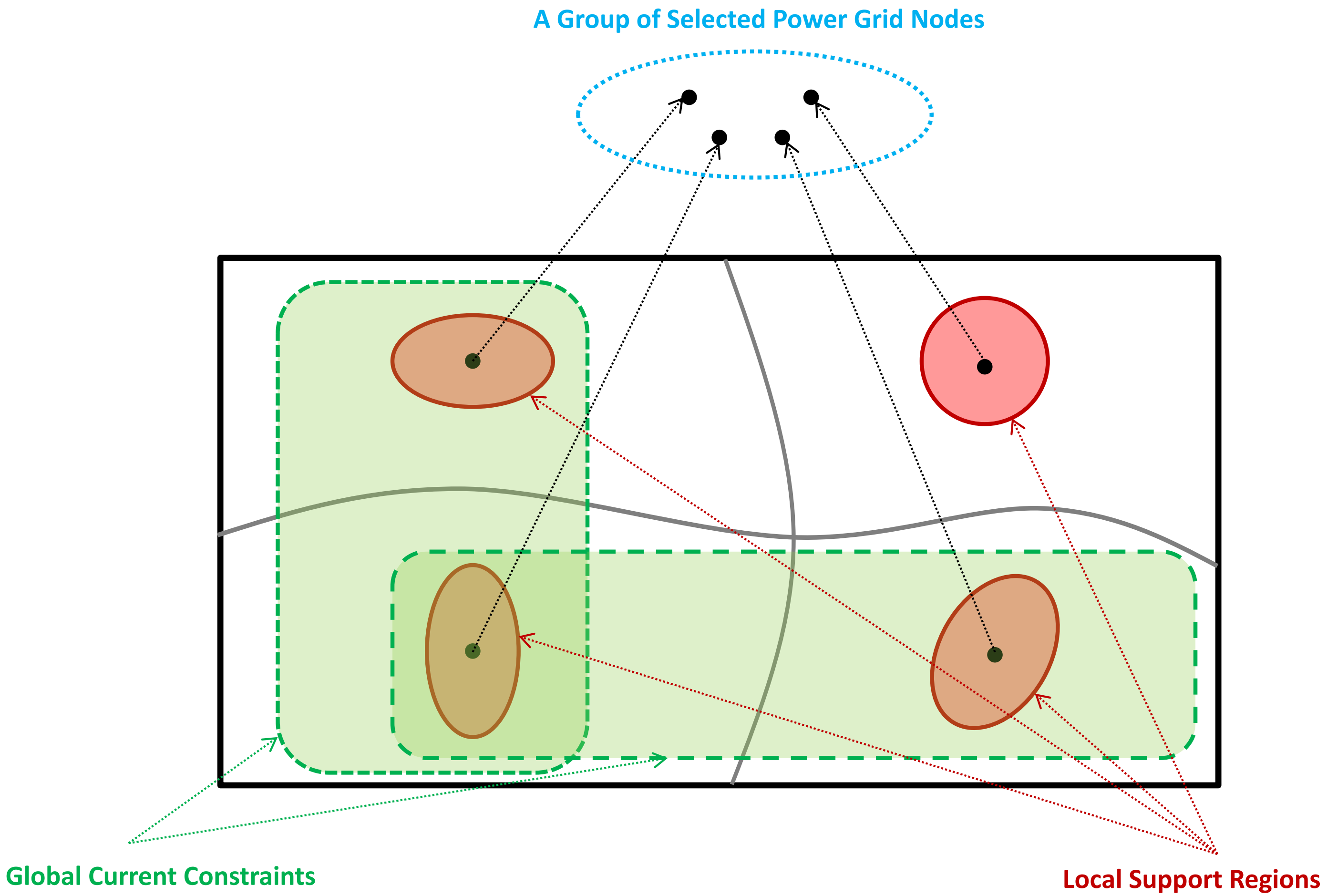
$$v_{P_{j^*}}(\mathbf{i}_j^*) = max\ \left\{v_{P_{j1}}(\mathbf{i}_j^*), v_{P_{j2}}(\mathbf{i}_j^*), \cdots, v_{P_{jk}}(\mathbf{i}_j^*)\right\}$$

Framework

- **Node grouping based on circuit partitioning**
  - **Divide the set of power grid nodes into k subsets**
  - **Node grouping from each subset**
- **Verification for each group nodes**
  - **Maximization for the objective of each group**
  - **Obtain the current solution $\mathbf{i}_j^* = argmax_{\mathbf{i}\in\tilde{\mathcal{L}}}\, f(\mathbf{i})$**
  - **Find the worst case node of this group by substituting $\mathbf{i}_j^*$ to each grid node**
  - **Perform accurate verification on the above worst case node**

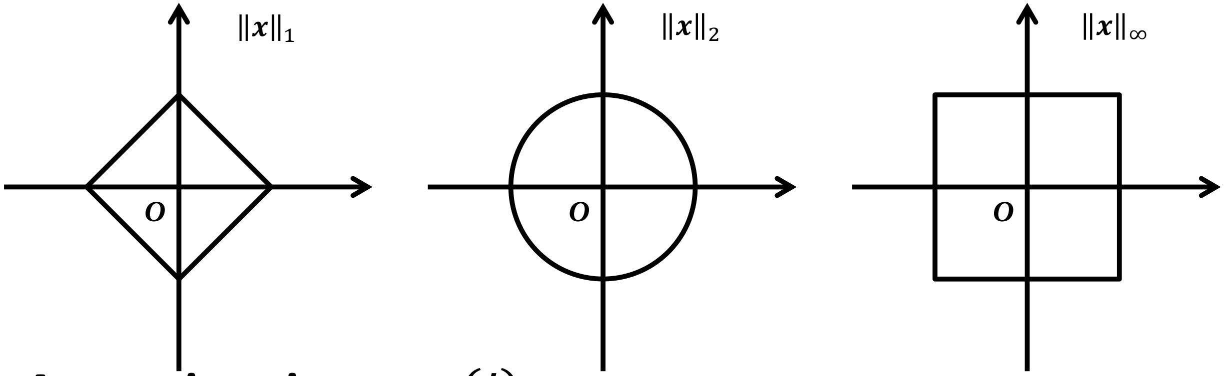
Modified Feasible Region

- **Local support regions**



How to perform group-wise verification?

- **Objective function**
  - **Group wise** $g(\mathbf{i}) = max\ \{v_{P_{j1}}, v_{P_{j2}}, \cdots, v_{P_{jk}}\}$
  - $h(\mathbf{i}) = ln(e^{v_{P_{j1}}} + e^{v_{P_{j2}}} + \cdots + e^{v_{P_{jk}}})$
  - $r(\mathbf{i}) = \left(v_{P_{j1}}^{p} + v_{P_{j2}}^{p} + \cdots + v_{P_{jk}}^{p}\right)^{\frac{1}{p}} (p > 1)$
  - $f(\mathbf{i}) = v_{P_{j1}} + v_{P_{j2}} + \cdots + v_{P_{jk}}$



- **Approximation to $g(i)$**
- **Concave optimization**

Estimating Function

- $f(\mathbf{i}) = v_{P_{j1}} + v_{P_{j2}} + \cdots + v_{P_{jk}}$
  - **Linear programming**
  - **The estimation accuracy is based on the locality effect of the power grid**
- $\tilde{f}(\mathbf{i}) = w_1 v_{P_{j1}} + w_2 v_{P_{j2}} + \cdots + w_k v_{P_{jk}}\ (w_l > 0)$
  - **Handle the influence of current constraints in** $\tilde{\mathcal{L}}$

Group-wise Verification

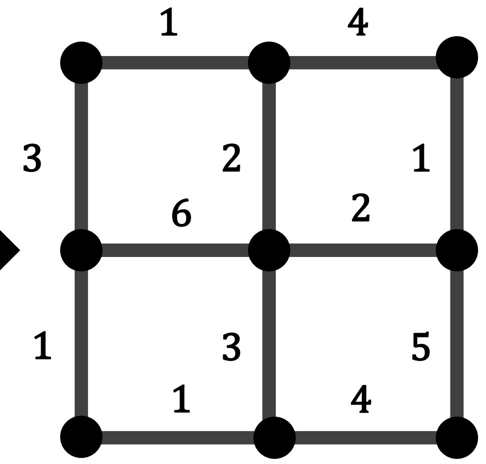
- Element-wise framework
  - Task 1: compute $\boldsymbol{c_i}$ by solving $\boldsymbol{Gx} = \boldsymbol{e_i}$
  - Task 2: maximize $\boldsymbol{v_i} = \boldsymbol{c_i^T i}$ s.t.

    $\boldsymbol{Ui} \leq \boldsymbol{I_G}$ and $\boldsymbol{0} \leq \boldsymbol{i} \leq \boldsymbol{I_L}$
- Group-wise Verification
  - For nodes $P_{j1}, P_{j2}, \ldots, P_{jk}$ in group $\boldsymbol{j}$
  - Compute $f(\mathbf{i}) = v_{P_{j_1}} + v_{P_{j_2}} + \cdots + v_{P_{jk}}$ is to perform
    - Task 1: compute $\boldsymbol{c_j}$ by solving $\boldsymbol{Gx} = \boldsymbol{e_{p_{j1}}} + \boldsymbol{e_{p_{j2}}} + \ldots + \boldsymbol{e_{p_{jk}}}$
    - Task 2: maximize $\boldsymbol{v_j} = \boldsymbol{c_j^T i}$ s. t. $\tilde{\mathcal{L}}$
  - Total cost to verify a power grid with $\boldsymbol{M}$ groups
    - Solving linear equations with $\boldsymbol{N}$ unknowns for $\boldsymbol{M}$ times
    - Solving LP problems for $\boldsymbol{M}$ times

Node Grouping Based on Circuit Partitioning

- **Geometric partitioning**
  - **Need detailed geometric information of the power grid**
- **Algebraic partitioning**
  - **Estimating the influence between any two nodes by computing the shortest path length connecting them in the resistance network**

$$\begin{bmatrix} * & -1 & 0 & -3 & 0 & 0 & 0 & 0 & 0 \\ -1 & * & -4 & 0 & -2 & 0 & 0 & 0 & 0 \\ 0 & -4 & * & 0 & 0 & -1 & 0 & 0 & 0 \\ -3 & 0 & 0 & * & -6 & 0 & -1 & 0 & 0 \\ 0 & -2 & 0 & -6 & * & -2 & 0 & -3 & 0 \\ 0 & 0 & -1 & 0 & -2 & * & 0 & 0 & -5 \\ 0 & 0 & 0 & -1 & 0 & 0 & * & -1 & 0 \\ 0 & 0 & 0 & 0 & -3 & 0 & -1 & * & -4 \\ 0 & 0 & 0 & 0 & 0 & -5 & 0 & -4 & * \end{bmatrix}$$



Experimental Results

- **HW/SW Platforms**
  - **C++ implementation with single thread**
  - ***Cholmod* for solving all involved linear equations**
  - ***lp_solve* for solving linear programming problems**
  - **64-bit Linux server with Intel Xeon E5345 CPU @ 2.33GHz and 8GB RAM**
- **Benchmarks**
  - **Power grid benchmarks for vectorless verification, Prof. Jia Wang, IIT**

Experimental Results

Benchmark information

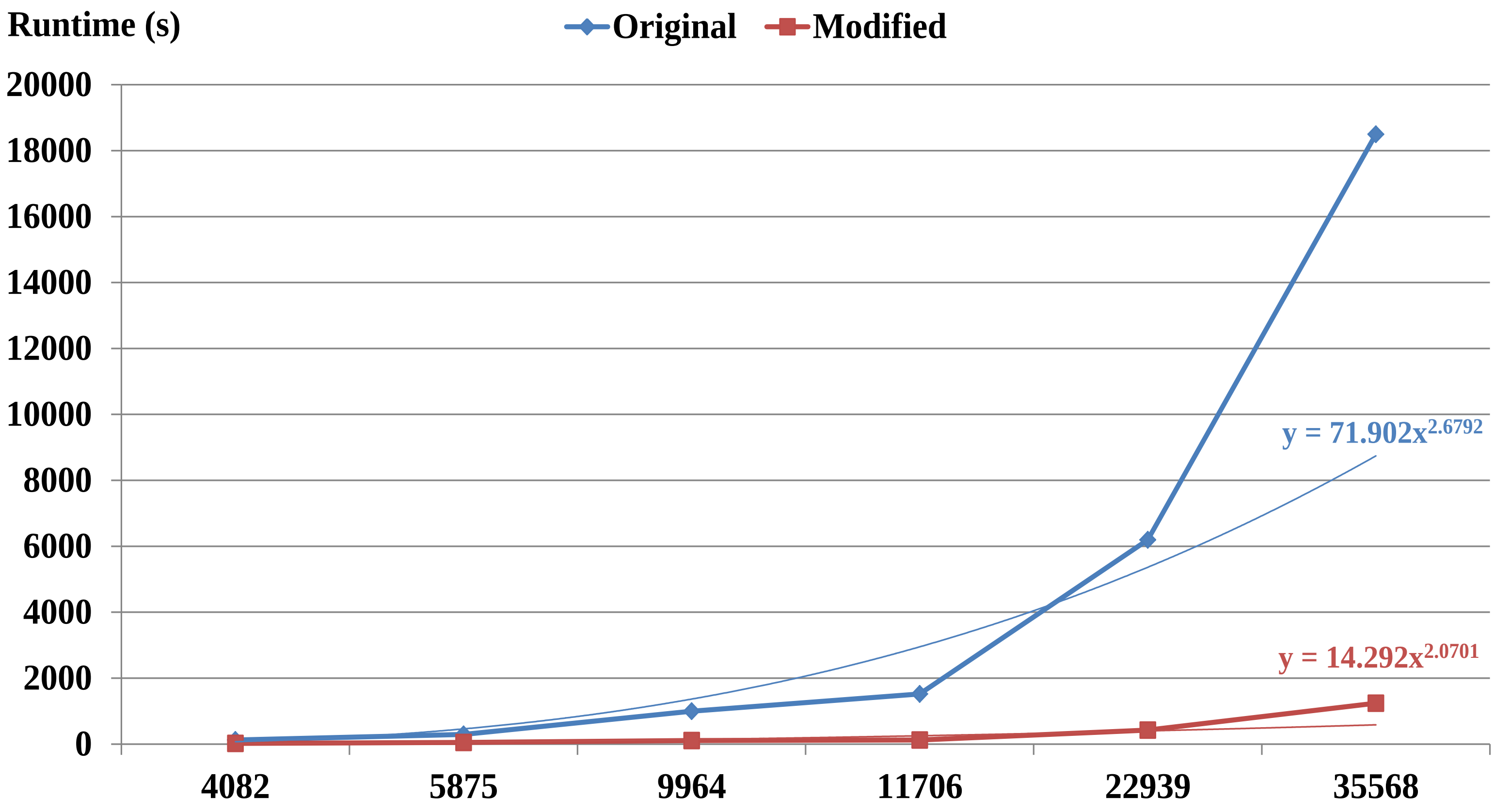
Power Grid	Type	#Nodes	#VDD Pads	#Global Constraints
PG1	2-D irregular	4082	9	6
PG2	3-D regular	5875	9	10
PG3	2-D irregular	9964	16	10
PG4	3-D irregular	11706	18	10
PG5	3-D regular	22939	25	10
PG6	3-D irregular	35568	36	12

Performance

Test Case	#Partitions	Runtime			Error(mV)
		Original	Modified	Speedup	
PG1	16	122.46s	21.16s	**5.79**	0.17
PG2	16	293.75s	48.63s	**6.04**	0
PG3	25	996.41s	105.43s	**9.45**	7.53
PG4	32	25.36m	122.76s	**12.40**	0
PG5	36	1.72h	424.35s	**14.60**	0
PG6	36	5.14h	20.66m	**14.92**	2.81

Experimental Results

- Runtime



Summary

- **Simulation is not enough for PG verification, more attention should be taken into vectorless approach.**
- **This paper proposed a modified vectorless power grid verification framework using a maximum voltage drop location estimation technique.**
- **The implementations of the group-wise verification are essential for significantly reducing the verification complexity.**
- **The experimental results show the verification accuracy is acceptable and the speedups are significant.**

THANKS FOR YOUR ATTENTION!
Q & A