Fast Vectorless Power Grid Verification using Maximum Voltage Drop Location Estimation

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Outline

- Introduction to Vectorless Verification
- Proposed Approach
  - Worst case location estimation
  - Group-wise verification
- Experimental Results & Summary
Power Grid Verification

- Design Challenge
  - Billion-transistors VLSI design
  - Early stage power grid safety check

Simulation is not enough!

Doing It Early Matters!

Impact on Project:
- No Iteration
- Fast Iteration

Design Cycle:
- Front End
- P & R
- Tape Out

(C) 2010 Apache Design, Inc.
Simulation vs. Vectorless

Simulation approach
- Input current patterns are required
- Solving linear equations to obtain voltage distribution

Vectorless approach
- Lack of knowledge of circuit details in early design stage
- Current constraints are required according to circuit behavior with uncertainty working mode
- **Problem**: Verify the grid voltages under all possible current waveforms that satisfy the current constraints
- Provide a specification or budget based framework for the power grid prototyping

\[ Gv = i \]

\[ v = G^{-1}i \]
Problem Definition

- Current Constraints
  - Local constraints: upper bound on individual current sources
    \[ 0 \leq i \leq I_L \]
  - Global constraints: bounds on sums of groups of currents
    \[ U_i \leq I_G \]

- Obtain the worst case of the grid voltage
  - To estimate the worst-case voltage fluctuations by solving optimization problems
    \[ \nu = G^{-1}i \]
  - Maximize voltage drops subject to current constraints
    \[
    \text{maximize } \nu \quad \text{s.t.} \\
    G\nu = i \quad , \quad U_i \leq I_G \quad \text{and} \quad 0 \leq i \leq I_L
    \]
Vectorless Power Grid Verification

- The problem can be divided into two major tasks

  - Let $c_i \triangleq G^{-1}e_i$
    where $e_i$ is the $n \times 1$ vector of all zeros except the $i$-th component being 1, it is to obtain the $i$-th column of $G^{-1}$ by solving $Gx = e_i$

  - The voltage of the $i$-th node can be obtained by
    $$v_i = c_i^T i$$

  - Task 1: compute $c_i$ by solving $Gx = e_i$
  - Task 2: maximize $v_i = c_i^T i$ s.t.
    $$Ui \leq I_G \quad \text{and} \quad 0 \leq i \leq I_L$$

- Total cost to verify a power grid with $N$ nodes

  - Solving linear equations with $N$ unknowns for $N$ times
  - Solving LP problems for $N$ times
Motivation

- Prototype Vectorless Power Grid Verification
  - Element-wise verification
    
    1. For $k = 1$ to $n$
    2. Maximize $v_k = (G^{-1}e_k)^T i$ s.t. $i \in \mathcal{L}$
    3. Let $v_{\text{max}_k} = \max v_k$
    4. End For
    5. Find $v_{\text{max}} = \max \{v_{\text{max}_1}, v_{\text{max}_2}, \ldots, v_{\text{max}_n}\}$

- Maximum voltage drop location estimation
  - Group-wise verification
    
    1. Maximize $f(i) = f(v_{P_{j_1}}, v_{P_{j_2}}, \ldots, v_{P_{j_k}})$ s.t. $i \in \tilde{\mathcal{L}}$
    2. Let $i_j^* = \text{argmax}_{i \in \tilde{\mathcal{L}}} f(i)$
    3. Find $v_{P_{j^*}}(i_j^*) = \max \{v_{P_{j_1}}(i_j^*), v_{P_{j_2}}(i_j^*), \ldots, v_{P_{j_k}}(i_j^*)\}$
Node grouping based on circuit partitioning
- Divide the set of power grid nodes into $k$ subsets
- Node grouping from each subset

Verification for each group nodes
- Maximization for the objective of each group
- Obtain the current solution $i_j^* = \arg\max_{i \in \mathcal{L}} f(i)$
- Find the worst case node of this group by substituting $i_j^*$ to each grid node
- Perform accurate verification on the above worst case node
Modified Feasible Region

- Local support regions

A Group of Selected Power Grid Nodes

Global Current Constraints

Local Support Regions
How to perform group-wise verification?

- **Objective function**
  - Group wise \( g(i) = \max \{v_{Pj_1}, v_{Pj_2}, \ldots, v_{Pj_k}\} \)
  - \( h(i) = \ln(e^{v_{Pj_1}} + e^{v_{Pj_2}} + \cdots + e^{v_{Pj_k}}) \)
  - \( r(i) = \left(v_{Pj_1}^p + v_{Pj_2}^p + \cdots + v_{Pj_k}^p\right)^{\frac{1}{p}} (p > 1) \)
  - \( f(i) = v_{Pj_1} + v_{Pj_2} + \cdots + v_{Pj_k} \)

- Approximation to \( g(i) \)
- Concave optimization
Estimating Function

- \( f(i) = v_{P_{j1}} + v_{P_{j2}} + \cdots + v_{P_{jk}} \)
  - Linear programming
  - The estimation accuracy is based on the locality effect of the power grid

- \( \tilde{f}(i) = w_1 v_{P_{j1}} + w_2 v_{P_{j2}} + \cdots + w_k v_{P_{jk}} \quad (w_l > 0) \)
  - Handle the influence of current constraints in \( \tilde{L} \)
Group-wise Verification

- Element-wise framework
  - Task 1: compute $c_i$ by solving $Gx = e_i$
  - Task 2: maximize $v_i = c_i^T i$ s.t. $Ui \leq I_G$ and $0 \leq i \leq I_L$

- Group-wise Verification
  - For nodes $P_{j1}, P_{j2}, ..., P_{jk}$ in group $j$
  - Compute $f(i) = v_{P_{j1}} + v_{P_{j2}} + \cdots + v_{P_{jk}}$ is to perform
    - Task 1: compute $c_j$ by solving $Gx = e_{P_{j1}} + e_{P_{j2}} + \cdots + e_{P_{jk}}$
    - Task 2: maximize $v_j = c_j^T i$ s. t. $\tilde{L}$

- Total cost to verify a power grid with $M$ groups
  - Solving linear equations with $N$ unknowns for $M$ times
  - Solving LP problems for $M$ times
Node Grouping Based on Circuit Partitioning

- **Geometric partitioning**
  - Need detailed geometric information of the power grid

- **Algebraic partitioning**
  - Estimating the influence between any two nodes by computing the shortest path length connecting them in the resistance network

\[
\begin{bmatrix}
* & -1 & 0 & -3 & 0 & 0 & 0 & 0 & 0 & 0 \\
-1 & * & -4 & 0 & -2 & 0 & 0 & 0 & 0 & 0 \\
0 & -4 & * & 0 & 0 & -1 & 0 & 0 & 0 & 0 \\
-3 & 0 & 0 & * & -6 & 0 & -1 & 0 & 0 & 0 \\
0 & -2 & 0 & -6 & * & -2 & 0 & -3 & 0 & 0 \\
0 & 0 & -1 & 0 & -2 & * & 0 & 0 & -5 & 0 \\
0 & 0 & 0 & -1 & 0 & 0 & * & -1 & 0 & 0 \\
0 & 0 & 0 & 0 & -3 & 0 & -1 & * & -4 & 0 \\
0 & 0 & 0 & 0 & 0 & -5 & 0 & -4 & * & 0
\end{bmatrix}
\]
Experimental Results

- **HW/SW Platforms**
  - C++ implementation with single thread
  - *Cholmod* for solving all involved linear equations
  - *lp_solve* for solving linear programming problems
  - 64-bit Linux server with Intel Xeon E5345 CPU @ 2.33GHz and 8GB RAM

- **Benchmarks**
  - Power grid benchmarks for vectorless verification, Prof. Jia Wang, IIT
## Experimental Results

### Benchmark information

<table>
<thead>
<tr>
<th>Power Grid</th>
<th>Type</th>
<th>#Nodes</th>
<th>#VDD Pads</th>
<th>#Global Constraints</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG1</td>
<td>2-D irregular</td>
<td>4082</td>
<td>9</td>
<td>6</td>
</tr>
<tr>
<td>PG2</td>
<td>3-D regular</td>
<td>5875</td>
<td>9</td>
<td>10</td>
</tr>
<tr>
<td>PG3</td>
<td>2-D irregular</td>
<td>9964</td>
<td>16</td>
<td>10</td>
</tr>
<tr>
<td>PG4</td>
<td>3-D irregular</td>
<td>11706</td>
<td>18</td>
<td>10</td>
</tr>
<tr>
<td>PG5</td>
<td>3-D regular</td>
<td>22939</td>
<td>25</td>
<td>10</td>
</tr>
<tr>
<td>PG6</td>
<td>3-D irregular</td>
<td>35568</td>
<td>36</td>
<td>12</td>
</tr>
</tbody>
</table>

### Performance

<table>
<thead>
<tr>
<th>Test Case</th>
<th>#Partitions</th>
<th>Runtime</th>
<th>Error(mV)</th>
<th>Speedup</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Original</td>
<td>Modified</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Speedup</td>
<td></td>
</tr>
<tr>
<td>PG1</td>
<td>16</td>
<td>122.46s</td>
<td>21.16s</td>
<td>5.79</td>
</tr>
<tr>
<td>PG2</td>
<td>16</td>
<td>293.75s</td>
<td>48.63s</td>
<td>6.04</td>
</tr>
<tr>
<td>PG3</td>
<td>25</td>
<td>996.41s</td>
<td>105.43s</td>
<td>9.45</td>
</tr>
<tr>
<td>PG4</td>
<td>32</td>
<td>25.36m</td>
<td>122.76s</td>
<td>12.40</td>
</tr>
<tr>
<td>PG5</td>
<td>36</td>
<td>1.72h</td>
<td>424.35s</td>
<td>14.60</td>
</tr>
<tr>
<td>PG6</td>
<td>36</td>
<td>5.14h</td>
<td>20.66m</td>
<td>14.92</td>
</tr>
</tbody>
</table>
**Experimental Results**

- **Runtime**

![Graph showing runtime comparison](image)

- Equation for Original runtime: \( y = 71.902x^{2.6792} \)
- Equation for Modified runtime: \( y = 14.292x^{2.0701} \)
Summary

- Simulation is not enough for PG verification, more attention should be taken into vectorless approach.
- This paper proposed a modified vectorless power grid verification framework using a maximum voltage drop location estimation technique.
- The implementations of the group-wise verification are essential for significantly reducing the verification complexity.
- The experimental results show the verification accuracy is acceptable and the speedups are significant.
THANKS FOR YOUR ATTENTION!
Q & A