1S-20

A Low-Power VCO based ADC with asynchronous sigma-delta modulator in 65nm CMOS

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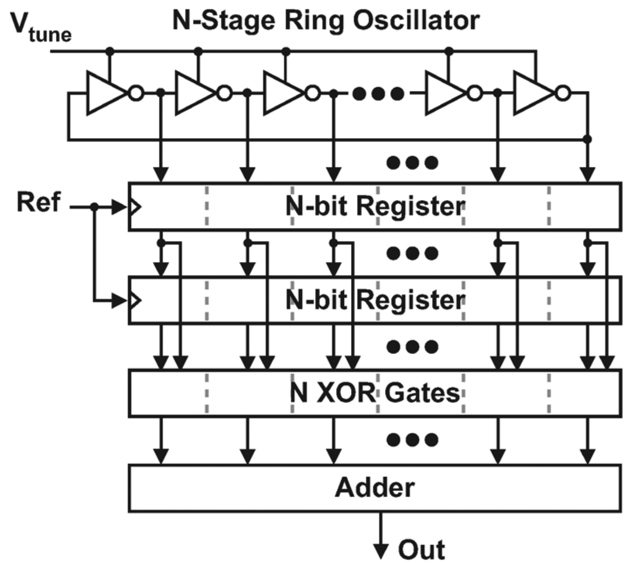
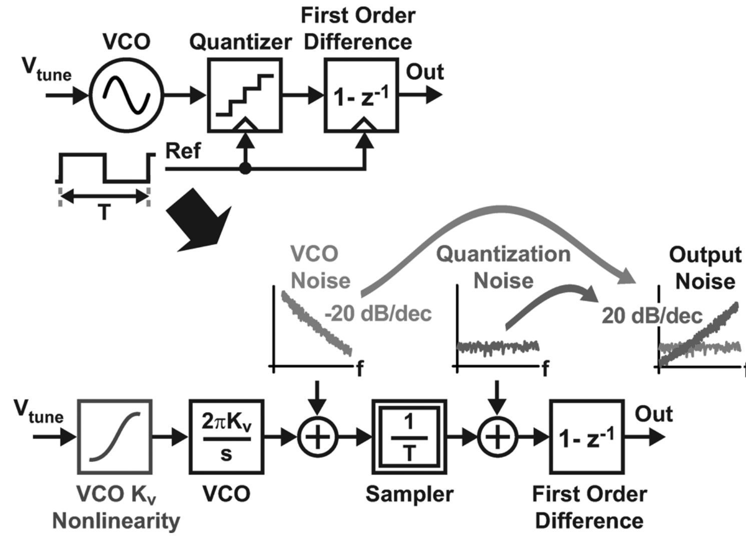
VCO-based Quantizer



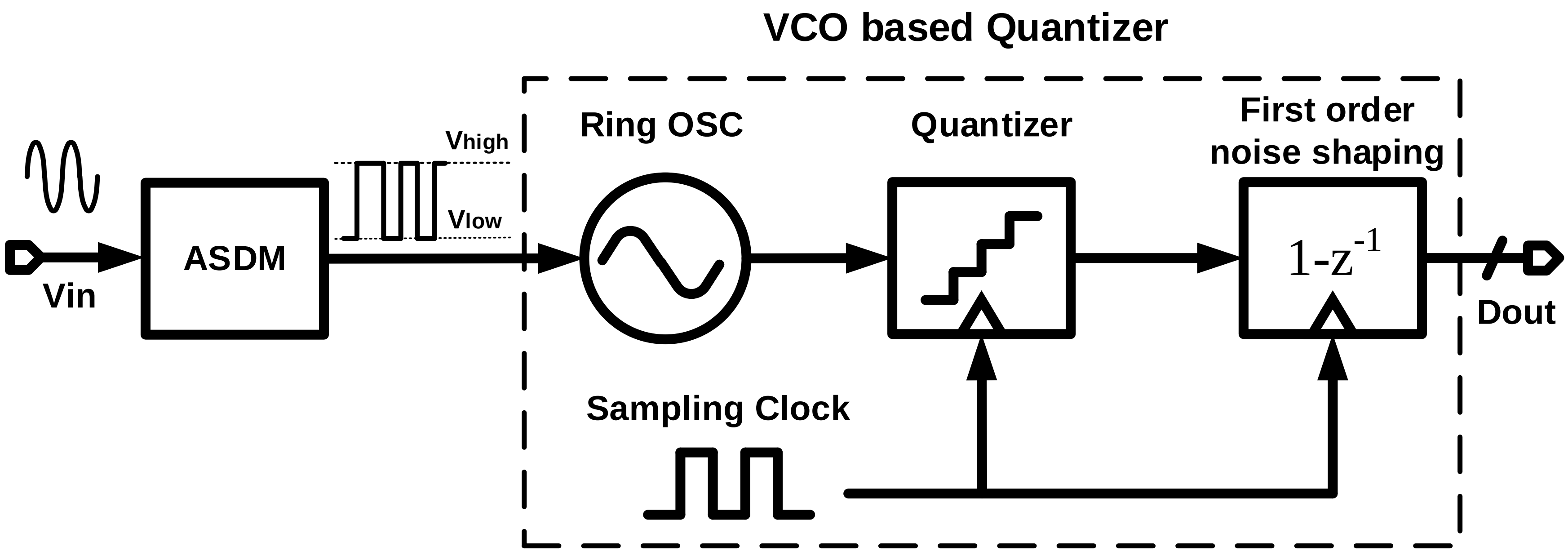
VCO-based quantizer



Equivalent frequency domain model

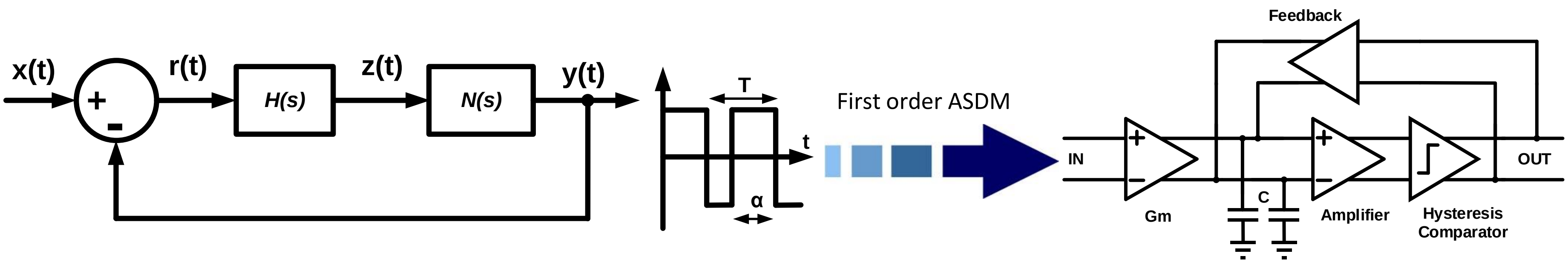
- ✔ Only need VCO and digital gate circuits
- ✔ Time resolution and speed improved with technology scaling
- ✔ First order noise shaping property
- ✘ The non-linearity of the VCO voltage to frequency transfer character limits the performance.

Proposed VCO based ADC with ASDM



- ASDM transfer input signal voltage information into pulse width information in time domain
- VCO only works at two voltage levels: V_{high} and V_{low}
- Sense-amp flip-flops work as phase quantizer

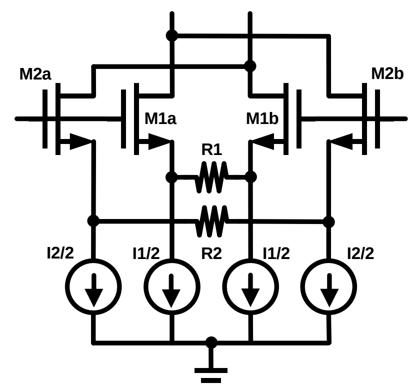
Implementation of ASDM



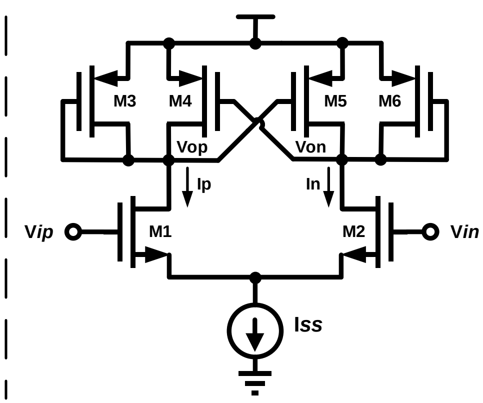
Block diagram of ASDM

- Output Duty cycle : $\frac{\alpha}{T} = \frac{V+1}{2}$
- Self-oscillation frequency : $\frac{\omega}{\omega_c} = 1 - V^2$

Where α is the pulse width, *V is* instantaneous magnitude of input signal that normalized to 1, $T = 2\pi/\omega$ is the output period , ω is the instantaneous frequency of the square, ω_c is self-oscillation frequency when x(t)=0

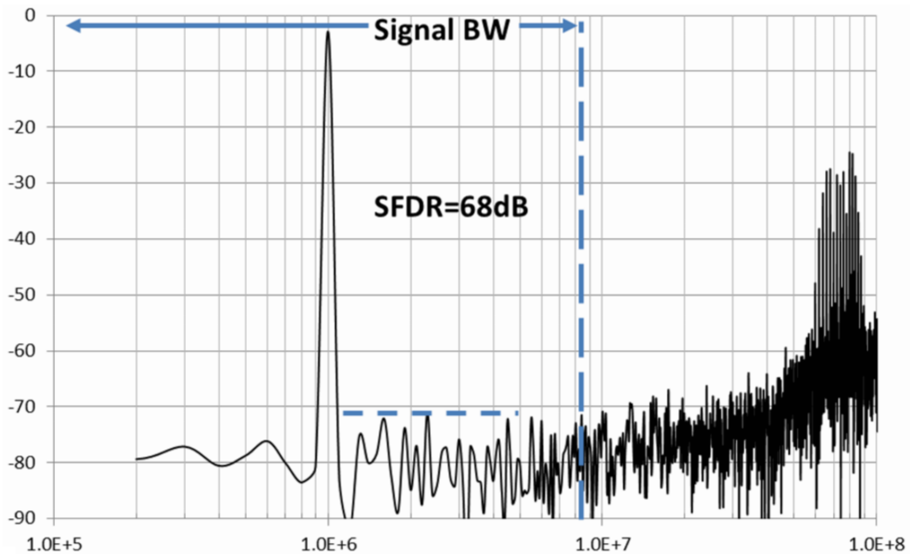


Harmonic-distortion cancelling V-I converter

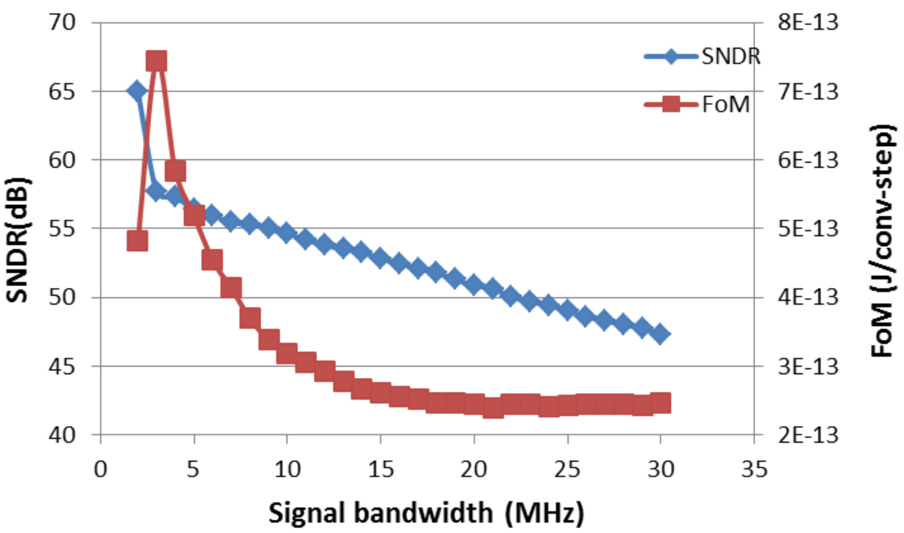


Hysteresis Comparator

Measurement result



Output Spectrum of proposed ADC with 600 $mV_{pp\text{-}diff}$ 1 MHz tone



SNDR&FOM vs. signal Bandwidth

Fsampling MHz	BW MHz	SNR dB	SNDR dB	ENOB bits	Power mW	Area mm^2	FoM fJ/conv
1500	8	54.8	54.3	8.7	2.8	0.08	334

Reference

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