A Low-Power VCO based ADC with asynchronous sigma-delta modulator in 65nm CMOS

Jili Zhang, Chenluan Wang, Shengxi Diao, Fujiang Lin

University of Science and Technology of China, Hefei, China
Only need VCO and digital gate circuits
Time resolution and speed improved with technology scaling
First order noise shaping property
The non-linearity of the VCO voltage to frequency transfer character limits the performance.
Proposed VCO based ADC with ASDM

- ASDM transfer input signal voltage information into pulse width information in time domain
- VCO only works at two voltage levels: $V_{high}$ and $V_{low}$
- Sense-amp flip-flops work as phase quantizer
Output Duty cycle: \( \frac{\alpha}{T} = \frac{V + 1}{2} \)

Self-oscillation frequency: \( \frac{\omega}{\omega_c} = 1 - V^2 \)

Where \( \alpha \) is the pulse width, \( V \) is instantaneous magnitude of input signal that normalized to 1, \( T = \frac{2\pi}{\omega} \) is the output period, \( \omega \) is the instantaneous frequency of the square, \( \omega_c \) is self-oscillation frequency when \( x(t) = 0 \)
### Measurement result

**Output Spectrum of proposed ADC with 600 mV_{pp-diff} 1 MHz tone**

**SNDR&FOM vs. signal Bandwidth**

<table>
<thead>
<tr>
<th>Fsampling (MHz)</th>
<th>BW (MHz)</th>
<th>SNR (dB)</th>
<th>SNDR (dB)</th>
<th>ENOB (bits)</th>
<th>Power (mW)</th>
<th>Area (mm²)</th>
<th>FoM (fJ/conv)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1500</td>
<td>8</td>
<td>54.8</td>
<td>54.3</td>
<td>8.7</td>
<td>2.8</td>
<td>0.08</td>
<td>334</td>
</tr>
</tbody>
</table>
Reference


