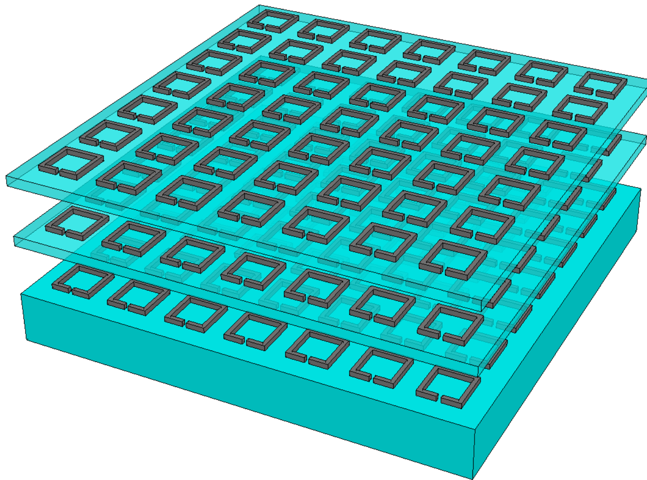
Circuit and Package Design for 44GB/s Inductive-Coupling DRAM/SoC Interface

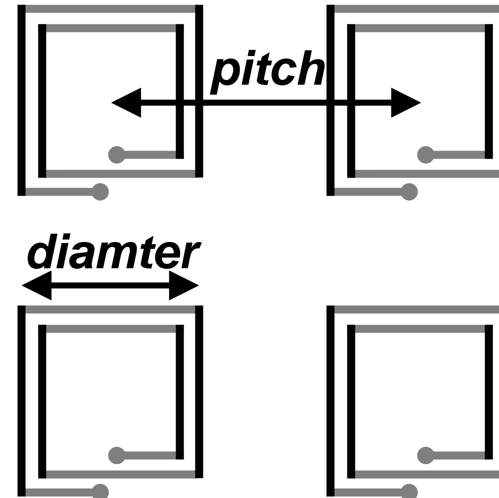
Akira Okada, Abdul Raziz Junaidi, Yasuhiro Take, Atsutake Kosuge and Tadahiro Kuroda

Keio University, Japan

Background

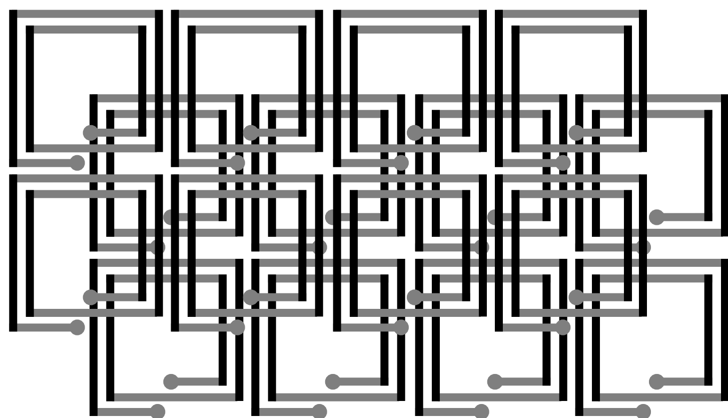
- ►Thru-Chip Interface (TCI) is low cost, low power interface between stacked chips alternative to TSV.
- ►Issues of TCI: Area Inefficiency
  - – Number of coils is limited due to area constraints of the IO region.
  - – To locate many coils in IO region, *pitch* or *diameter* of the coils should be reduced

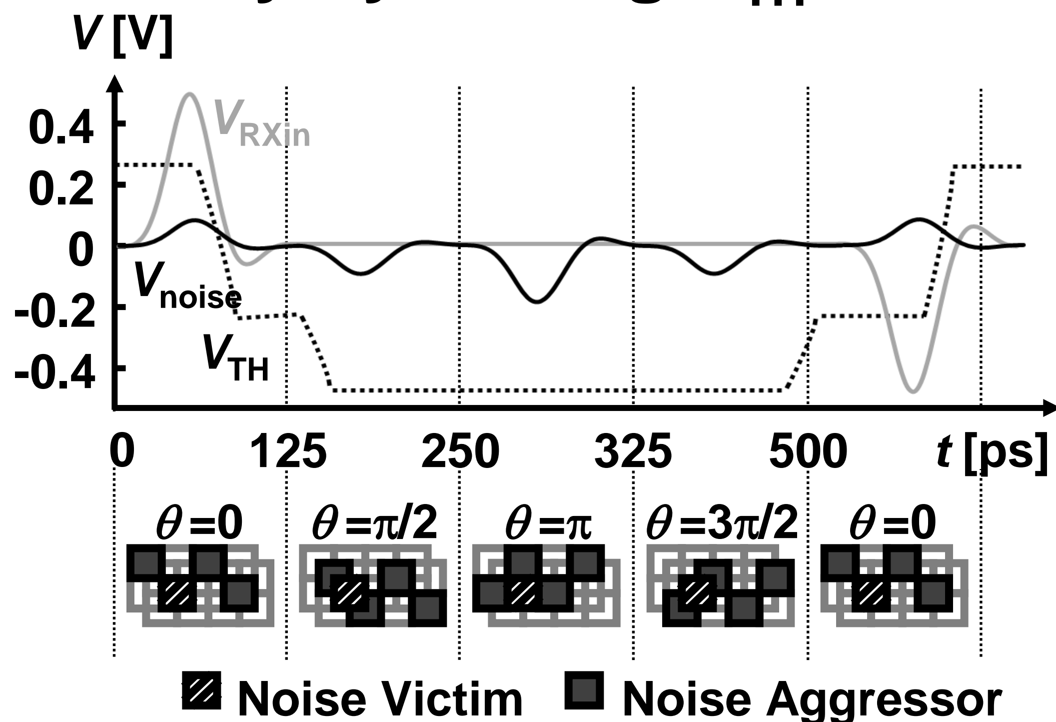




Overlapping coils with quadrature phase division multiplexing

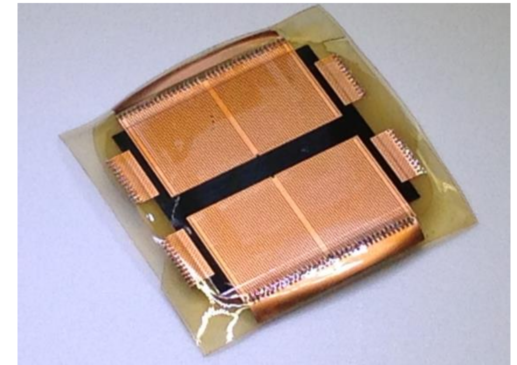
- ►Overlapping coils are formed by multilayer wires
- ►Active channels for communication are switched at four different phases to avoid cross talk
- ►Strengthens noise immunity by raising V_{TH}

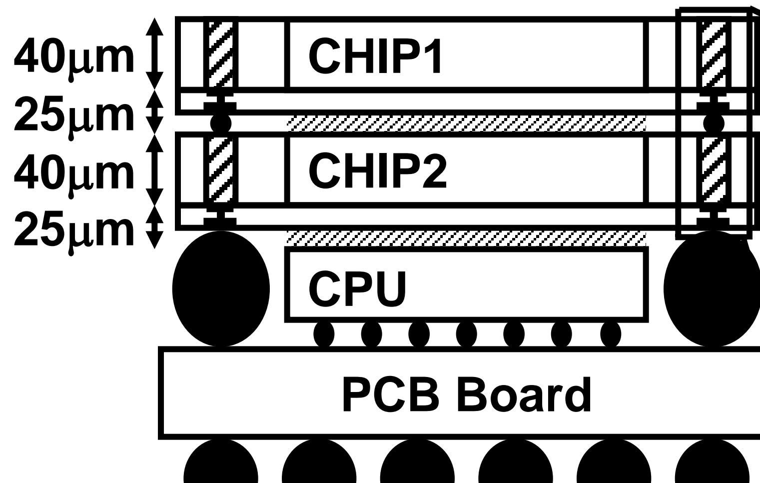


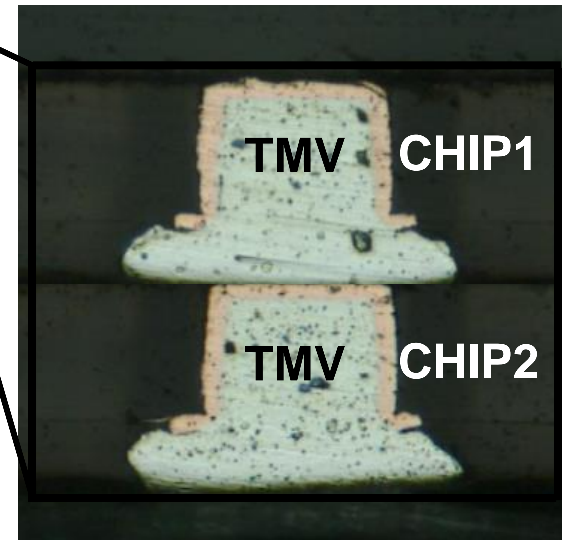


Ultra-thin fan-out wafer level package

- ►UT-FOWLP is Low cost package technology
- ►Chip communication distance is reduced compared to TAB
  - Thickness: from 70μm to 40μm
  - Distance: from 45μm to 25μm

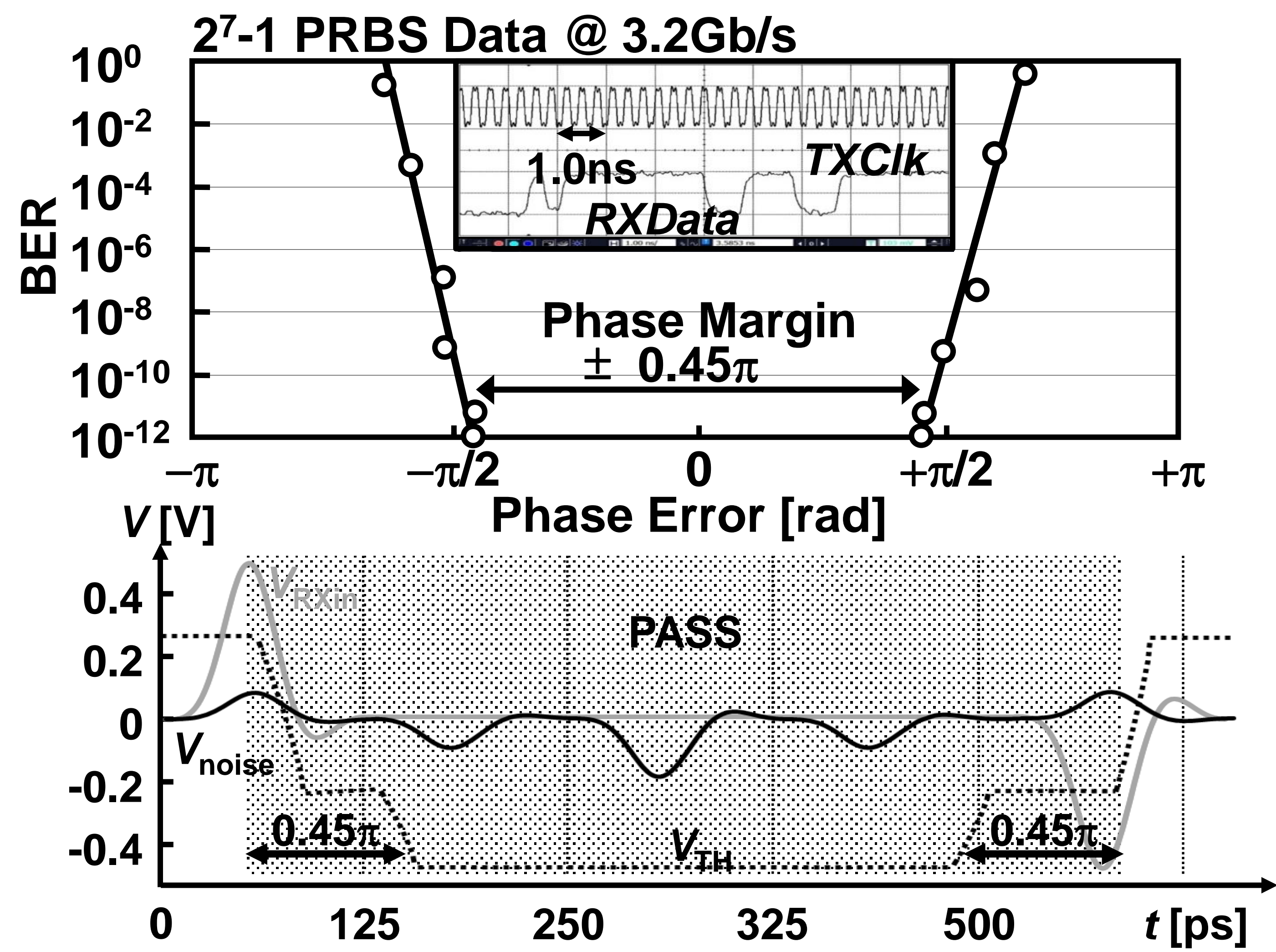






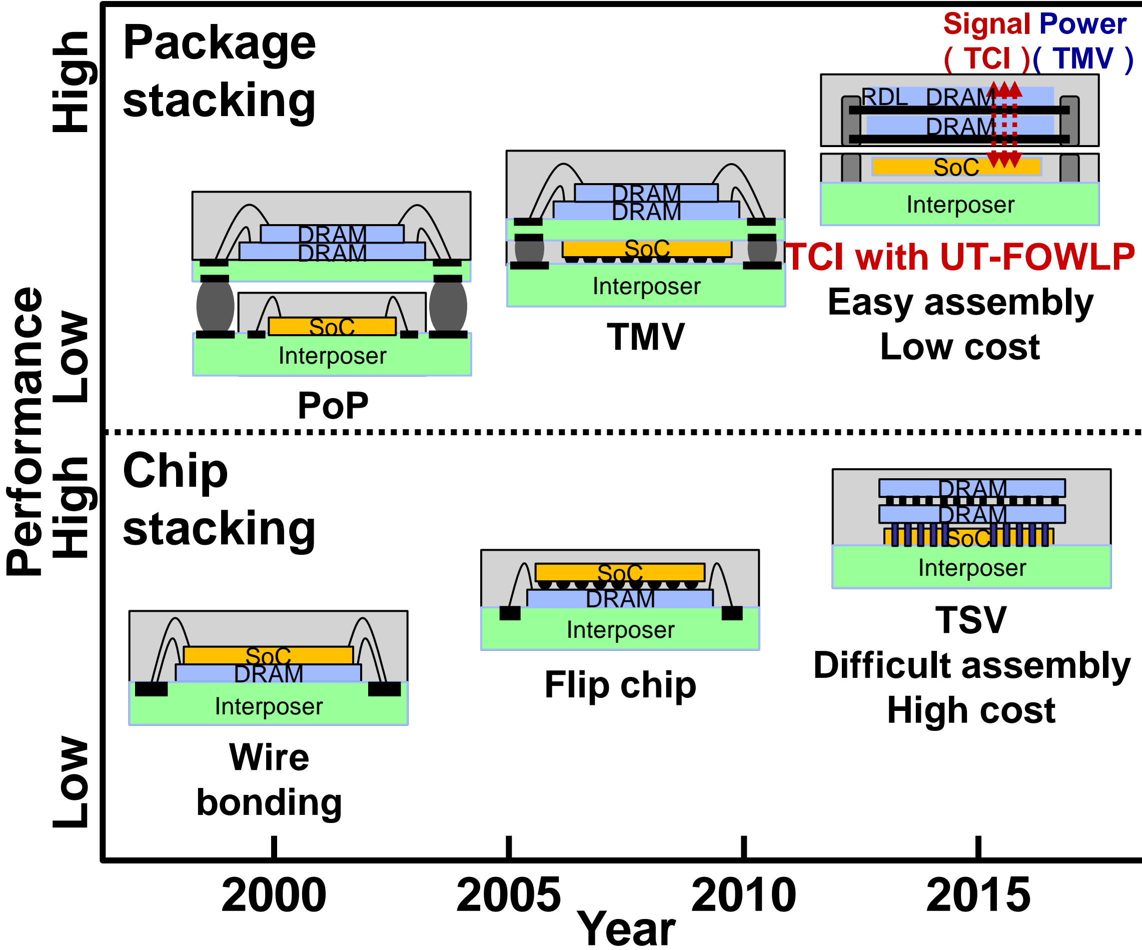
Measurement result

► Communication with BER<10^{-12} is verified



TCI with UT-FOWLP utilizes the advantages of TSV

► TCI outperforms TSV in terms of area efficiency and power efficiency



	TCI-WI02 [this work]	TSV-WIO[1]
Data Bandwidth	44GB/s	12.8GB/s
Number of Data Links	44	512
Data Rate / Link	8Gb/s/link (40)	0.2Gb/s/link (1)
IO Area	2.08mm²	2.70mm²
Area Efficiency	0.0059 mm²/Gb/s (0.22)	0.0264 mm²/Gb/s (1)
Power Efficiency	0.71 mW/Gb/s (0.91)	0.78 mW/Gb/s (1)

[1] J. Kim, et al., ISSCC, pp. 496-497, 2011.