

Reliability-Configurable Mixed-Grained Reconfigurable Array Compatible with High-Level Synthesis

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1S-7 Background

- NRE cost is elevating as VLSI technology advances.
 - Reconfigurable VLSIs are widely used to save cost.
- Guaranteeing reliability of information systems becomes a societal requirement.

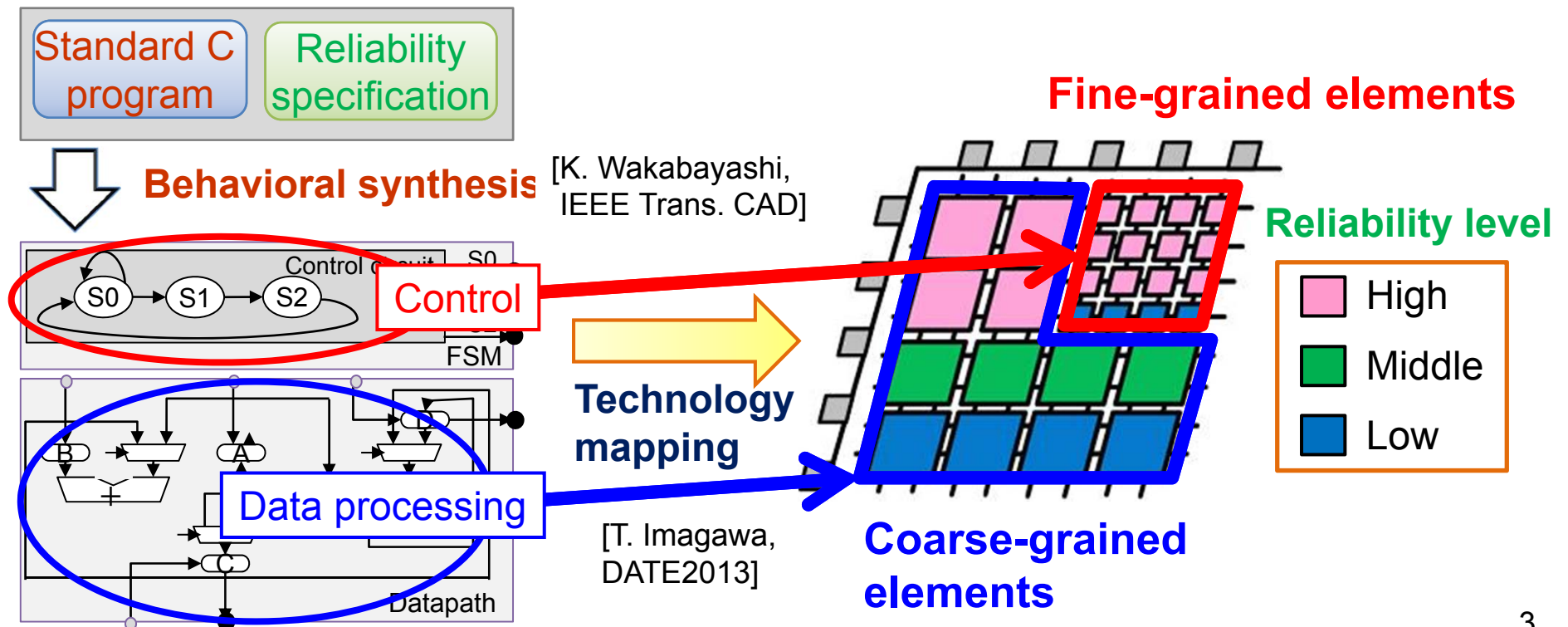


- Reliability of reconfigurable VLSIs is drawing much attention
 - especially from mission critical applications such as space and medical ones.

1S-7 Objective

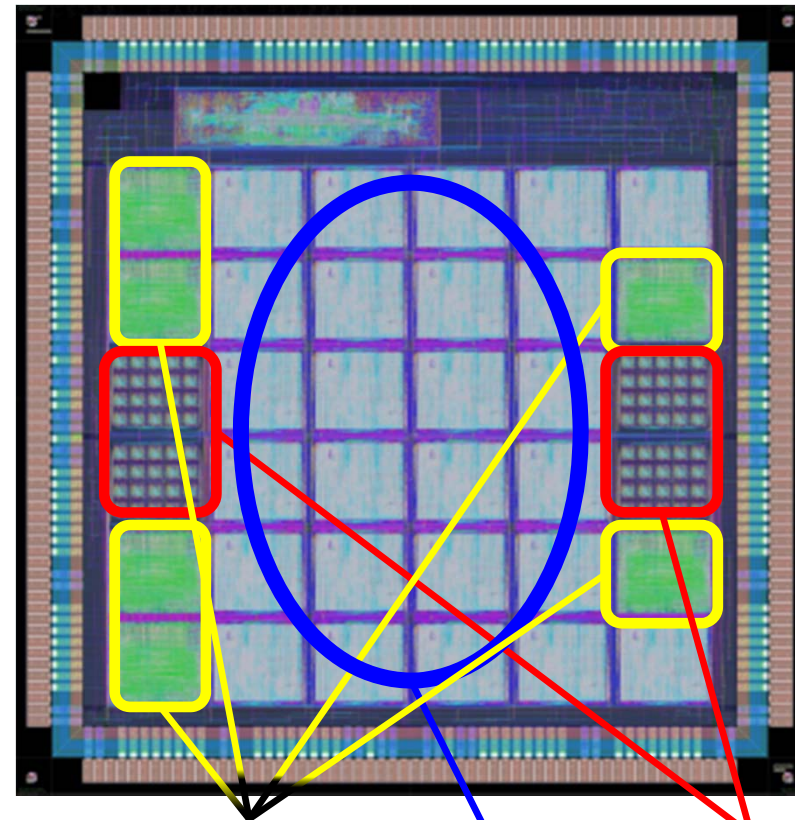
Develop a **mixed-grained reliability-variable** reconfigurable array enabling **C-based design**

- **Fine-grained** elements for state machine
- **Coarse-grained** elements for data processing
- **Element-wise configuration to cover various apps.**



1S-7 Implementation

Process	65nm 12ML CMOS
Die size	4.2 x 4.2 mm ²
Config. bits	165,312
#gates	ALU: 120k, LUT: 4k, MEM: 99k



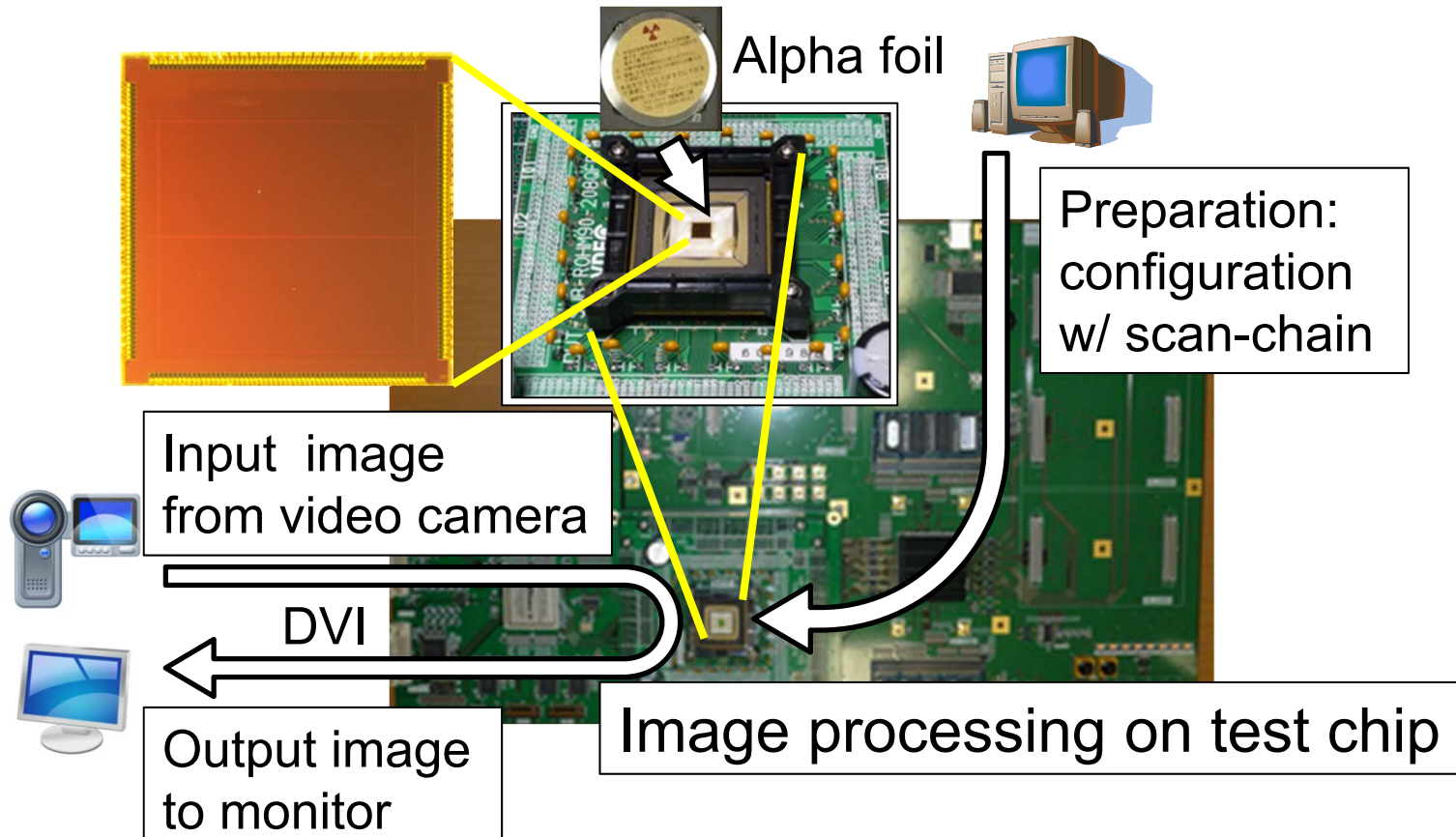
MEM clusters
Memory

ALU clusters
Coarse-grained

LUT blocks
Fine-grained

1S-7 Demonstration setup

- To validate the functionality and reliability, a demonstration using two mappings with different reliability levels was performed.



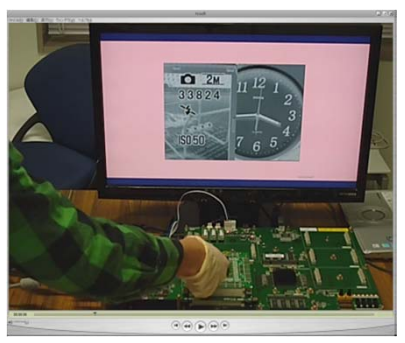
1S-7 Demo: Alpha irradiation test

Start irradiation

After 10 secs.

Normal mapping

- config. mem. singular
- datapaths singular



4 trials

High reliability mapping

- config. mem. triplicated
- datapaths singular



Trial #1	Trial #2
Trial #3	Trial #4

Corrupted or stopped

All working

Single chip can cover wide reliability specifications with different mappings.