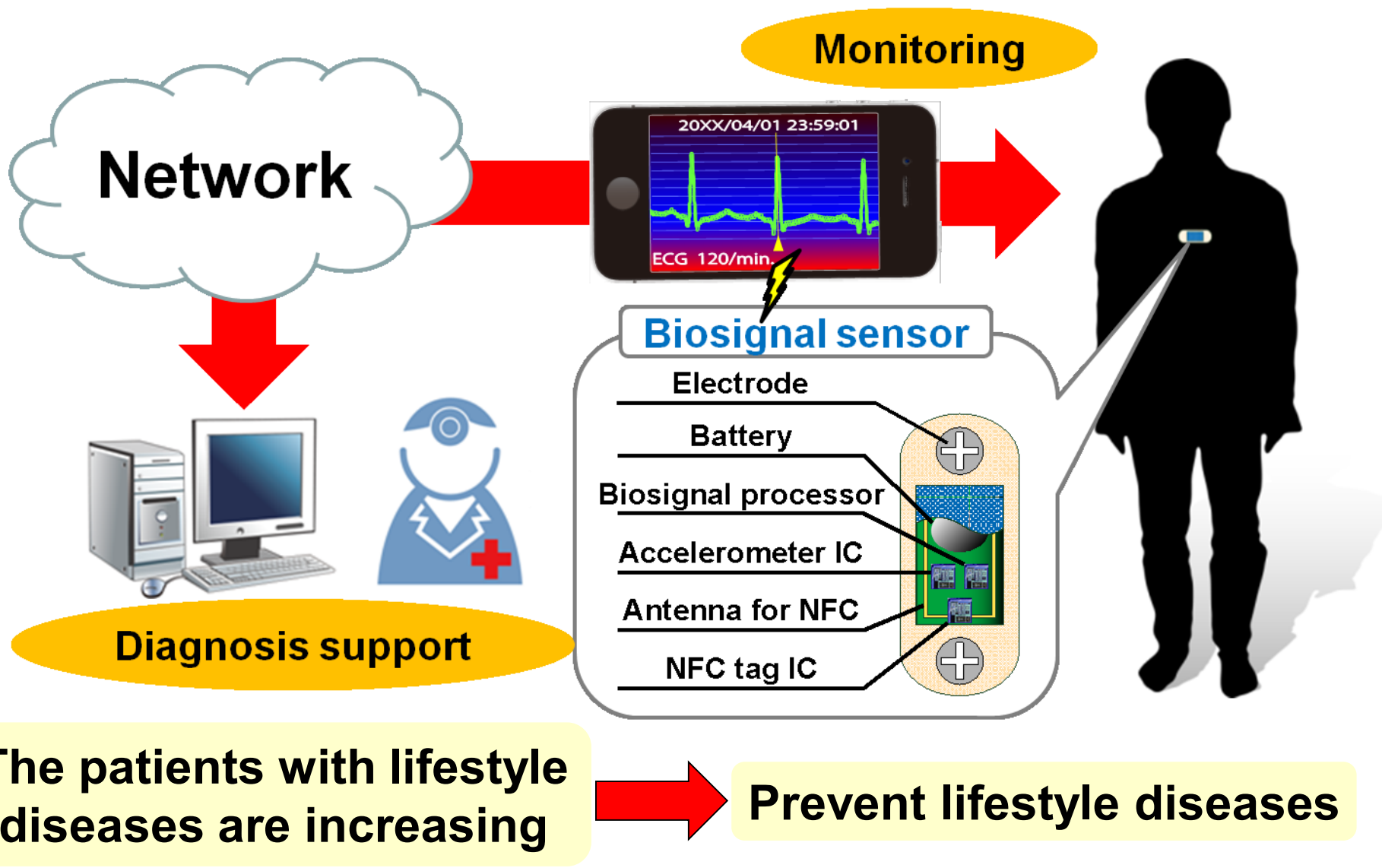


A 14 μ A ECG processor with Noise Tolerant Heart Rate Extractor and FeRAM for Wearable Healthcare Systems

Yozaburo Nakai, Shintaro Izumi, Masanao Nakano, Ken Yamashita, Hiroshi Kawaguchi, and Masahiko Yoshimoto

Kobe University, Japan

Background

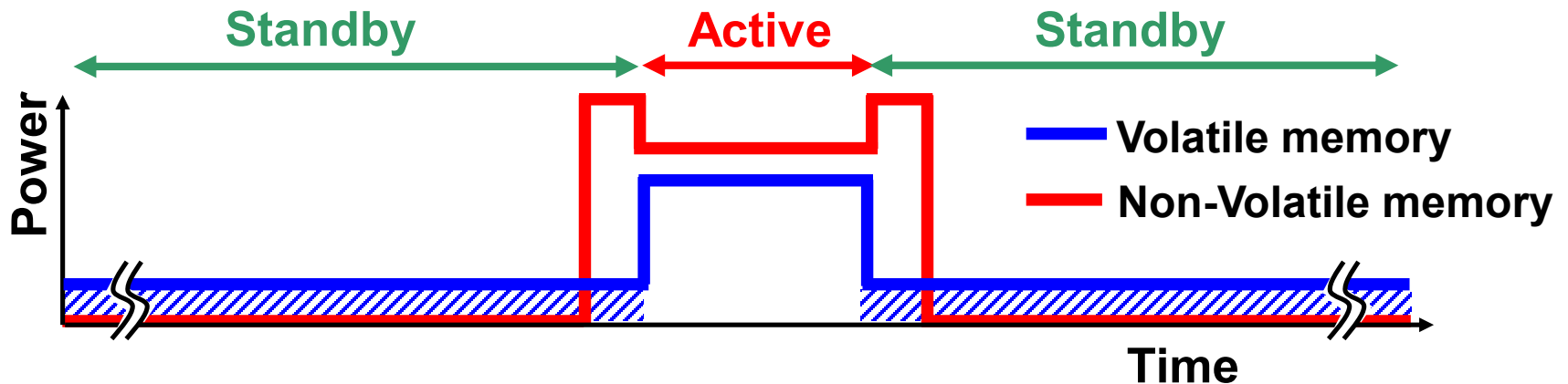


Normally-Off computing

	Frequency component
ECG	0.1 - 150Hz
EEG	0.5 - 60Hz
VEP	0.5 - 60Hz
EMG	few kHz

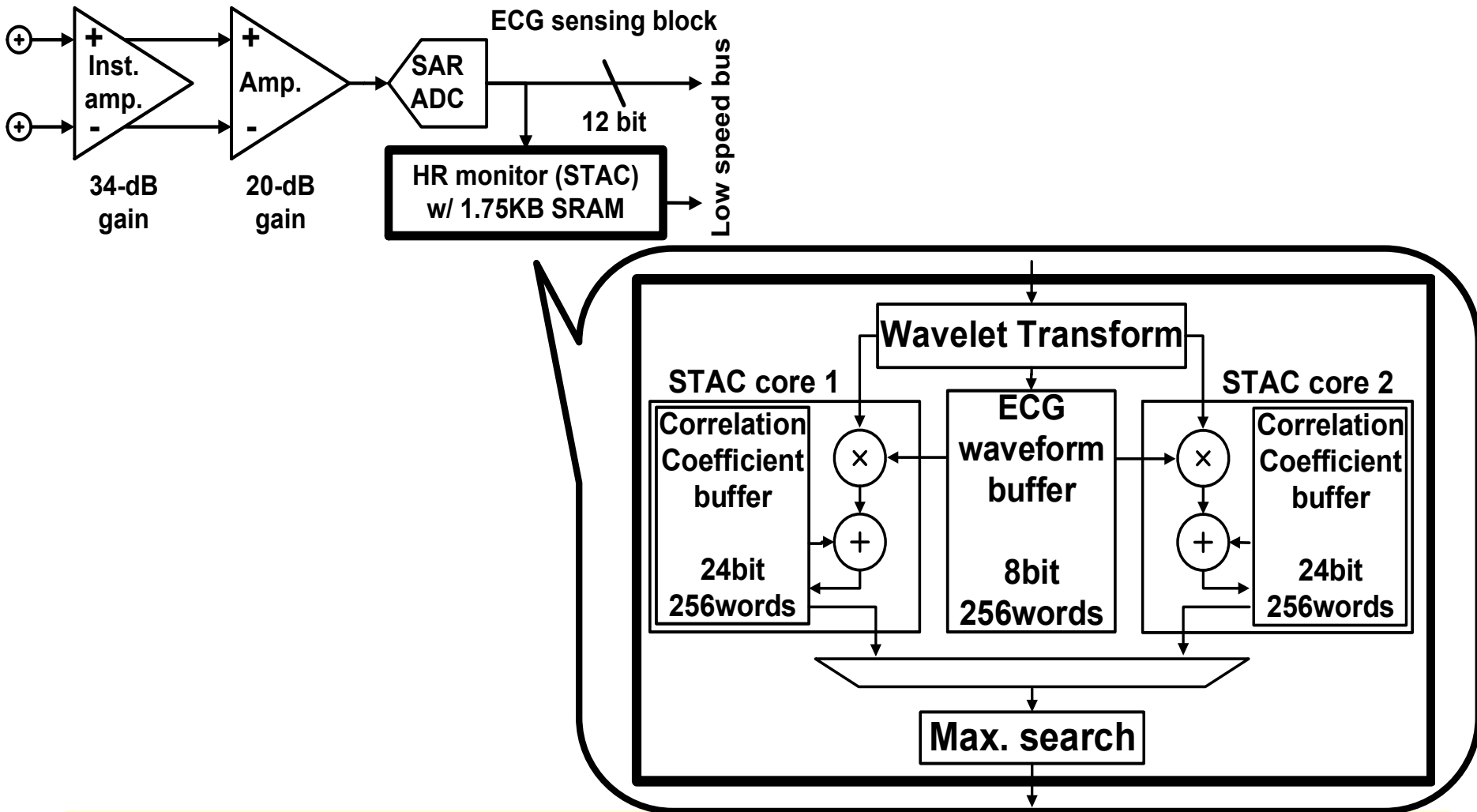
Operational clock
✓ CPU
✓ MPU
etc...

- Frequency range of biosignal is low
→ Standby power reduction is effective



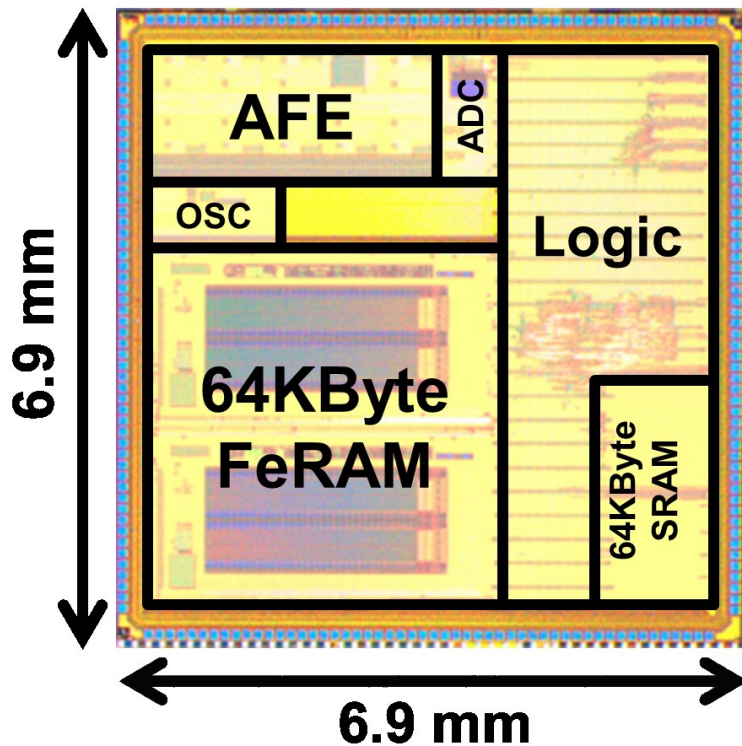
We use Normally-Off technique to the memory

Heart rate detection algorithm



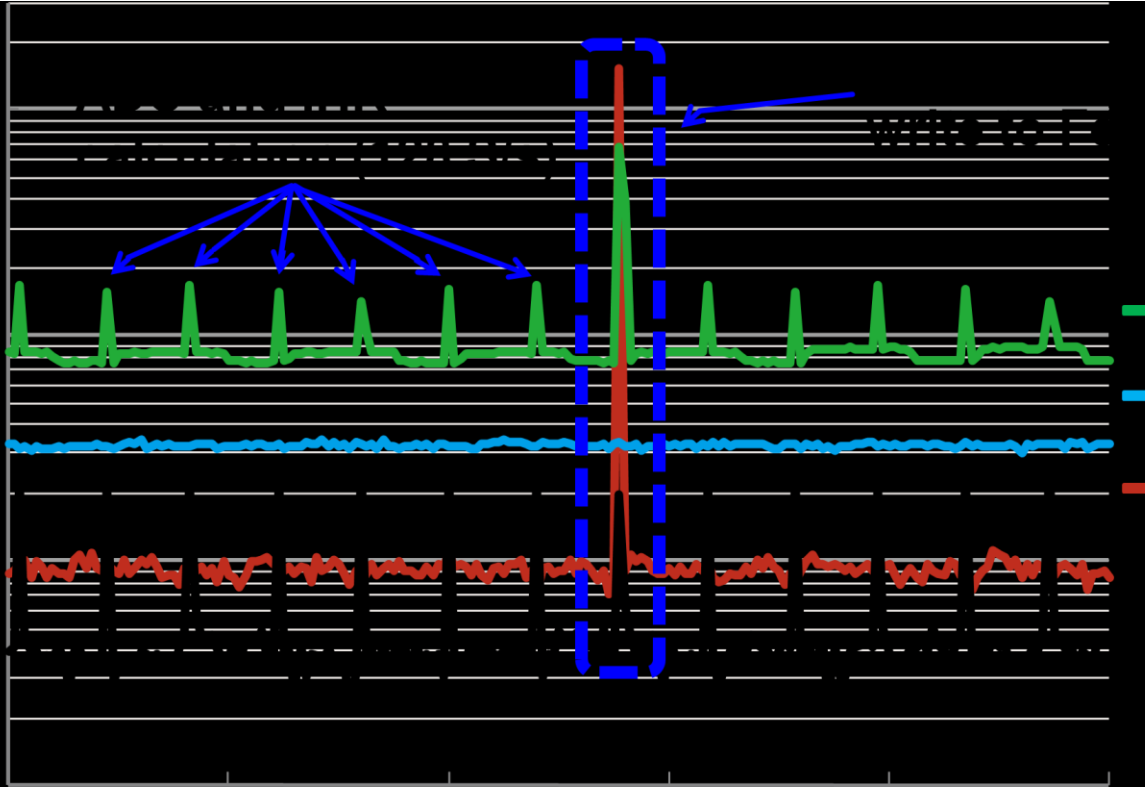
Use the correlation coefficient to calculate a heart rate

Chip photograph



Technology	130-nm CMOS	
Supply voltage	1.2V (Digital, SRAM, ADC, AFE)	
	3.0V (FeRAM, 32kHz OSC, I/O)	
Chip area	6.9 mm × 6.9 mm	
Frequency	24 MHz (for MCU)	
	32 kHz (for other blocks)	
MCU	32-bit Cortex M0	
On chip memory	64-KB FeRAM (for logging data)	
	64-KB SRAM (for MCU)	
	1.75-KB SRAM (for IHR detector)	
ADC	Resolution	12 bit
	Current	0.5 μA @128 S/s, 1.4 μA @1 kS/s
AFE	Gain	54 dB
	Bandwidth	0-100 Hz
	CMRR	73 dB
	Current	3.4 μA
Total current	13.7 μA (for heart rate logging)	

Performance evaluation



The measured total current consumption is **13.7** μA for the heart rate logging application