Cut Mask Optimization with Wire Planning in Self-Aligned Multiple Patterning Full-Chip Routing

Shao-Yun Fang

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Department of Electrical Engineering
National Taiwan University of Science and Technology

TAIWAN TECH National Taiwan University of Science and Technology

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Introduction

SAMP Routing Rules and Post Layout Optimization

SAMP Full-Chip Routing with Wire Planning

Experimental Results

Conclusions

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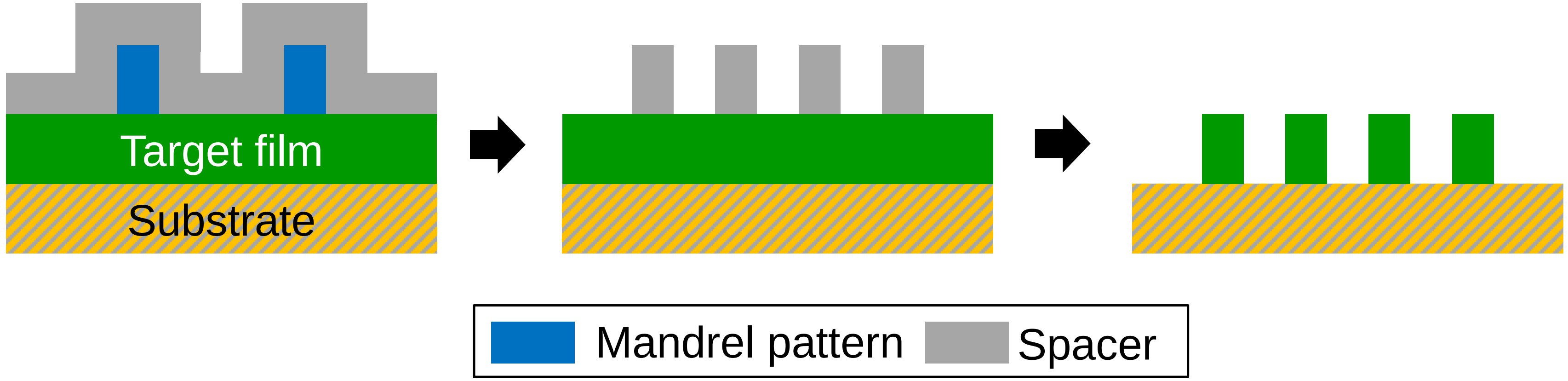
Self-Aligned Multiple Patterning

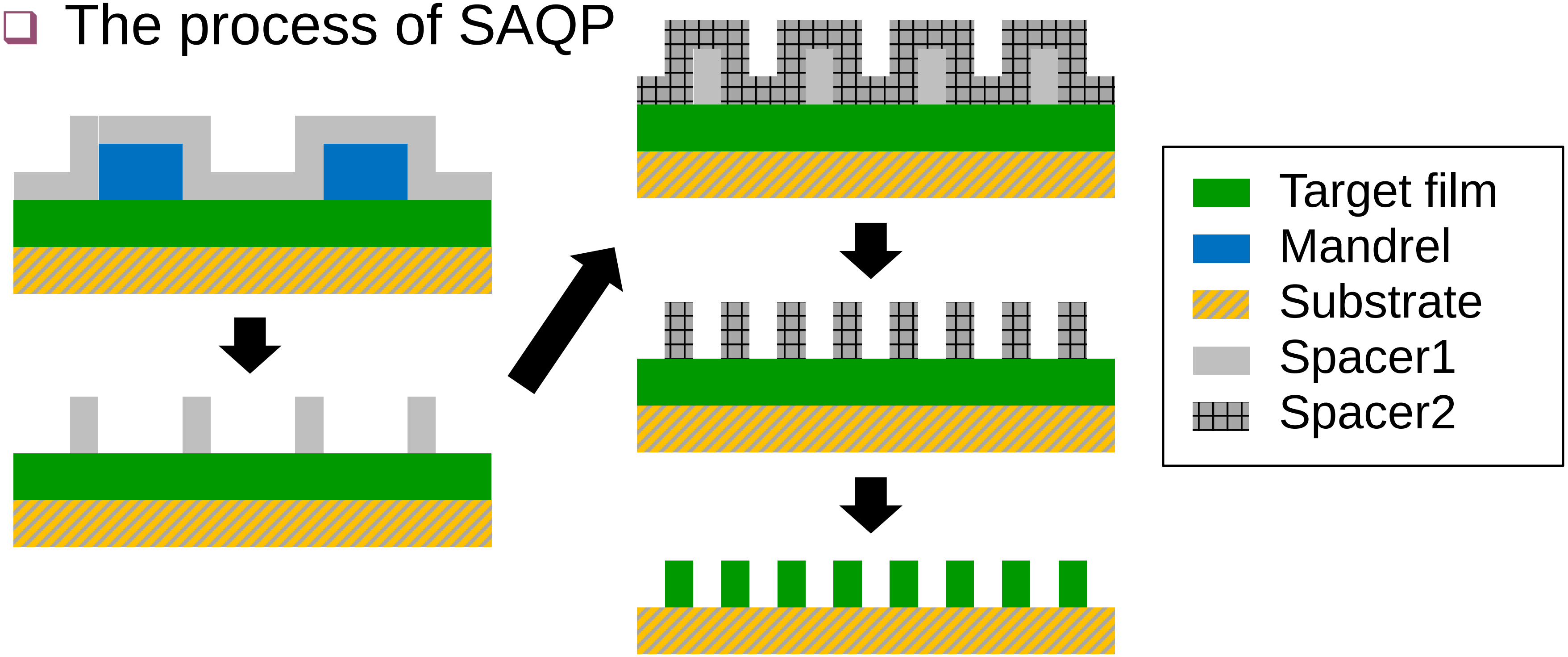
- Self-aligned multiple patterning (SAMP) has become a leading candidate of multiple patterning lithography
  - The intrinsic self-aligning property makes SAMP immune from the overlay error among multiple masks

- The process of self-aligned double patterning (SADP)



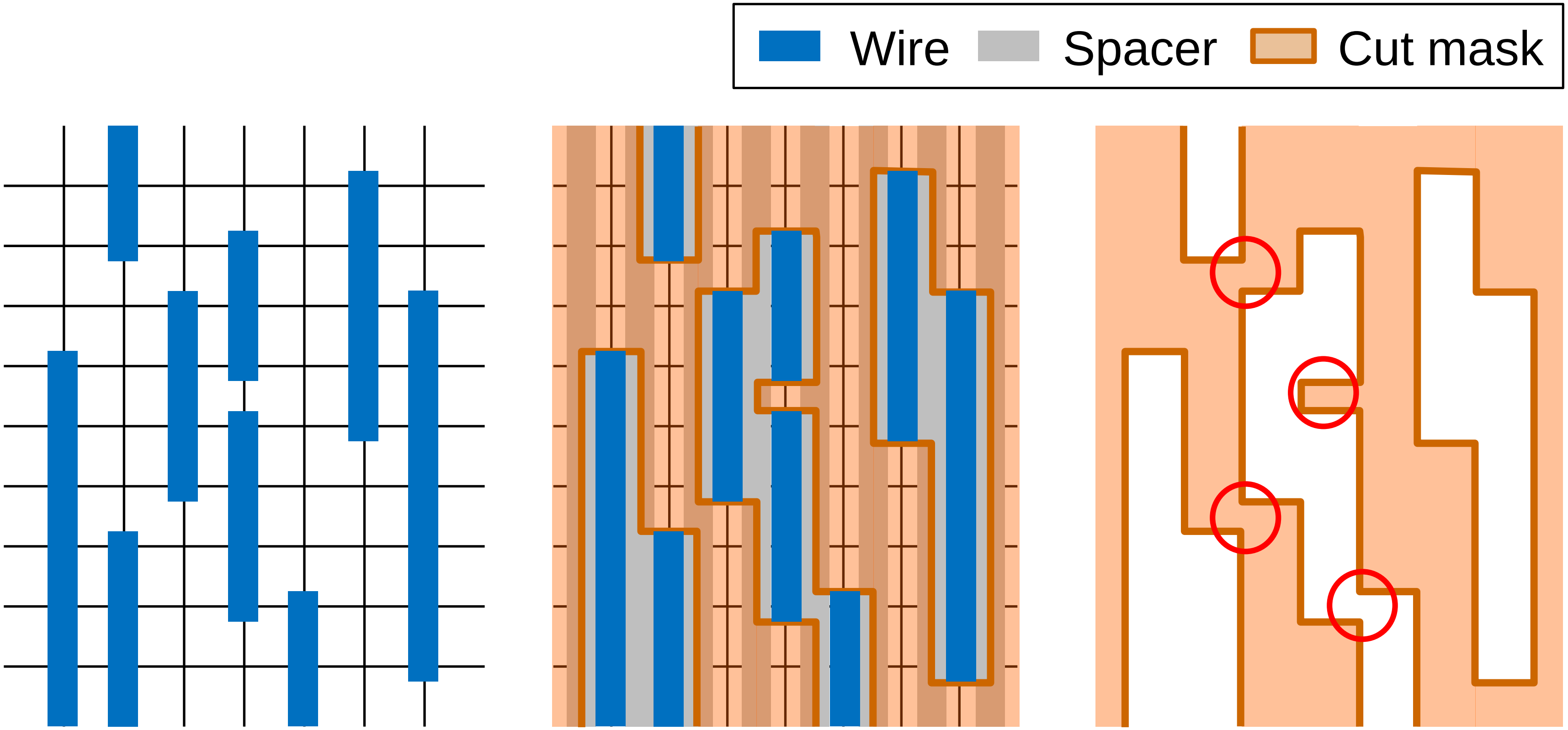
Self-Aligned Multiple Patterning (cont’d)

- Double patterning will not be sufficient for sub-10nm technology nodes
- Self-aligned quadruple patterning (SAQP) or even self-aligned octuple patterning (SAOP) will be required
- The process of SAQP



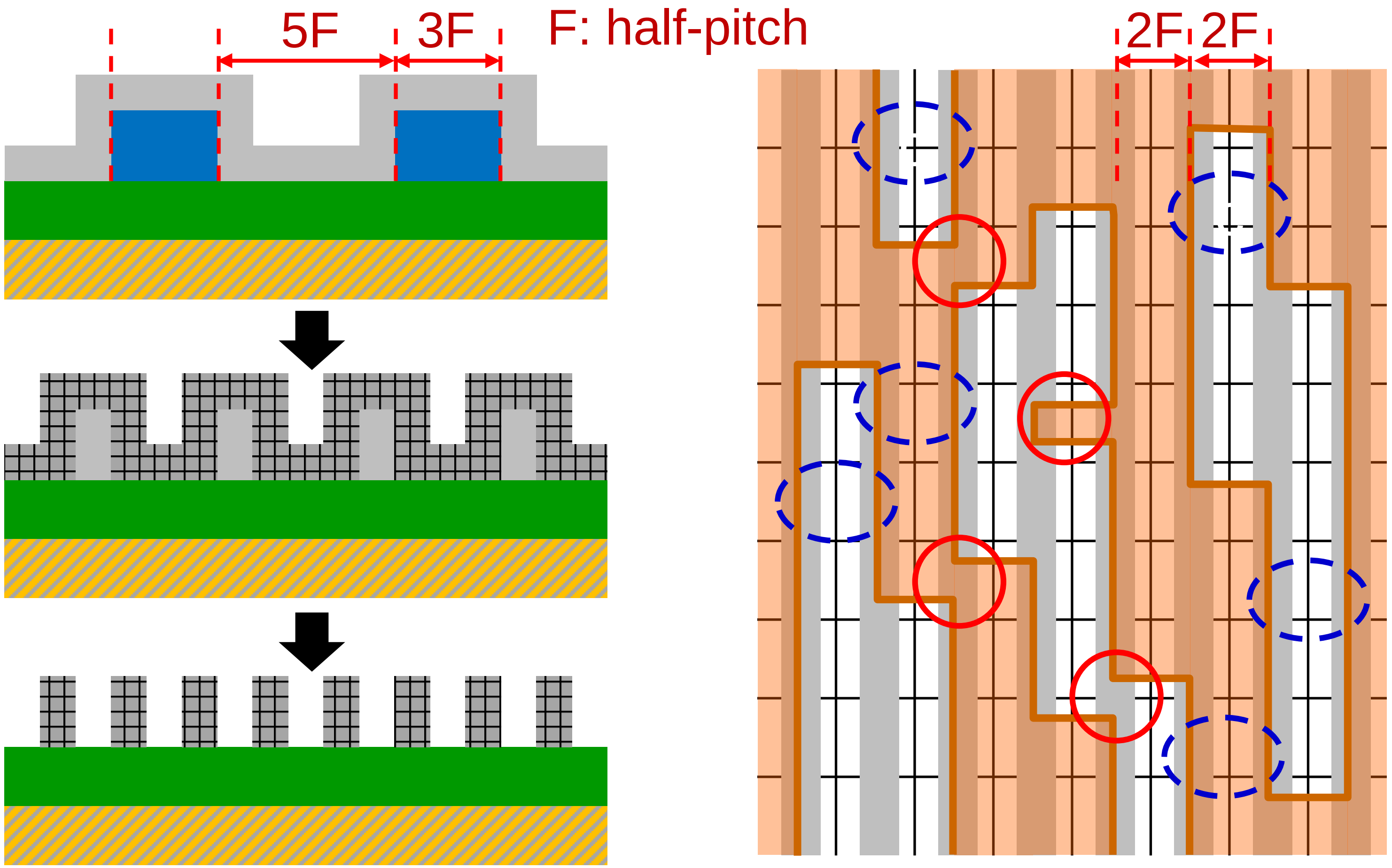
1-D Grid-based Layout Fabrication

- One-dimensional (1-D) grid-based layout structure will be adopted in sub-10 nm nodes
- To fabricate 1-D wire structure, a cut mask is required



Hotspots on Cut Masks

- For more advanced technology nodes where SAQP or SAOP is adopted, designing cut masks becomes much more difficult



Cut Mask-aware Routing for SAMP

- Several existing SADP or SAQP routers, where cut mask manufacturability is either not considered or considered only for SADP
  - Mirsaeedi et al., SPIE'11
  - Gau and Pan, ISPD'12
  - Kodama et al., ASPDAC'13
  - Du et al., DAC'13
  - Nakajima et al., SPIE'14
  - Lie et al., DAC'14
- We propose the ***first work*** of cut mask-aware full-chip routing for general SAMP processes

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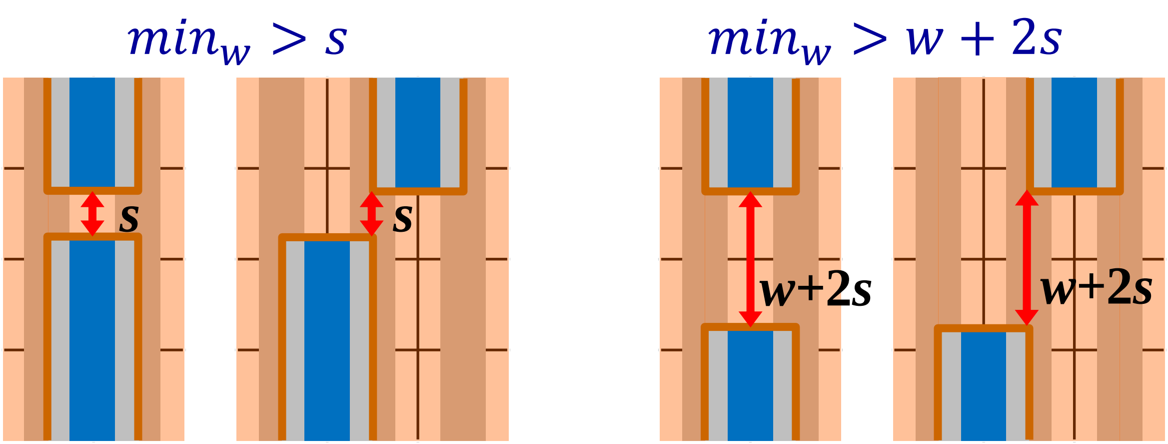
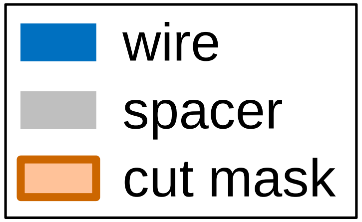
Cut Mask-aware Routing Rules

- Infeasible wire configurations are identified for cut mask manufacturability
  - The minimum width rule (min_w) of cut masks
  - The minimum spacing rule (min_s) of cut masks
- Cut mask violations against the minimum cut width rule are categorized according to violation directions:
  - Parallel width violations



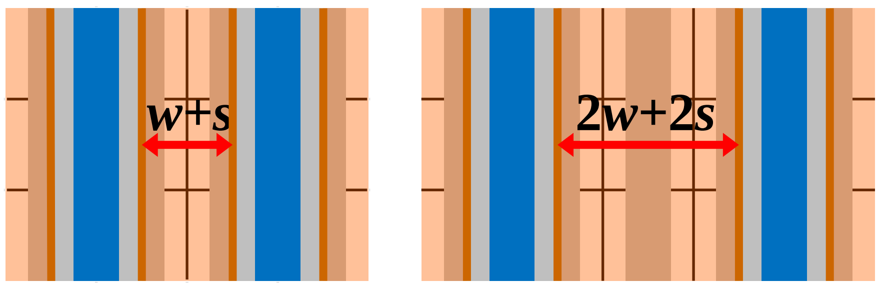
w: wire width
s: wire spacing



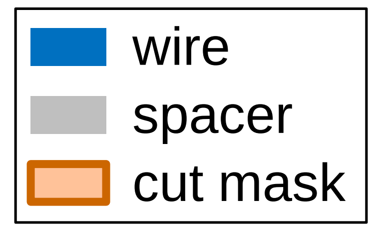
Cut Mask-aware Routing Rules (cont'd)

- Cut mask violations against the minimum cut width rule
  - Perpendicular width violations

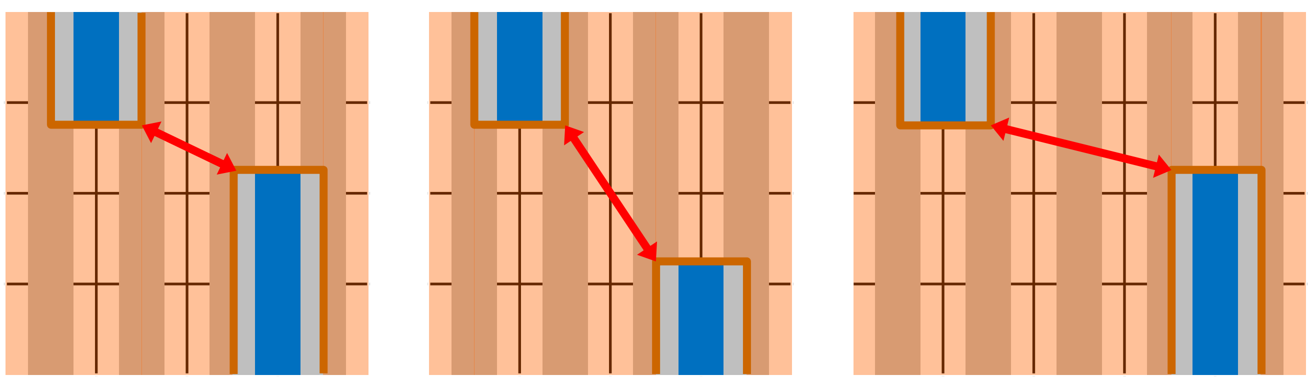
$min_w > w + s$ $\quad$ $min_w > 2w + 2s$



w: wire width
s: wire spacing



  - Diagonal width violations



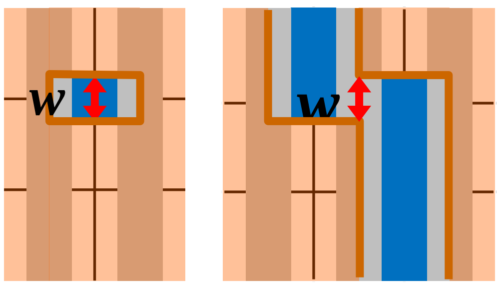
$\sqrt{(\boldsymbol{w}+\boldsymbol{s})^2+\boldsymbol{s}^2}$ $\quad$ $\sqrt{(\boldsymbol{w}+\boldsymbol{s})^2+(\boldsymbol{w}+2\boldsymbol{s})^2}$ $\quad$ $\sqrt{(2\boldsymbol{w}+2\boldsymbol{s})^2+\boldsymbol{s}^2}$

Cut Mask-aware Routing Rules (cont'd)

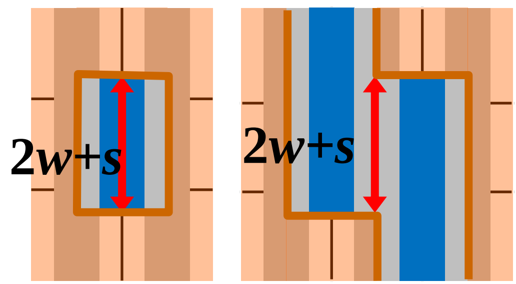
- Cut mask violations against the minimum cut spacing rule are similarly categorized

Parallel spacing violations

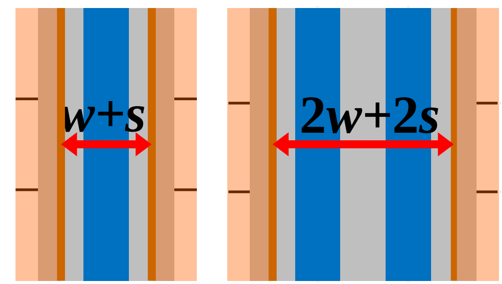
$min_s > w$



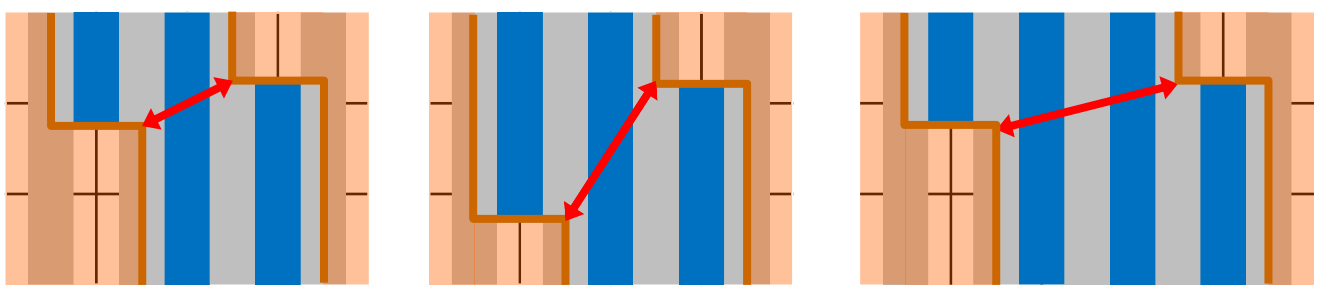
$min_s > 2w + s$



Perpendicular spacing violations



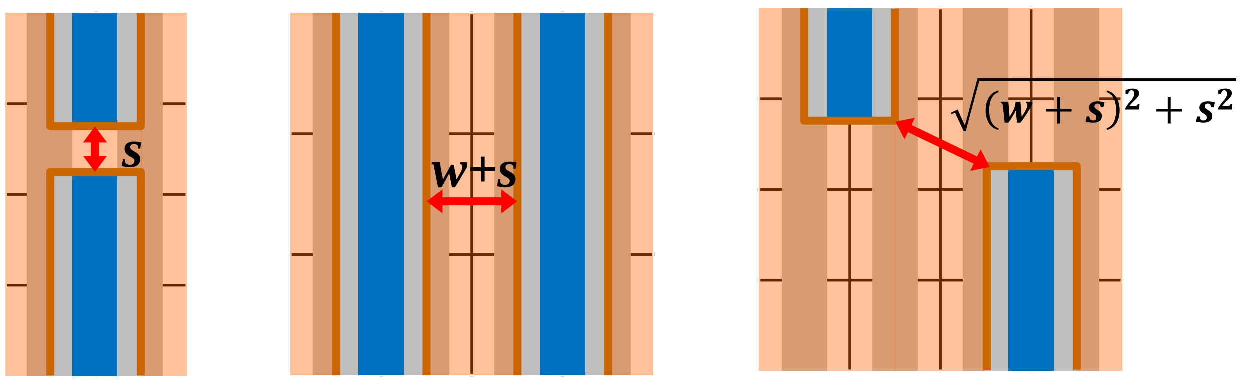
Diagonal spacing violations



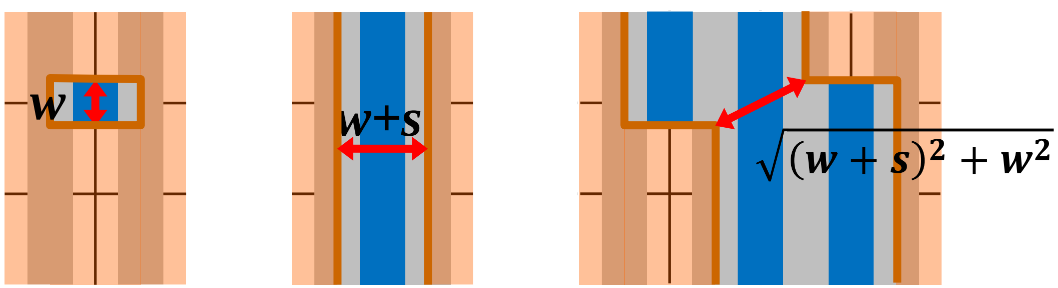
$\sqrt{(\boldsymbol{w}+\boldsymbol{s})^2+\boldsymbol{w}^2}$ $\sqrt{(\boldsymbol{w}+\boldsymbol{s})^2+(2\boldsymbol{w}+\boldsymbol{s})^2}$ $\sqrt{(2\boldsymbol{w}+2\boldsymbol{s})^2+\boldsymbol{w}^2}$

Infeasible Wire Configurations

- we assume that min_w and $min_s \in (2.5F, 3.0F)$
- Infeasible wire configurations considered in this work:
  - Cut width violations



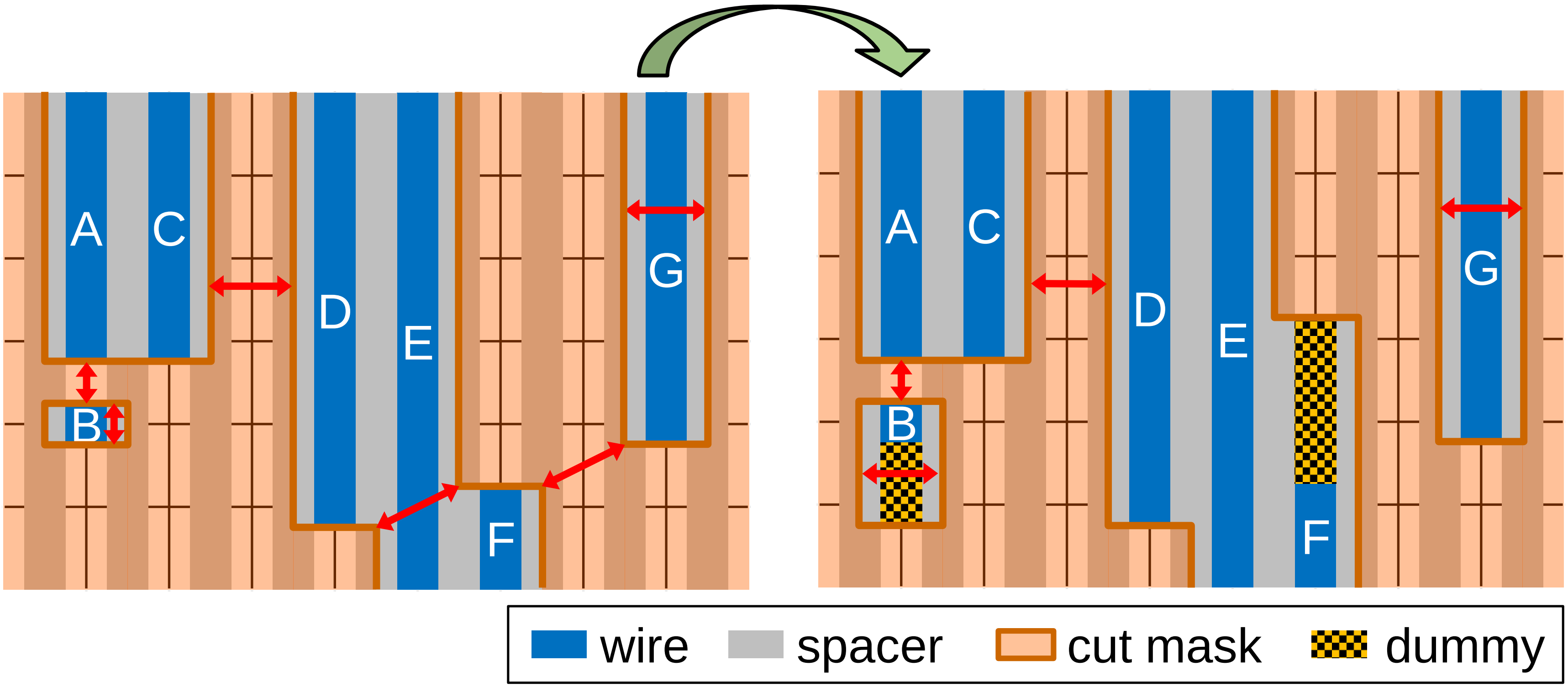
  - Cut spacing violations



Post Layout Modification

- Cut mask violations might not be avoided during full-chip routing in SAMP
- Post-layout modification techniques can be applied

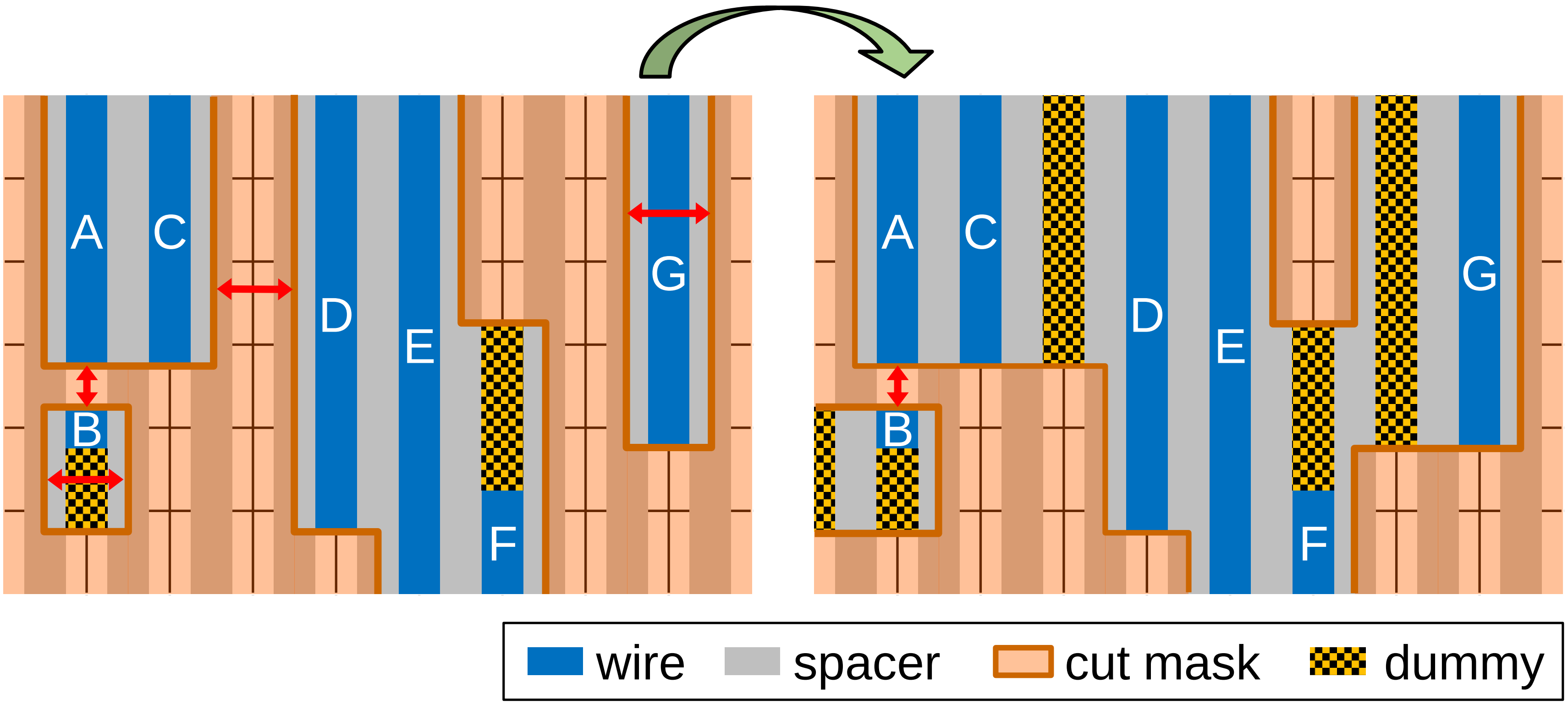
Technique 1 ***Wire extension***



Post Layout Modification (cont'd)

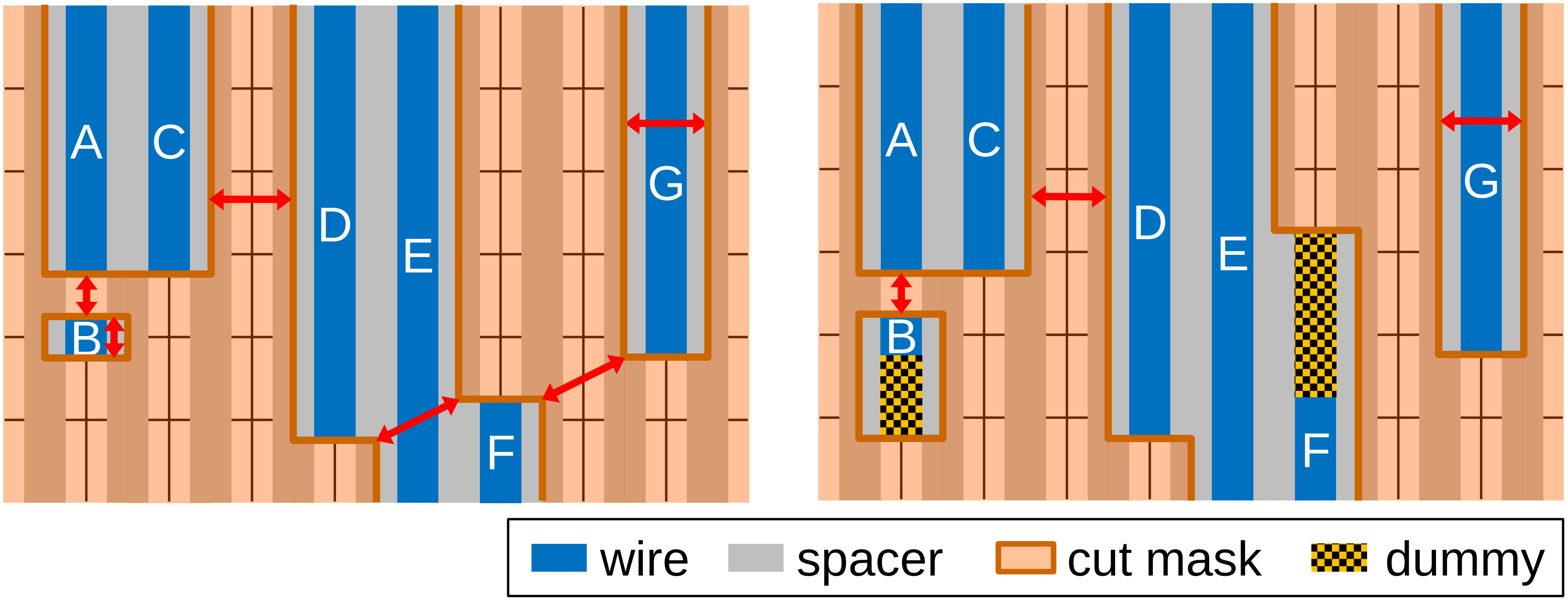
- Post-layout modification techniques can be applied

  Technique 2 ***Dummy wire insertion***



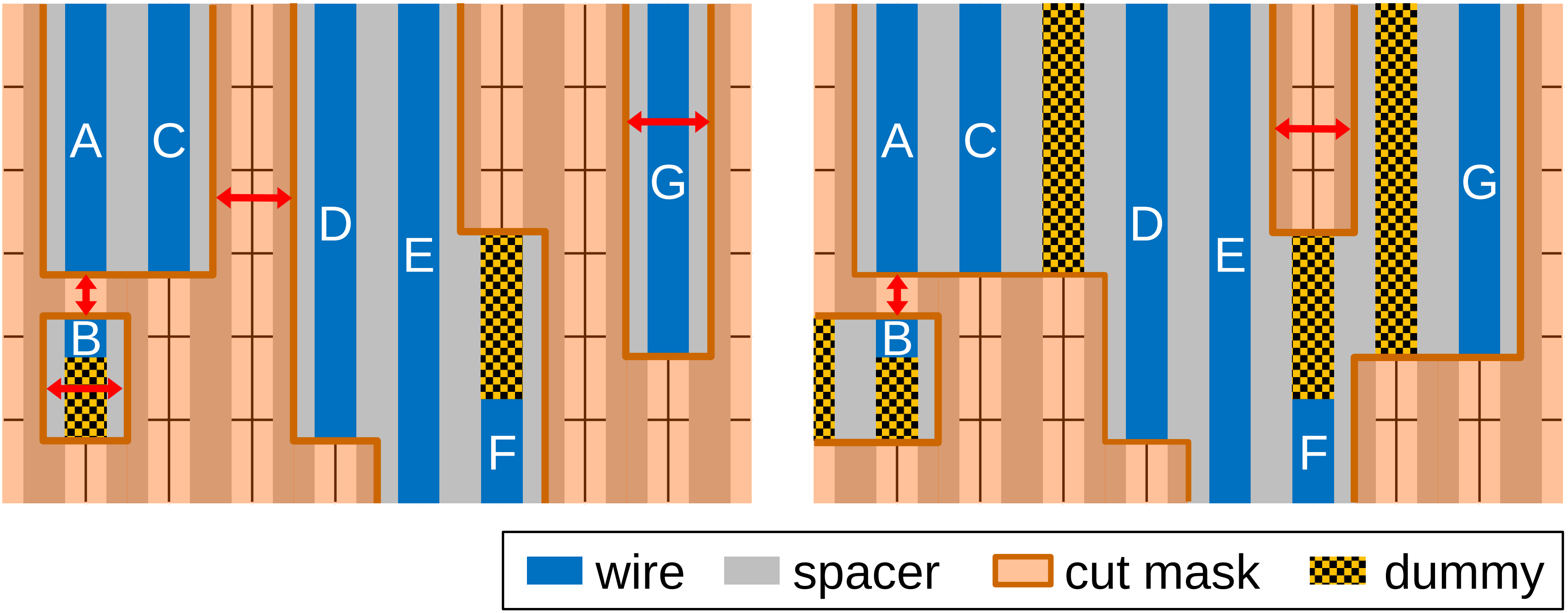
Issues of Post-Layout Modification

- Parallel width violations caused by close line ends on the same track cannot be solved
- Parallel spacing violations and diagonal violations may be eliminated by slightly extending line ends



Issues of Post-Layout Modification (cont'd)

- A perpendicular violation can only be resolved by inserting a dummy wire of the same length as ***a single track segment*** or ***a single wire segment***
- Extended wire segments and inserted dummy wires may cause additional mask violations



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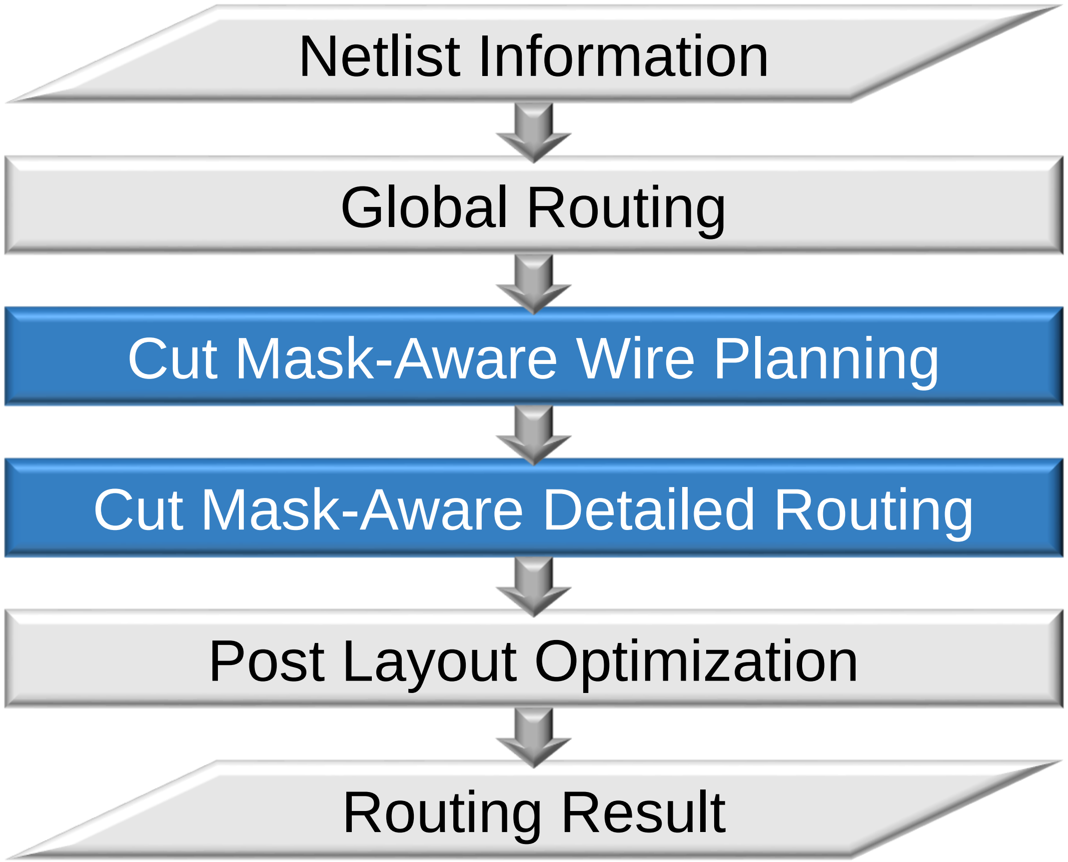
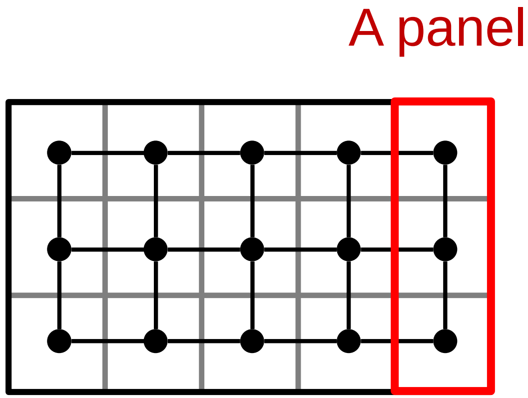
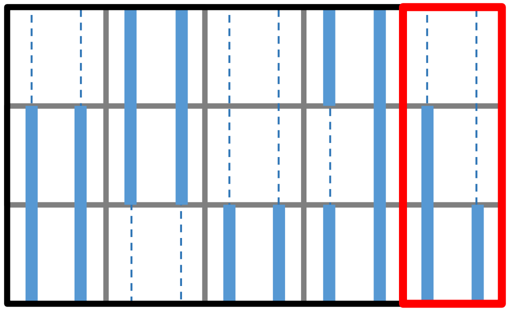
SAMP Full-Chip Routing Flow



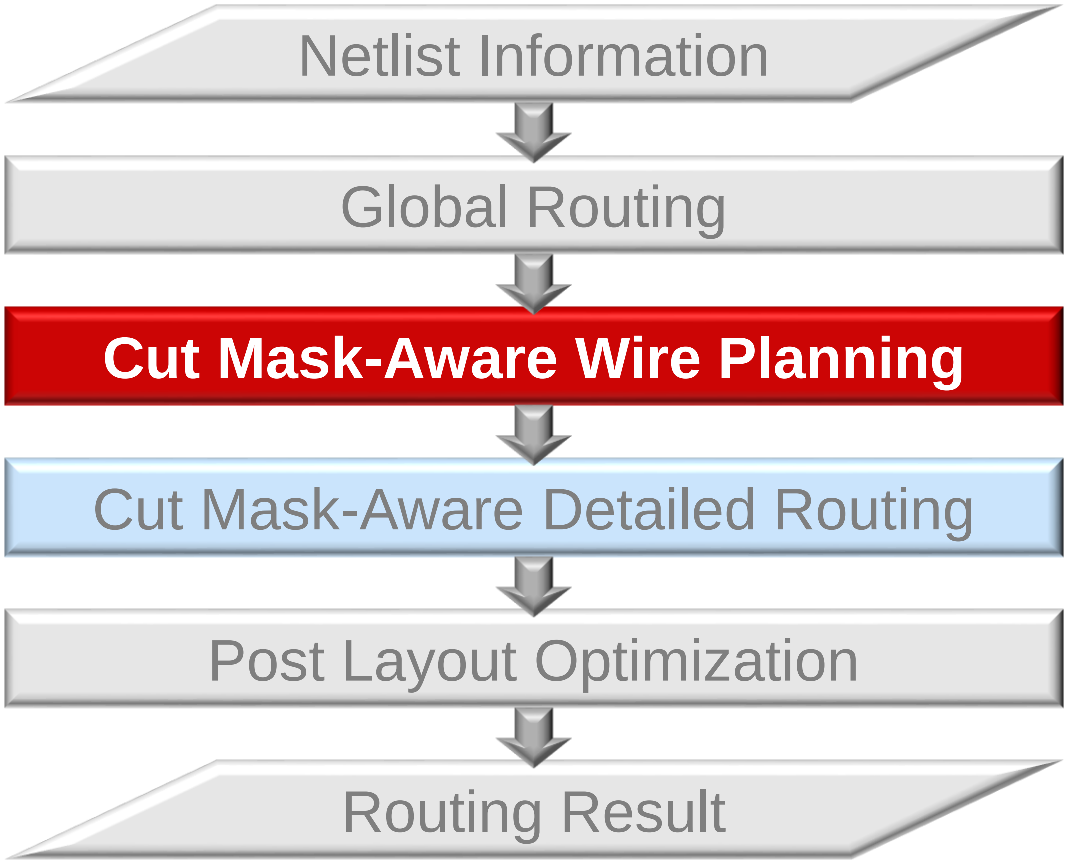


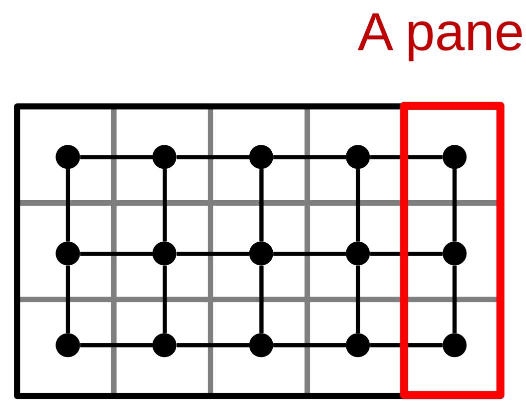
Global routing graph



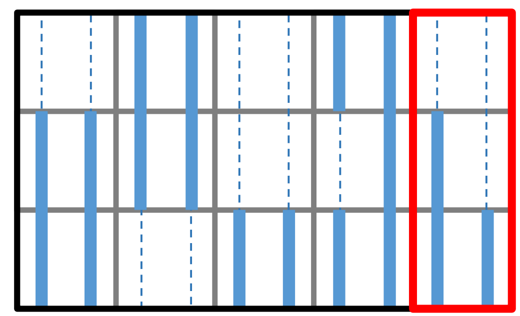
Wire planning

SAMP Full-Chip Routing Flow





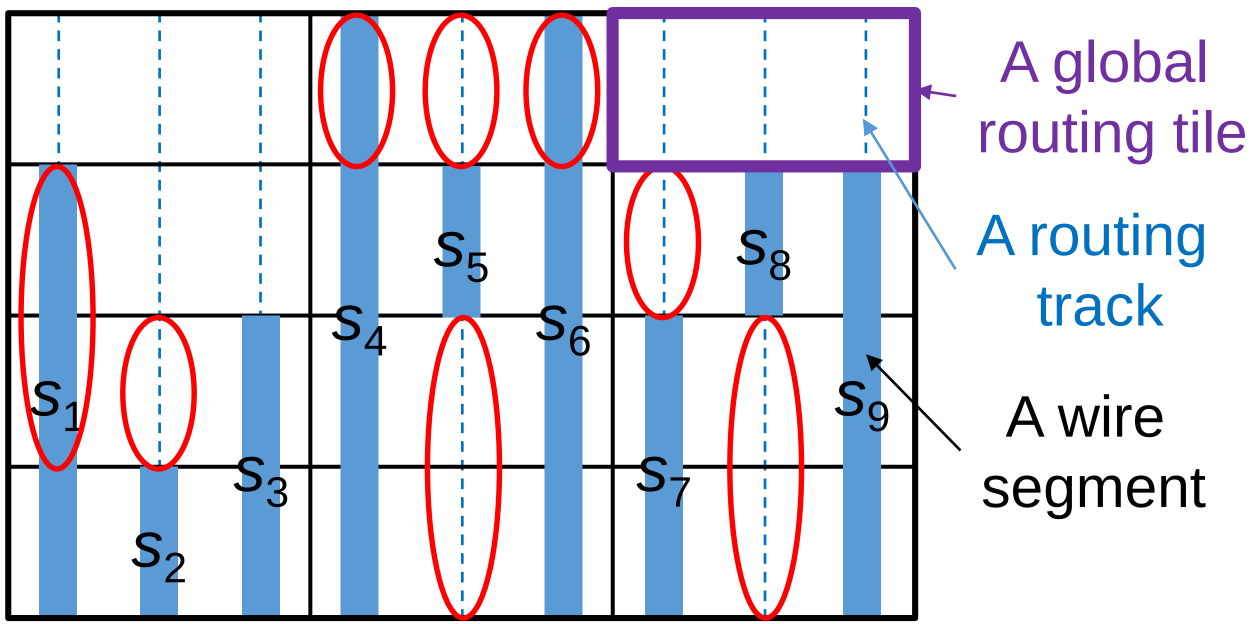
Global routing graph



Wire planning

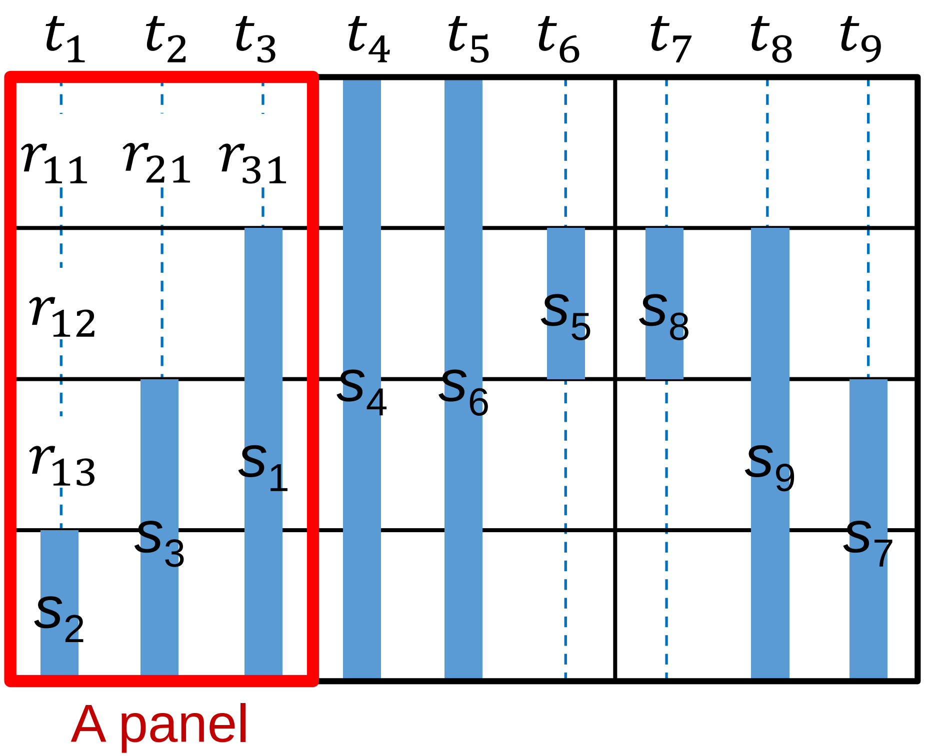
Track Routing w/o SAMP Consideration

- Track routing places the major trunks of each net on specific routing tracks
- If wire segments are assigned to tracks in an arbitrary order, many single track/wire segments will be generated



ILP Notations

- $\boldsymbol{s_i}$: the i-th wire segment.
- $\boldsymbol{t_j}$: the j-th track.
- $\boldsymbol{r_{jk}}$: the k-th interval of track t_j
- $\boldsymbol{x_{ij}}$: 0/1 variable. $x_{ij} = 1$ if segment s_i is assigned to track t_j
- $\boldsymbol{y_{jk}}$: 0/1 variable. $y_{jk} = 1$ if interval r_{jk} is occupied by some segment
- $\boldsymbol{tl_i}$: the leftmost track of the panel segment s_i belongs to
- $\boldsymbol{tr_i}$: The rightmost track of the panel segment s_i belongs to



ILP-based Wire Planning

- Objective:

$$minimize \sum st_{jk} + \sum sw_{jk}$$

  - $\boldsymbol{st_{jk}}$: 0/1 variable. $st_{jk} = 1$ if interval r_{jk} is a single track segment
  - $\boldsymbol{sw_{jk}}$: 0/1 variable. $sw_{jk} = 1$ if interval r_{jk} is a single wire segment
  - ***Minimize the total length of single track and wire segments***
- Subject to
  - Each wire segment is exactly assigned to one specific track in the panel it belongs to

$$\sum x_{ij} = 1, \forall s_i$$

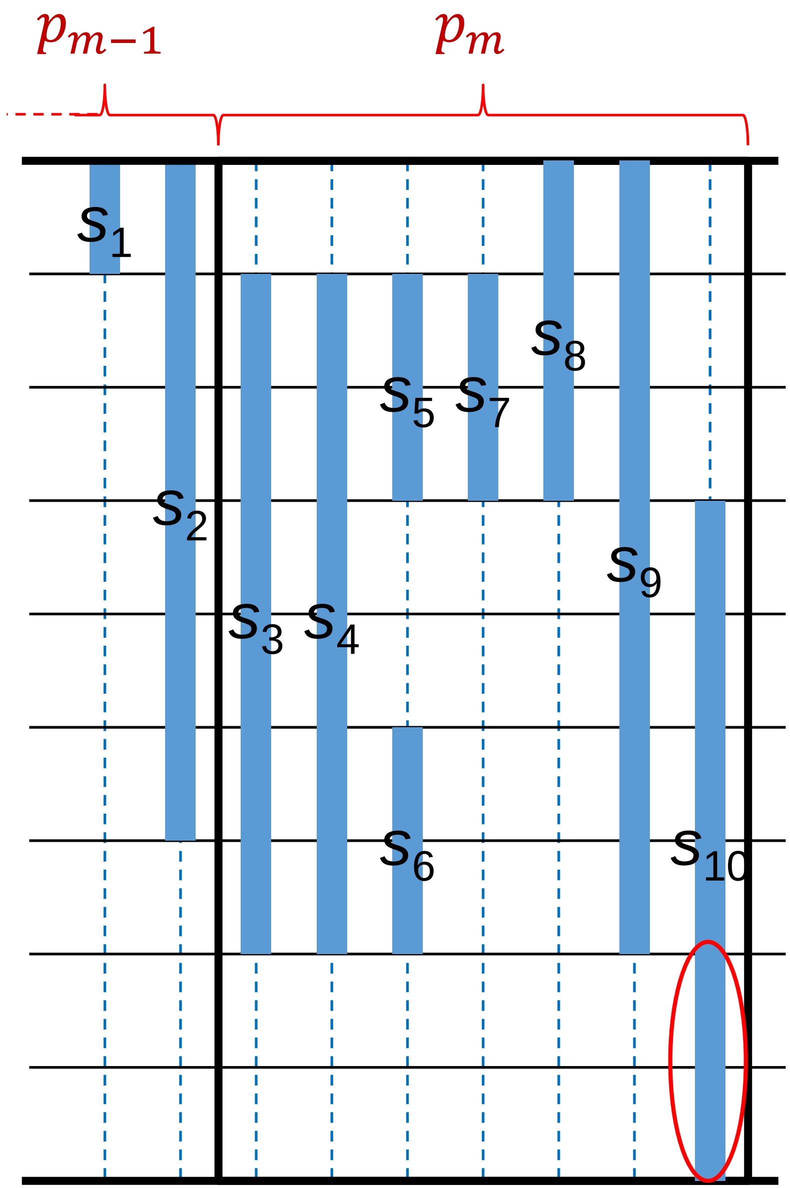
$$x_{ij} = 0, \forall s_i, \forall t_j \notin [tl_i, tr_i]$$

ILP-based Wire Planning (cont'd)

- Subject to
  - Two conflicting segments will not be assigned to the same track
    $$x_{aj} + x_{bj} \leq 1, \forall s_a \; and \; s_b \; are \; conflicting$$
  - Determine whether a track interval r_{jk} is empty ($y_{jk} = 0$) or occupied by some wire segment ($y_{jk} = 1$)
    $$\sum_{s_i \in S_k} x_{ij} = y_{jk}, \forall r_{jk}$$
  - Inspect whether a track interval r_{jk} becomes a single track ($st_{jk} = 1$)/wire ($sw_{jk} = 1$) segment or not
    $$-y_{jk} + y_{(j-1)k} + y_{(j+1)k} - 1 \leq st_{jk}, \forall r_{jk}$$
    $$y_{jk} - y_{(j-1)k} - y_{(j+1)k} \leq sw_{jk}, \forall r_{jk}$$

ILP Reduction

- ***Panel-based wire planning***
  - Solve the wire planning problem for one panel at a time
  - Sequentially perform track routing on panels from left to right
  - Use the first segment in p_m to optimize the last segment in p_{m-1}
  - Put the segment that can not be optimized in p_m to the last track



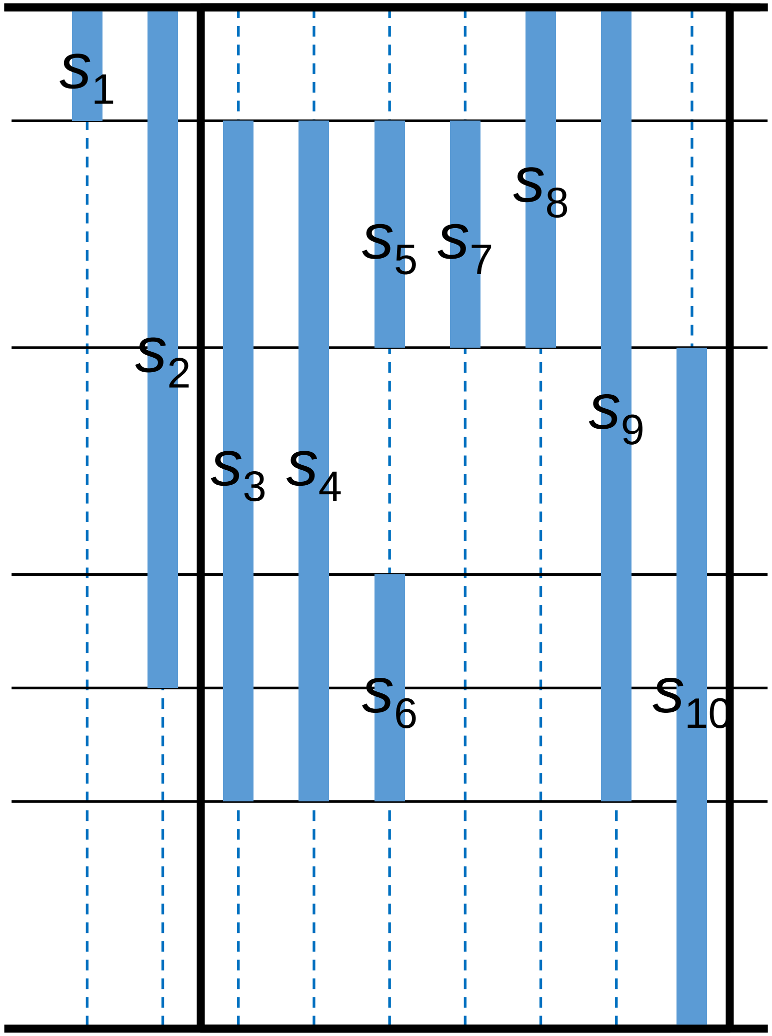
ILP Reduction (cont'd)

- ***Line end-based interval reduction***
  - Tracks are divided into intervals according to the line ends of wire segments
  - Since the lengths of intervals are various now, the objective function needs to be modified:

$$minimize$$

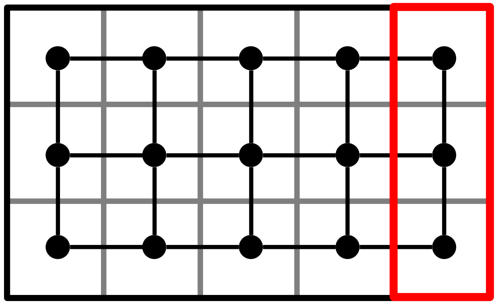
$$\sum c_{jk} \cdot st_{jk} + \sum c_{jk} \cdot sw_{jk}$$

    - c_{jk}: #global tiles r_{jk} contains

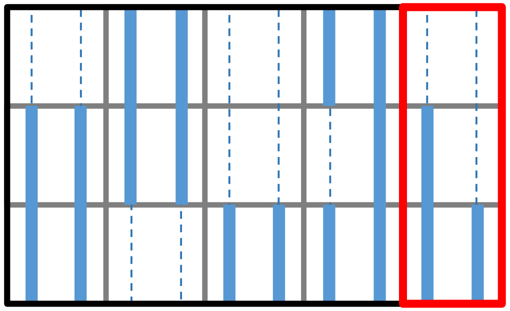


SAMP Full-Chip Routing Flow

A panel



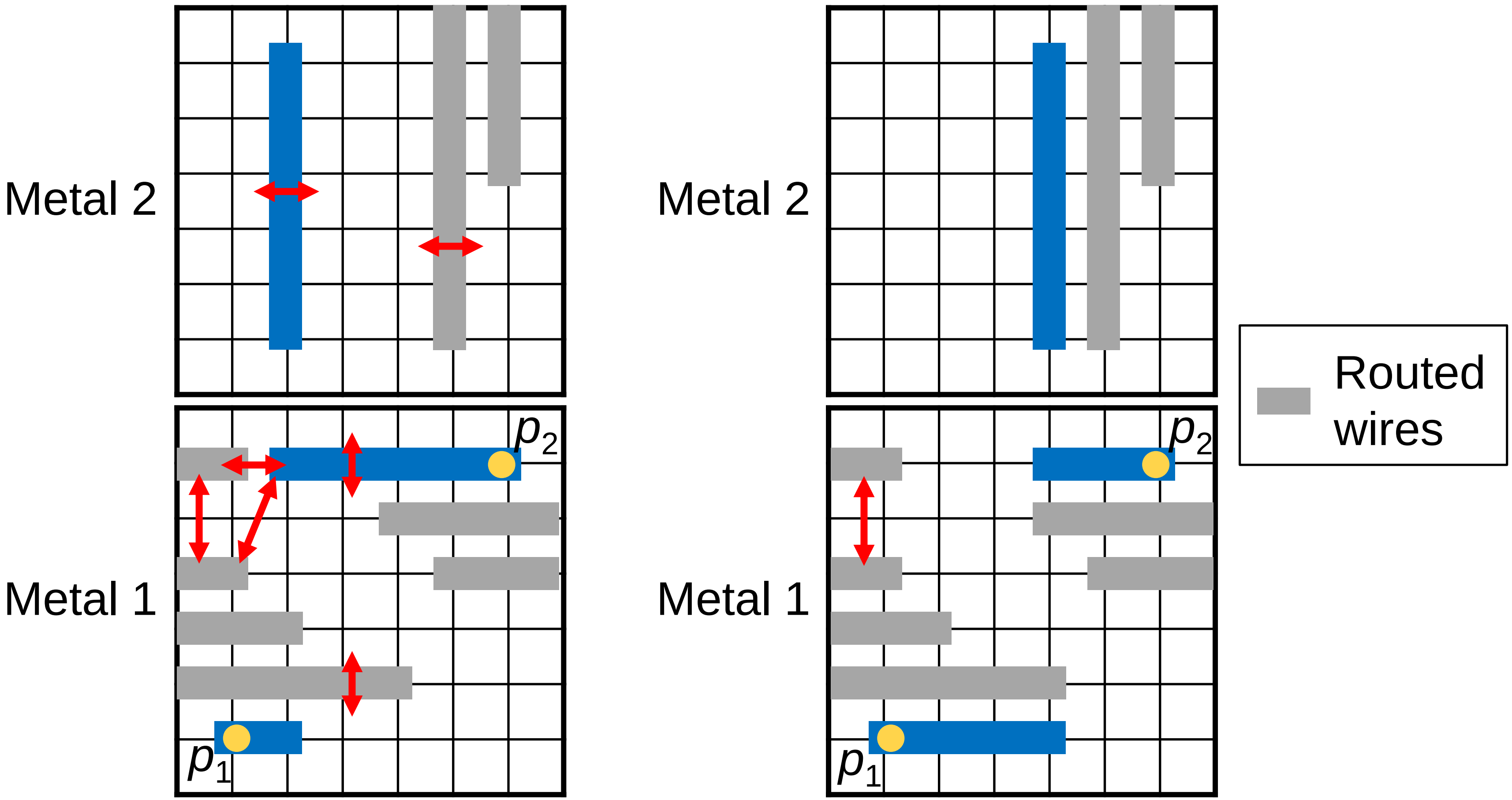
Global routing graph



Wire planning

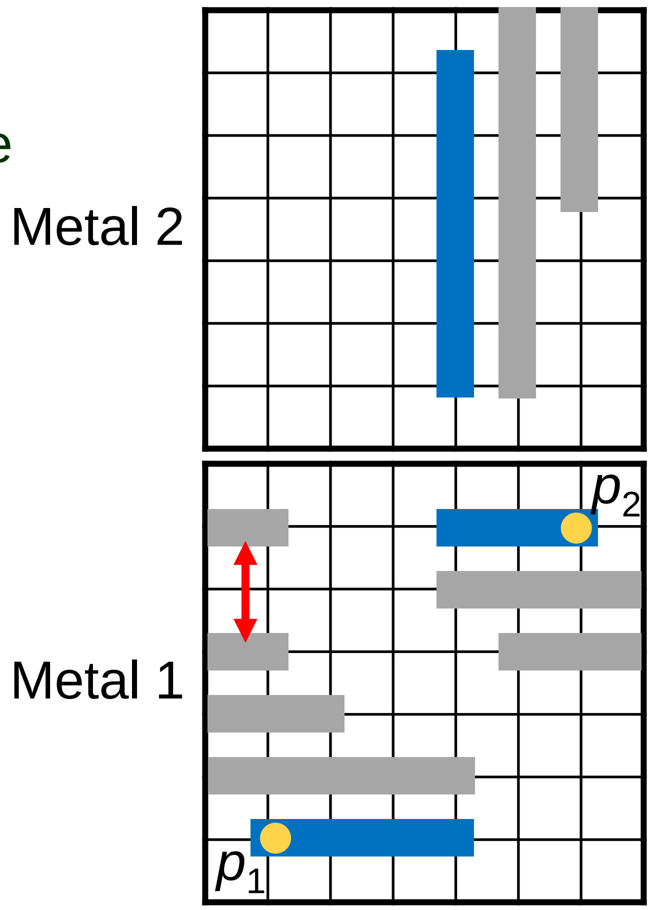
Cut Mask-aware Detailed Routing

- Cut mask-aware detailed routing may
  - Avoid generating additional mask violations
  - Fix some violations on already routed wires



Cut Mask-aware Detailed Routing Principles

- We have the following principles as detailed routing a wire:
  - For parallel mask violations
    - Avoid too close line ends on the same track and too short wire segments
  - For diagonal mask violations
    - Avoid close opposite line ends and overlapping line ends on nearby but not adjacent tracks
  - For perpendicular mask violations
    - Avoid single track/wire segments
    - Encourage wires to eliminate single track/wire segments during routing



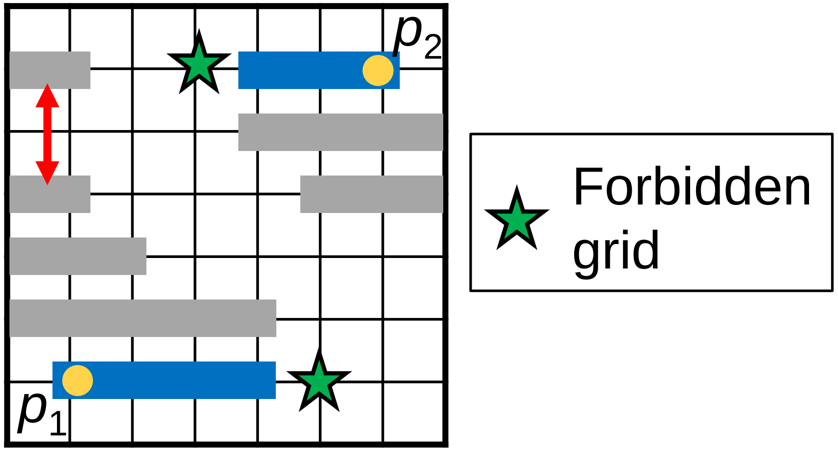
Cut Mask-aware Detailed Routing Cost

- Based on the routing principles, the cost of routing on a grid g_j from a grid g_i is defined as follows:

$$Cost(j) = Cost(i) + W_{ij} + \alpha \times Inc(j) - \beta \times Dec(j)$$

  - W_{ij}: the wiring cost from g_i to g_j
  - $Inc(j)$: # generated mask violations due to routing on g_j
  - $Dec(j)$: # eliminated mask violations due to routing on g_j

- Forbidden points are inserted next to the line ends of a routed path to avoid parallel width violations



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Experimental Setup

- Platform
  - C++ programming language
  - 2.0 GHz Linux workstation with 56 GB memory
- Benchmark
  - 5 dense circuits from the MCNC benchmark
  - $w = s = 18\ nm$
  - $min_w = min_s = 50\ nm$
  - $\alpha = \beta = 0.5$
- Comparison
  - A conventional routability-driven baseline router

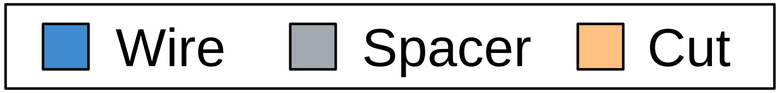
Experimental Results

- Compared to the baseline router, our SAMP full-chip router
  - Reduce mask violations by 64%
  - Reduce the use of dummy wires by 36%
  - Reduce routability by 0.1%
  - Increase wirelength by 2%

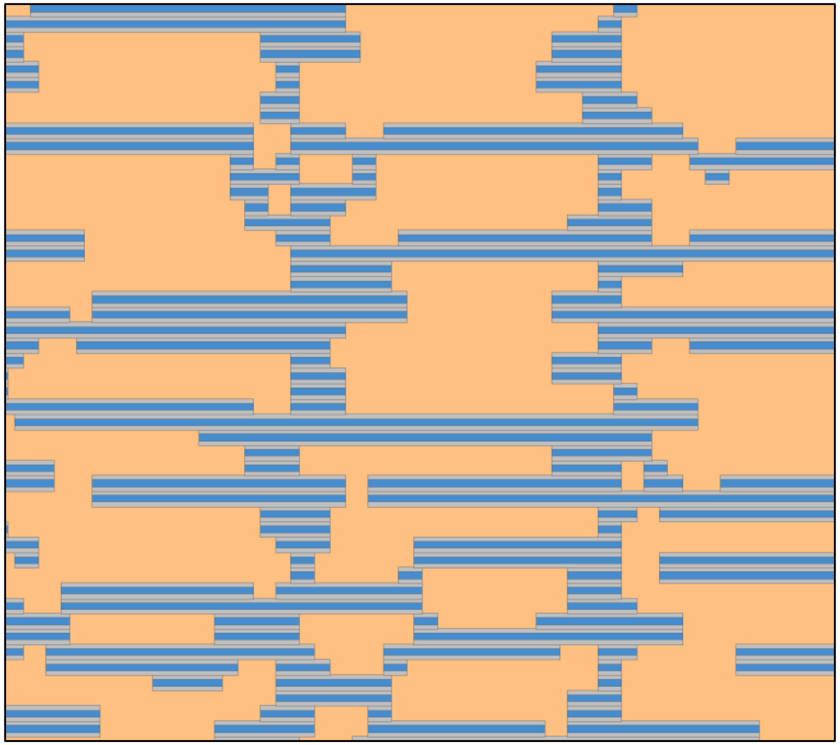
Circuit	Baseline Router					Our SAMP Router				
	Rout.	WL	Vio.	Dum.	CPU (s)	Rout.	WL	Vio.	Dum.	CPU (s)
S5378	100%	3744	91	2185	5	99.9%	3799	32	1438	22
S9234	100%	2766	67	1682	4	99.9%	2816	19	1173	15
S13207	100%	8975	167	5086	10	99.9%	9139	60	3196	78
S15850	100%	11089	212	6559	14	99.9%	11298	82	3803	79
S38417	99.9%	24188	486	14158	30	99.9%	24890	161	9348	625
S38584	100%	33776	717	19953	57	99.9%	34576	244	12351	687
Avg.	1.00	1.00	1.00	1.00	1.00	0.999	1.02	**0.34**	**0.64**	9.08

Vio.: the mask violations after applying post-layout optimization
Dum.: the dummy wires used for post-layout optimization

Optimized Routing Result



A routing result of the baseline router



A routing result of our SAMP router with post-layout optimization

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Conclusions

- This paper proposes the first work of cut mask optimization for SAMP during full-chip routing
- The cut mask rules and the corresponding routing rules are identified to guide the router
- An ILP-based wire planning approach and cut mask-aware detailed routing are proposed
- Experimental results have shown that our flow can generate routing results that optimize cut masks