Highlights

Opening and Keynote I

Tuesday, January 20, 2015, 8:30-9:50

Udo Wolz (Executive Vice President and Director for Engineering and Innovation, Bosch Corporation) “The required technologies for Automotive towards 2020”

Keynote II

Wednesday, January 21, 2015, 9:00-9:50

Atsushi Takahara (Director of NTT Network Innovation Laboratories) “Programmable Network”

Keynote III

Thursday, January 22, 2015, 9:00-9:50

Noriko Arai (Professor of Information and Society Research Division, National Institute of Informatics) “When and how will an AI be smart enough to design?”

Special Sessions

1S: (Presentation + Poster Discussion) University Design Contest

Tuesday, January 20, 2015, 10:20-13:40

2S: (Invited Talks) Internet of Things

Tuesday, January 20, 2015, 13:50-15:30

3S: (Invited Talks) New Challenges and Solutions in Nanometer Physical Design

Tuesday, January 20, 2015, 15:50-17:30

4S: (Invited Talks) Machine Learning in EDA: Promises and Challenges in Selected Applications

Wednesday, January 21, 2015, 10:15-12:20

5S: (Invited Talks) The Future of Emerging ReRAM Technology

Thursday, January 22, 2015, 10:15-12:20

9B: (Invited Talks) System-Level Designs and Tools for Multicore Systems

Thursday, January 22, 2015, 15:50-17:30

Designers’ Forum

5S: (Oral Session) Car Electronics

Wednesday, January 21, 2015, 13:50-15:30

6S: (Panel Discussion) Challenges in the Era of Big-Data Computing

Wednesday, January 21, 2015, 15:50-17:30

8S: (Oral Session) Technology Trend toward 8K Era

Thursday, January 22, 2015, 13:50-15:30

9S: (Panel Discussion) IP base SoC design and IP design innovation

Thursday, January 22, 2015, 15:50-17:30

Tutorials

ASP-DAC 2015 offers attendees a set of two-hour intense introductions to specific topics. Each tutorial will be presented twice a day to allow attendees to cover multiple topics. If you register for tutorials, you have the option to select three out of the six topics.

Tutorial-1: Ultra-low power ultra-low voltage design techniques in Fully Depleted SOI technologies

Monday, January 19, 2015, 9:30-11:30, 13:00-15:00

Organizer: Andreia Cathelin (STMicroelectronics)

Speakers: Giorgio Cesana (STMicroelectronics), Edith Beigné (CEA-Leti), Nobuyuki Sugii (LEAP)

Tutorial-2: Leading-Edge Lithography and TCAD

Monday, January 19, 2015, 9:30-11:30, 13:00-15:00

Organizer: Shigeki Nojima (Toshiba)

Speakers: Seiji Nagahara (Tokyo Electron), Tomoyuki Matsuyama (Nikon), Shigyo Naoyuki (Toshiba)


Monday, January 19, 2015, 9:30-11:30, 15:30-17:30

Organizers: Hiroshi Nakamura (The University of Tokyo), Takashi Nakada (The University of Tokyo)

Speakers: Takashi Nakada (The University of Tokyo), Shinobu Fujita (Toshiba Corporate R&D Center)

Tutorial-4: Hardware Trust in VLSI Design and Implementations

Monday, January 19, 2015, 9:30-11:30, 15:30-17:30

Organizers: Kazuo Sakiyama (The University of Electro-Communications), Makoto Nagata (Kobe University)

Speakers: Patrick Schaumont (Virginia Tech, US), Swarup Bhunia (Case Western Reserve University, US), Kazuo Sakiyama (The University of Electro-Communications, JP), Makoto Nagata (Kobe University, JP)

Tutorial-5: High-Level Synthesis for FPGAs: From Software to Programmable Hardware

Monday, January 19, 2015, 13:00-15:00, 15:30-17:30

Organizer: Jason Anderson (University of Toronto)

Speakers: Jason Anderson (University of Toronto), Ben Carrion Schafer (Hong Kong Polytechnic University)

Tutorial-6: Electronic Design Automation for Nanotechnologies

Monday, January 19, 2015, 13:00-15:00, 15:30-17:30

Organizers: Pierre-Emmanuel Gaillardon (EPFL), Giovanni De Micheli (EPFL)

Speakers: Pierre-Emmanuel Gaillardon (EPFL), Luca Amaru (EPFL), Anupam Chattopadhay (Nanyang Technical University), Subhasish Mitra (Stanford University)
ASP-DAC 2015 offers attendees a set of two-hour intense introductions to specific topics. Each tutorial will be presented twice a day to allow attendees to cover multiple topics. If you register for tutorials, you have the option to select three out of the six topics.

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<td>20th Anniversary Reception (18:00 - 19:30)</td>
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(All participants are welcome.)
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<tr>
<th>Time</th>
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<tr>
<td>08:30</td>
<td>Opening</td>
<td>Kunio Uchiyama (Hitachi)</td>
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<td>09:40</td>
<td>Main Talk</td>
<td>Udo Wol (Bosch, Japan)</td>
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<td>10:20</td>
<td>1A: NoC I Performance and Fault Tolerance</td>
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<td>1B: Toward Power Efficient Design</td>
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<td>1C: Modeling and Design Methodologies of Post-silicon Devices</td>
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<td>14:00</td>
<td>University LSI Design Contest Poster Presentation</td>
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**Session 1A: NoC I Performance and Fault Tolerance**

- **Chair:** Hiroyuki Ito (Tokyo Inst. of Tech., Japan)
- **Noriyuki Miura (Kobe Univ., Japan)**
- **Yoshinori Takeuchi (Osaka Univ., Japan)
- **Kimiyoshi Usami (Shibaura Inst. of Tech., Japan)
- **Masanori Hashimoto (Osaka Univ., Japan)**
- **Zili Shao (Hong Kong Polytechnic Univ., Hong Kong)
- **Duo Liu (Chongqing Univ., China)**

**Talks:**

- **1A-1:** Leibo Lin, Yu Ren, Chenchen Deng (Tsinghua Univ., China), Jianguo Wang (Tsinghua Univ., China), "The Required Technologies for Automotive towards 2020"
- **1A-2:** Peng Ning, Sheng Ma, Hongyi Lu, Zhiyong Wang, Chen Li (National Univ. of Defense Tech., China), "Adaptive Remaining Hop Count Flow Control: Consider the Interaction between Packets"
- **1A-3:** Takeshi Saga (Tohoku Univ., Japan), Tatsuhiko Kawasaki, Kyoko Takahashi, "Modeling and Design Methodologies of Post-silicon Devices"
- **1A-4:** Takanori Soga (ISIT Kyushu, JST CREST, Japan), Hiroshi Sasaki, Tomoya Hiro, "A Flexible Hardware Barrier Mechanism for Many-Core Processors"
- **1B-1:** Alireza Shafaei, Shuang Chen, Yanzhi Wang, Massoud Pedram (Univ. of Southern California, U.S.A.), "A Cross-Layer Framework for Designing and Optimizing Deeply-Scaled FinFET-Based SRAM Cells under Process Variations"
- **1B-2:** Adam Temam (EPFL, Switzerland), Davide Rossi (Univ. of Bologna, Italy), Pascal Meinerzhagen (EPFL, Switzerland), Luca Benini (Univ. of Bologna, Italy/ETH, Switzerland), Andreas Burg (EPFL, Switzerland), "Controlled Placement of Standard Cell Memory Arrays for High Density and Low Power in 28nm FD-SOI"
- **1B-3:** Jun Shiono, Tatsunobu Kitahara, "Quantitative Modeling of Racetrack Memory: A Tradeoff among Area, Performance, and Power"
- **1B-4:** Lian Zeng, Takahiro Watanabe (Waseda Univ., Japan), "A Performance Enhanced Dual-Switch Network-on-Chip Architecture"
- **1C-1:** Peng Gu, Boxun Li, Tianqi Tang (Tsinghua Univ., China), "Technological Exploration of RRAM Crossbar Array for Matrix-Vector Multiplication"
- **1C-2:** Yingchun Cong, Xiu Rong, "A Defect-Aware Approach for Mapping Reconfigurable Single-Electron Transistor Arrays to 3D ICs for Mapping, Recognition, and Control of Single-Electron Transistor Arrays"
1S-1: Dongsheng Yang, Wei Deng, Tomohiro Ueno, Teerachat Siriburanon, Satoshi Kondo, Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan) “An HDL-Synthesized Gated-Edge-Injection PLL with A Current Output DAC”

1S-2: Takehiko Amaki, Masanori Hashimoto, Takao Onoye (Osaka Univ./JST, CREST, Japan) “An Oscillator-Based True Random Number Generator with Process and Temperature Tolerance”

1S-3: Takanori Machida (Univ. of Electro-Communications, Japan), Dai Yamamoto (Fujitsu Labs., Japan), Mitsugu Iwamoto, Kazuo Sakiyama (Univ. of Electro-Communications, Japan) “Implementation of Double Arbitrer PUF and Its Performance Evaluation on FPGA”

1S-4: Yohei Umeki, Koji Yanagida (Kobe Univ., Japan), Shusuke Yoshimoto (Stanford Univ., U.S.A.), Shintaro Izumi, Masahiko Yoshimoto, Hiroshi Kawaguchi (Kobe Univ., Japan), Koji Tsunoda, Toshihiro Sugii (Low-Power Electronics Association and Project (LEAP), Japan) “A Negative-Resistance Sense Amplifier for Low-Voltage Operating STT-MRAM”

1S-5: Nobuaki Kobayashi, Ryusuke Ito, Tadayoshi Enomoto (Chuo Univ., Japan) “A High Stability, Low Supply Voltage and Low Standby Power Six-Transistor CMOS SRAM”

1S-6: Xuan-Thuan Nguyen, Cong-Kha Pham (Univ. of Electro-Communications, Japan) “An Efficient Multi-Port Memory Controller for Low-Power Applications”

1S-7: Masanori Hashimoto, Dawood Alnajjar, Hiroaki Konoura (Osaka Univ./JST, CREST, Japan), Yukio Mitsuyama (Kochi Univ. of Tech./JST, CREST, Japan), Hajime Shimada (Nagoya Univ./JST, CREST, Japan), Kazutoshi Kobayashi (Kyoto Inst. of Tech./JST, CREST, Japan), Hirokiyuki Kanbara (ASTEM/JST, CREST, Japan), Hiroki Ochi (Ritsumeikan Univ./JST, CREST, Japan), Takashi Imagawa (Kyoto Univ./JST, CREST, Japan), Kazutoshi Wakabayashi (NEC/JST, CREST, Japan), Takao Onoye (Osaka Univ./JST, CREST, Japan), Hitodoshi Onodera (Kyoto Univ./JST, CREST, Japan) “Reliability-Configurable Mixed-Grained Reconfigurable Array Compatible with High-Level Synthesis”

1S-8: Yozaburo Nakai, Shintaro Izumi, Ken Yamashita, Masanao Nakanou, Hiroshi Kawaguchi, Masahiko Yoshimoto (Kobe Univ., Japan) “A 14μA ECG Processor with Noise Tolerant Heart Rate Extractor and FeRAM for Wearable Healthcare Systems”

1S-9: Xiaowei Ren, Qihang Yu, Badong Chen, Nanning Zheng, Pengjiu Ren (Xi’an Jiaotong Univ., China) “A 128-Way FPGA Platform for the Acceleration of KLMS Algorithm”

1S-10: Xiaowei Ren, Qihang Yu, Badong Chen, Nanning Zheng, Pengjiu Ren (Xi’an Jiaotong Univ., China) “A Real-Time Permutation Entropy Computation for EEG Signals”

1S-11: Jiang Yu, Geng Liu, Xin Zhang, Pengjiu Ren (Xi’an Jiaotong Univ., China) “A High Efficient Hardware Architecture for Multiview 3DTV”

1S-12: Hsiao-Wei Chien, Junan-Ling Lai, Chao-Chieh Wu, Chih-Tsun Huang, Ting-Shuo Hsu, Jing-Jia Liou (National Tsing Hua Univ., Taiwan) “Design of A Scalable Many-Core Processor for Embedded Applications”


1S-14: Xiwei Huang, Jing Guo, Mei Yan, Hao Yu (Nanyang Technological Univ., Singapore) “A 64x64 1200fps Dual-Mode CMOS Ion-Image Sensor for Accurate DNA Sequencing”

1S-15: Toshihiro Ozaki, Tetsuya Hirose, Takahiro Nagai, Masahiro Numa (Kobe Univ., Japan) “0.21-V Minimum Input, 73.6% Maximum Efficiency, Fully Integrated 3-Terminal Voltage Converter with MPPT for Low-Voltage Energy Harvesters”

1S-16: Toshihiro Ozaki, Tetsuya Hirose, Takahiro Nagai, Keishi Tsukabaki, Nobutaka Saka, Masahiro Numa (Kobe Univ., Japan) “A 0.21-V Minimum Input, 73.6% Maximum Efficiency, Fully Integrated 3-Terminal Voltage Converter with MPPT for Low-Voltage Energy Harvesters”

1S-17: Junki Hashiba, Toru Kawajiri, Yuya Hasegawa, Hiroki Ishikuro (Keio Univ., Japan) “Dual-Output Wireless Power Delivery System for Small Size Large Volume Wireless Memory Card”

1S-18: Daisuke Kanemoto (Univ. of Yamanashi, Japan), Keigo Oshiro, Keiji Yoshida, Haruichi Kanaya (Kochi Univ., Japan) “A Tri-Level 50MS/s 10-bit Capacitive-DAC for Bluetooth Applications”

1S-19: Aravind Tharayil Narayanan, Wei Deng, Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan) “A Tail-Current Modulated VCO with Adaptive-Bias Scheme”

1S-20: Jili Zhang, Chenluan Wang, Shengxi Diao, Fujiang Lin (Univ. of Science and Tech. of China, China) “A Low-Power VCO Based ADC with Asynchronous Sigma-Delta Modulator in 65nm CMOS”


1S-22: Teerachat Siriburanon, Tomohiro Ueno, Kenio Kimura, Satoshi Kondo, Wei Deng, Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan) “A 58.3- to 65.4 GHz 34.2 mW Sub-Harmonically Injection-Locked PLL with a Sub-Sampling Phase Detection”

1S-23: Akira Okada, Abdul Raziz Junaidi, Yasuhiro Take, Atsutake Kusuge, Tadahiro Kuroda (Keio Univ., Japan) “Circuit and Package Design for 44GB/s Inductive-Coupling DRAM/SoC Interface”

1S-24: Li-Chung Hsu, Yasuhiro Take, Atsutake Kusuge, So Hasegawa, Junichiro Kadamoto, Tadahiro Kuroda (Keio Univ., Japan) “Design and Analysis for ThruChip Design for Manufacturing (DFM)”
2S: (Special Session) Internet of Things
Chair: Li Shang (Univ. of Colorado Boulder, U.S.A.)

2S-1: Hyung Gyu Lee (Daegu Univ., Republic of Korea) "Powering the IoT: Storage-Less and Converter-Less Energy Harvesting"

2S-2: Shao-Yi Chien, Wei-Kai Chan, Yu-Hsiang Tseng (National Taiwan Univ., Taiwan), Chia-Han Lee (Academia Sinica, Taiwan), V. Srinivasa Somayazulu, Yin-Kuang Chen (Intel, U.S.A.) "Distributed Computing in IoT: System-on-a-Chip for Smart Cameras as an Example"

2S-3: James Williamson, Qi Liu, Fenglong Lu, Wyatt Mohrman, Kun Li (Univ. of Colorado Boulder, U.S.A.), Li Shang (Univ. of Colorado Boulder, U.S.A.) "Data Sensing and Analysis: Challenges for Wearables"

2A: NoCS II (Power and Emerging Technology)
Chairs: Mehdi Tahoori (Karlsruhe Inst. of Tech., Germany), Tomoya Horiguchi (Toshiba)

2A-1: Hang Lu (Univ. of Chinese Academy of Sciences, China), Guihai Yan, Yinhe Han, Ying Wang (Chinese Academy of Sciences, China), Xiaowei Li (Univ. of Chinese Academy of Sciences, China) "ShuttleNoC: Boosting On-Chip Communication Efficiency by Enabling Localized Power Adaptation"

2A-2: Hui Li, Sébastien Le Beux (Lyon Institute of Nanotechnology, France), Gabriela Nicolescu (Ecole Polytechnique de Montréal, Canada), Ian O'Connor (Lyon Institute of Nanotechnology, France) "Energy-Efficient Optical Crossbars on Chip with Multi-Layer Deposited Silicon"

2A-3: Julian Hilgemberg Pontes, Pascal Vivet, Yvain Thonnart (CEA/LETI, France) "Two-Phase Protocol Converters for 3D Asynchronous I-of-n Data Links"

2A-4: Xiaohang Wang, Tengfei Wang (Chinese Academy of Sciences, China), Terrence Mak (Chinese Academy of Sciences/Chinese Univ. of Hong Kong, China), Mei Yang, Yingtao Jiang (Univ. of Nevada, Las Vegas, U.S.A.), Masoud Daneshfalih (Royal Inst. of Tech. Sweden/Univ. of Turku, Finland) "Fine-Grained Runtime Power Budgeting for Networks-on-Chip"

2B: Design Automation for Tomorrow’s Circuit Technologies
Chairs: Anupam Chattopadhyay (RWTH Aachen Univ., Germany), Shigeru Yamashita (Ritsumeikan Univ.)

2B-1: Shuangchen Li (Tsinghua Univ., China/Univ. of California, Santa Barbara, U.S.A.), Ang Li, Yongpan Liu (Tsinghua Univ., China), Yuan Xie (Univ. of California, Santa Barbara, U.S.A.), Huazhong Yang (Tsinghua Univ., China) "Nonvolatile Memory Allocation and Hierarchy Optimization for High-Level Synthesis"

2B-2: Robert Wille, Oliver Keszocze, Rolf Drechsler (Univ. of Bremen, Germany) "Reverse BDD-Based Synthesis for Splitter-Free Optical Circuits"

2B-3: Aaron Lye (Univ. of Bremen, Germany), Robert Wille, Rolf Drechsler (Univ. of Bremen/Cyber Physical Systems, DFKI GmbH, Germany) "Determining the Minimal Number of SWAP Gates for Multi-Dimensional Nearest Neighbor Quantum Circuits"

2B-4: Robert Wille, Oliver Keszocze, Rolf Drechsler (Univ. of Bremen/Cyber Physical Systems, DFKI GmbH, Germany) "Determining the Minimal Number of SWAP Gates for Multi-Dimensional Nearest Neighbor Quantum Circuits"

2C: Emerging Applications
Chairs: Juinn-Dar Huang (National Chiao Tung Univ., Taiwan), Youhua Shi (Waseda Univ.)

2C-1: Zipeng Li (Duke Univ., U.S.A.), Tsung-Yi Ho (National Chiao Tung Univ., Taiwan), Krishnendu Chakrabarty (Duke Univ., U.S.A.) "Design and Optimization of 3D Digital Microfluidic Biochips for the Polymerase Chain Reaction"

2C-2: Lixue Xia, Rong Luo, Bin Zhao, Yu Wang, Huazhong Yang (Tsinghua Univ., China) "An Accurate and Low Cost PM2.5 Estimation Method Based on Artificial Neural Network"

2C-3: Zhi Hu, Yibo Fan, Xiaoyang Zeng (Fudan Univ., China) "Iterative Disparity Voting Based Stereo Matching Algorithm and Its Hardware Implementation"

2C-4: Yu-Wei Wu (National Cheng Kung Univ., Taiwan), Yi-yu Shi (Missouri Univ. of Science and Tech., U.S.A.), Sudip Roy (National Cheng Kung Univ., Taiwan), Tsung-Yi Ho (National Chiao Tung Univ., Taiwan) "Obstacle-Avoiding Wind Turbine Placement for Power-Loss and Wake-Effect Optimization"
3S: (Special Session) New Challenges and Solutions in Nanometer Physical Design
Chair: Mark Po-Hung Lin (National Chung Cheng Univ., Taiwan)

3S-1: Haitong Tian (Univ. of Illinois, Urbana-Champaign, U.S.A.), Hongbo Zhang (Synopsys, U.S.A.), Zigang Xiao, Martin D. F. Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.) "An Efficient Linear Time Triple Patterning Solver"

3S-2: Tiago Reimann (Univ. Federal do Rio Grande do Sul, Brazil), Cliff C.N. Sze (IBM, U.S.A.), Ricardo Reis (Univ. Federal do Rio Grande do Sul, Brazil) "Gate Sizing and Threshold Voltage Assignment for High Performance Microprocessor Designs"

3S-3: Yasuhiro Takashima (Univ. of Kitakyushu, Japan) "Analytical Placement for Rectilinear Blocks"

3S-4: Eric Jia-Wei Fang, Terry Chi-Jih Shih, Dar- ton Shen-Yu Huang (MediaTek, Taiwan) "IR to Routing Challenge and Solution for Interposer-Based Design"

3A: Circuits for Performance and Reliability
Chairs: Sri Parameswaran (Univ. of New South Wales, Australia), Chengmo Yang (Univ. of Delaware)

3A-1: Anteneh Gebregiorgis (TU Delft, Netherlands), Mojtaba Ebrahimi, Saman Kiamehr, Fabian Oboril (Karlsruhe Inst. of Tech., Germany), Said Hamdiong (TU Delft, Netherlands), Mehdi Tahoori (Karlsruhe Inst. of Tech., Germany) "Aging Mitigation in Memory Arrays Using Self-Controlled Bit-Flipping Technique"

3A-2: Chang Liu, Xingshu Yang, Fei Qiao, Qi Wei, Huazhong Yang (Tsinghua Univ., China) "Design Methodology for Approximate Accumulator Based on Statistical Error Model"

3A-3: Linbo Wang, Jin Chen, Hanli Wang, Jianhua Wu, Zhiwei Fu, Zhong Li (Huazhong Univ. of Sci. and Tech., China) "A New Floorplanning Algorithm Based on Co-Types Bundle Cuts and Clustering"

3A-4: Eric Jia-Wei Fang, Terry Chi-Jih Shih, Dar- ton Shen-Yu Huang (MediaTek, Taiwan) "IR to Routing Challenge and Solution for Interposer-Based Design"

3B: Frontiers in Logic Synthesis
Chairs: Robert Wille (Univ. of Bremen, Germany), Yuko Hara-Azumi (Tokyo Inst. of Tech.)

3B-1: Luca Amaru (Integrated Systems Laboratory - EPFL, Switzerland), Gage Hills (Stanford Univ., U.S.A.), Pierre-Emmanuel Gaillardon (Integrated Systems Laboratory - EPFL, Switzerland), Subhashis Mitra (Stanford Univ., U.S.A.), Giovanni De Micheli (Integrated Systems Laboratory - EPFL, Switzerland) "Multiple Independent Gate FETs: How Many Gates Do We Need?"

3B-2: Subhendu Roy (Univ. of Texas, Austin, U.S.A.), Mihir Choudhury, Ruchir Puri (IBM, U.S.A.), David Z Pan (Univ. of Texas, Austin, U.S.A.) "Polynomial Time Algorithm for Area and Power Efficient Adder Synthesis in High-Performance Designs"

3B-3: Yusuke Matsunaga (Kyushu Univ., Japan) "Accelerating SAT-Based Boolean Matching for Heterogeneous FPGAs Using One-Hot Encoding and CEGAR Technique"

3B-4: Matthias Kauer, Swaminathan Narayanaswamy, Sebastian Steinhorst, Martin Lukasiewycz (TUM CREATE, Singapore), Samarjit Chakraborty (TU Munich, Germany) "Many-to-Many Active Cell Balancing Strategy Design"

3C: Energy Optimization for Electric Vehicles and Smart Grids
Chairs: Hideki Takase (Kyoto Univ., Japan), Yongpan Liu (Tsinghua Univ., China)

3C-1: Ji Li, Yanzi Wang, Xue Lin, Shahin Nazarian, Massoud Pedram (USC, U.S.A.) "Negotiation-Based Task Scheduling and Storage Control Algorithm to Minimize User’s Electric Bills under Dynamic Prices"

3C-2: Matthias Kauer, Swaminathan Narayanaswamy, Sebastian Steinhorst, Martin Lukasiewycz (TUM CREATE, Singapore), Samarjit Chakraborty (TU Munich, Germany) "Many-to-Many Active Cell Balancing Strategy Design"

3C-3: Ta-Yang Huang, Chia-Jui Chang (National Cheng Kung Univ., Taiwan), Chung-Wei Lin (Univ. of California, Berkeley, U.S.A.), Sudip Roy (National Cheng Kung Univ., Taiwan), Tsung-Yi Ho (National Chiao Tung Univ., Taiwan) "Intra-Vehicle Network Routing Algorithm for Wiring Weight and Wireless Transmit Power Minimization"

3C-4: Yusuke Sakumoto (Tokyo Metropolitan Univ., Japan), Ittetsu Taniguchi (Ritsumeikan Univ., Japan) "An Autonomous Decentralized Mechanism for Energy Interchanges with Accelerated Diffusion Based on MCMC"

ACM SIGDA Student Research Forum at ASP-DAC 2015 [Food will be served] (18:00 - 20:00)
(The title of the posters are listed in the next page)
1. Ahmed Awad (Tokyo Institute of Technology) “A Fast Process Variation and Pattern Fidelity Aware Mask Optimization Algorithm”
2. Alireza Shafaei (University of Southern California) “Energy Efficient Cache Memories in Deeply-Scaled Technologies”
3. Boxun Li (Tsinghua University) “Energy Efficient System Design for Neural Networks”
4. Ching-Yi Huang (National Tsing Hua University) "Analysis and Power Optimization for Probabilistic Boolean Circuits"
6. Hayato Mashiko (University of Aizu) “A Tuning Method of Programmable Delay Element with an Ordered Finite Set of Delays for Yield Improvement”
7. Jaemin Kim (Seoul National University, KAIST) “Reconfigurable PV Powered Full Electric Vehicles”
8. Jan Malburg (University of Bremen) “Feature Localization and Design Understanding for Hardware Designs”
10. Keitaro Takizawa (University of Aizu) "Development of A Design Environment for Asynchronous Circuits with Bundle-data Implementation on FPGAs”
11. Mengying Zhao (City University of Hong Kong) “Endurance and Energy Aware Optimizations for Phase Change Memory”
12. Renhai Chen (Hong Kong Polytechnic University) “vFlash: Unified Non-Volatile Memory and NAND Flash Memory Architecture in Smartphones”
13. Rickard Ewetz (Purdue University) “Robust Clock Network Synthesis”
15. Sergej Deutsch (Duke University) "Contactless Pre-Bond TSV Test and Diagnosis Using Ring Oscillators and Multiple Voltage Levels"
16. Shengcheng Wang (Karlsruhe Institute of Technology) “Multi-objective P/G TSV Planning in 3D-ICs”
17. Shoichi Iizuka (Osaka University) “Fast Error Rate Estimation with Stochastic Modeling for Adaptive Speed Controlled Circuit”
20. Xiang Chen (University of Pittsburgh) “Demystify Energy Usage in Smartphones”
22. Xiao Zhu (Chongqing University) “Understanding Swapping in Mobile Systems”
23. Xiwei Huang (Nanyang Technological University) “A Contact-Imaging Based Microfluidic Cytometer with Machine-Learning for Single-Frame Super-Resolution Processing”
### Registration (7:30 - )

**9:00**

**2K: Keynote II**
- **Chair:** Kunio Uchiyama (Hitachi)
- Atsushi Takahara (NTT, Japan) "Programmable Network"

**9:50**

Coffee break (9:50 - 10:15)

### 10:15

**4S: (Special Session) Machine Learning in EDA: Promises and Challenges in Selected Applications**
- **Chair:** Li-C. Wang (Univ. of California, Santa Barbara, U.S.A.)

1. **4S-1:** Bei Yu, David Z. Pan (Univ. of Texas, Austin, U.S.A.), Tetsuaki Matsumanawa (Toshiba, Japan), Xuan Zeng (Fudan Univ., China) "Machine Learning and Pattern Matching in Physical Design"

2. **4S-2:** Fangming Ye, Krishnendu Chakrabarty (Duke Univ., U.S.A.), Zhaobo Zhang, Xinli Gu (Huawei Technologies, U.S.A.) "Self-Learning and Adaptive Board-Level Functional Fault Diagnosis"

3. **4S-3:** Shupeng Sun, Xin Li (Carnegie Mellon Univ., U.S.A.) "Fast Statistical Analysis of Rare Failure Events for Memory Circuits in High-Dimensional Variation Space"

4. **4S-4:** Li-C. Wang (Univ. of California, Santa Barbara, U.S.A.) "Data Mining in Functional Test Content Optimization"

### 12:20

Lunch Break (12:20 - 13:50)

### 13:50

### 14A: Efficient NVM Management, from Register to Disk**
- **Chairs:** Kyoungwoo Lee (Yonsei Univ., Republic of Korea), Koji Nii (Renesas Electronics)

1. **4A-1:** Mimi Xie, Chen Pan, Jingtong Hu (Okahama State Univ., U.S.A.), Chengmo Yang (Univ. of Delaware, U.S.A.), Yiran Chen (Univ. of Pittsburgh, U.S.A.) "Checkpoint-Aware Instruction Scheduling for Non-volatile Processor with Multiple Functional Units"

2. **4A-2:** Linbo Long, Duo Liu, Xiao Zhu, Kan Zhong (Chongqing Univ., China), Zili Shao (Hong Kong Polytechnic Univ., Hong Kong), Edwin H.-M. Sha (Chongqing Univ., China) "Balloonfish: Utilizing Morphable Resistive Memory in Mobile Virtualization"

3. **4A-3:** Yunbin Li, Xin Li, Lei Ju, Zhiping Jia (Shandong Univ., China) "A Three-Stage-Write Scheme with Flip-Flip for PCM Main Memory"

4. **4A-4:** Min Huang (Harbin Inst. of Tech., China), Yi Wang (Shenzhen Univ./Hong Kong Polytechnic Univ., China), Zhaqing Liu, Liyan Qiao (Harbin Inst. of Tech., China), Zili Shao (Hong Kong Polytechnic Univ., Hong Kong) "A Garbage Collection Aware Stripping Method for Solid-State Drives"

5. **4A-5:** Renhai Chen (Hong Kong Polytechnic Univ., Hong Kong), Yi Wang (Shenzhen Univ., China), Jingtong Hu (Okahama State Univ., U.S.A.), Duo Liu (Chongqing Univ., China), Zili Shao (Hong Kong Polytechnic Univ., Hong Kong), Yong Guan (Capital Normal Univ., China) "Unified Non-Volatile Memory and NAND Flash Memory Architecture in Smartphones"

### 14B: Robust Timing, and P/G Modeling and Design**
- **Chairs:** Ray Cheung (City Univ. of Hong Kong, Hong Kong), Fan Yang (Fudan Univ., China)

1. **4B-1:** Palkesh Jain (Qualcomm India Pvt, India), Sachin S. Sapatnekar (Univ. of Minnesota, U.S.A.), Jordi Cortadella (Univ. Politecnica de Catalunya, Spain) "A Retargetable and Accurate Methodology for Logic-IP-Internal Electromigration Assessment"

2. **4B-2:** Hai-Bao Chen, Sheldon X.-D. Tan, Xin Huang (Univ. of California, Riverside, U.S.A.), Valery Sukharev ( Mentor Graphics, U.S.A. ) "New Electromigration Modeling and Analysis Considering Time-Varying Temperature and Current Densities"

3. **4B-3:** Zahi Moudalal, Farid N Najm (Univ. of Toronto, Canada) "Generating Circuit Current Constraints to Guarantee Power Grid Safety"

4. **4B-4:** Aadithya Karthik (UC Berkeley, U.S.A.), Sayak Ray (Princeton Univ., U.S.A.), Jaijeet Roychowdhury (UC Berkeley, U.S.A.) "BEE: Predicting Realistic Worst Case and Stochastic Eye Diagrams by Accounting for Correlated Bitstreams and Coding Strategies"

5. **4B-5:** Chung-Hao Tsai, Wai-Kei Mak (National Tsing Hua Univ., Taiwan) "A Fast Parallel Approach for Common Path Pessimism Removal"

### 14C: New Issues in Placement and Routing**
- **Chairs:** Shigetoshi Nakatake (Univ. of Kitakyushu, Japan), Yuzi Kanazawa (Fujitsu Labs.)

1. **4C-1:** Chau-Chin Huang, Chien-Hsiung Chiou, Kai-Han Tseng, Yao-Wen Chang (National Taiwan Univ., Taiwan) "Detailed-Routing-Driven Analytical Standard-Cell Placement"

2. **4C-2:** Shih-Ying Liu (National Chiao Tung Univ./MediaTek, Taiwan), Hung-Chi Shao (Synopsys, Taiwan), Hung-Ming Chen (National Chiao Tung Univ., Taiwan) "An Approach to Anchoring and Placing High Performance Custom Digital Designs"

3. **4C-3:** Po-Ya Hsu, Yao-Wen Chang (National Taiwan Univ., Taiwan) "Non-Stitch Triple Pattern-Aware Routing Based on Conflict Graph Pre-Coloring"

4. **4C-4:** Shao-Yun Fang (National Taiwan Univ. of Science and Tech., Taiwan) "Cut Mask Optimization with Wire Planning in Self-Aligned Multiple Patterning Full-Chip Routing"

5. **4C-5:** Ran Zhang, Tieyun Pan, Li Zhu, Takahiro Watanabe (Waseda Univ., Japan) "A Length Matching Routing Method for Disordered Pins in PCB Design"
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<td>Hidekazu Nishimura (Keio Univ., Japan) “Systems Modeling for Additional Development in Automotive E/E Architecture”</td>
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<td>5S-2:</td>
<td>Nao Ozaki, Masato Uchiyama, Yasuki Tanabe, Shuichi Miyazaki, Takaaki Sawada, Takanori Tamai, Moriyasu Banno (Nihon University, Japan) “Implementation and Evaluation of Image Recognition Algorithm for An Intelligent Vehicle using Heterogeneous Multi-Core SoC”</td>
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<td>15:30</td>
<td>Coffee break (15:30 - 15:50)</td>
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<tr>
<td>5A:</td>
<td>Optimization and Exploration for Caches</td>
<td>Chairs: Hiroyuki Tomiyama (Ritsumeikan Univ., Japan), Lin Meng (Ritsumeikan Univ., Japan)</td>
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<td>5A-1:</td>
<td>Haifeng Xu (Univ. of Pittsburgh, U.S.A.), Yong Li (VMware, U.S.A.), Rami Melhem, Alex K. Jones (Univ. of Pittsburgh, U.S.A.) “Multilane Racetrack Caches: Improving Efficiency Through Compression and Independent Shifting”</td>
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<td>5A-3:</td>
<td>Guantao Liu, Tim Schmidt, Rainer Doerner (Univ. of California, Irvine, U.S.A.), Ajit Dangankar, Desmond Kirkpatrick (Intel, U.S.A.) “Optimizing Thread-to-Core Mapping on Manycore Platforms with Distributed Tag Directories”</td>
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<td>5A-4:</td>
<td>Mohammad Shihabul Haque, Ang Li, Akash Kumar (National Univ. of Singapore, Singapore), Qingsong Wei (Data Storage Institute, Singapore) “Accelerating Non-Volatile/Hybrid Processor Cache Design Space Exploration for Application Specific Embedded Systems”</td>
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<td>5B:</td>
<td>CAD for Analog/RF/Mixed-Signal Design</td>
<td>Chairs: Sheldon Tan (Univ. of California, Riverside, U.S.A.), Mark Po-Hung Li (National Chung Cheng Univ., Taiwan)</td>
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<td>5B-1:</td>
<td>Ying-Chih Wang, Shihui Yin, Minhee Jun, Xin Li, Lawrence T. Pileggi, Damir M. Maric, Rohit Negi (Carnegie Mellon Univ., U.S.A.) “Accurate Passivity-Enforced Macromodeling for RF Circuits via Iterative Zero/Pole Update Based on Measurement Data”</td>
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<td>5B-2:</td>
<td>Volker Meyer zu Bexten, Markus Tristl (Infineon Technologies AG, Germany), Dina Medhat (Mentor Graphics, Egypt) “Physical Verification Flow for Hierarchical Analog IC Design Constraints”</td>
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<td>5B-3:</td>
<td>Zhijian Pan, Chuan Qin, Zuochang Ye, Yan Wang (Tsinghua Univ., China) “Automatic Design for Analog/RF Front-End System in 802.11ac Receiver”</td>
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<td>5B-4:</td>
<td>Qicheng Huang, Xiao Li, Fan Yang, Xuan Zeng (Fudan Univ., China), Xin Li (Fudan Univ., China/Carnegie Mellon Univ., U.S.A.) “SIPredict: Efficient Post-Layout Waveform Prediction via System Identification”</td>
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<td>5C:</td>
<td>Next-Generation Clock Network Synthesis</td>
<td>Chairs: Atsushi Takahashi (Tokyo Inst. of Tech.), David Z. Pan (Univ. of Texas, Austin, U.S.A.)</td>
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<td>5C-1:</td>
<td>Juyeon Kim, Taewhan Kim (Seoul National Univ., Republic of Korea) “Useful Clock Skew Scheduling Using Adjustable Delay Buffers in Multi-Power Mode Designs”</td>
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<td>5C-2:</td>
<td>Rickard Ewetz (Purdue Univ., U.S.A.), Shankarshana Janarthanan (NVIDIA, U.S.A.), Cheng-Kok Koh (Purdue Univ., U.S.A.) “Fast Clock Skew Scheduling Based on Sparse-Graph Algorithms”</td>
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<td>5C-3:</td>
<td>Wulong Liu (Tsinghua Univ., China), Guoqing Chen (Research Lab, Advanced Micro Devices, China), Yu Wang, Huazhong Yang (Tsinghua Univ., China) “Modeling and Optimization of Low Power Resonant Clock Mesh”</td>
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<td>5C-4:</td>
<td>Seyong Ahn, Minseok Kang (Seoul National Univ., Republic of Korea), Marios C. Papaefthymiou (University of Michigan, U.S.A.), Taewhan Kim (Seoul National Univ., Republic of Korea) “Synthesis of Resonant Clock Networks Supporting Dynamic Voltage / Frequency Scaling”</td>
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<td>15:50</td>
<td>6A:</td>
<td>Optimization Techniques for Non-Volatile Memory based Systems</td>
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<td>6B:</td>
<td>Test for Higher Quality</td>
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<td>17:30</td>
<td>6C:</td>
<td>Reliability</td>
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**Panelists:**
- Kento Aida (NII, Japan)
- Derek Chiou (Microsoft, U.S.A.)
- Hiroshi Nakamura (Univ. of Tokyo, Japan)
- Hiroyuki Tanaka (Nippon Telegraph and Telephone, Japan)
- Iwao Yamazaki (Fujitsu, Japan)

**Panelists (6A):**
- Xiaoxiao Liu, Mengjie Mao, Xiuyuan Bi, Hai Li, Yiran Chen (Univ. of Pittsburgh, U.S.A.)

**Panelists (6B):**
- Songwei Pei, Ye Geng (Beijing Univ. of Chemical Tech., China), Huawei Li (Key Laboratory of Computer System and Architecture, Institute of Computing Technology, China), Jun Litt (Hefei Univ. of Tech., China), Song Jih (North China Electric Power Univ., China)

**Panelists (6C):**
- Minjie Lv, Hongbin Sun, Jingmin Xin, Nanjing Zheng (Xi’an Jiaotong Univ., China), Martin Wong (UIUC, U.S.A.)
Thursday, January 22, 2015

Registration (7:30 - )

Coffee break (9:50 - 10:15)

7A: Ensuring the Correctness of System Integration
Chairs: Takeshi Matsumoto (Ishiyama National College of Tech.), Akash Kumar (National Univ. of Singapore, Singapore) 
7A-2: Li-chun Chen, Hsin-I Wu, Ren-Song Tsay (National Tsing Hua Univ., Taiwan) "Automatic Timing-Independent Transactor Generation for Mixed-Level Simulations"
7A-3: Hsuan-Ming Cheng, Hong-Chang Wu, Yi-Chia Chen, Jean Tsao, Shih-Chieh Chang (National Tsing Hua Univ., Taiwan) "Hybrid Coverage Assertions for Efficient Coverage Analysis Across Simulation and Emulation Environments"
7A-4: Luis Gabriel Murillo, Richard Lajos, Bert Asnashari (Ishiyama National College of Tech.) "SWAT: Assertion-Based Debugging of Concurrency Issues at System Level"

7B: Orchestrating Tasks, Cores, and Communication
Chairs: Zhi Shao (Hong Kong Polytechnic Univ., Hong Kong), Masanori Hashimoto (Osaka Univ., Japan) 
7B-2: Cheng Tan, Thannirmalai Somu Muthukaruppan, Tulika Mitra (National Univ. of Singapore, Singapore), Lei Ju (Shandong Univ., China) "Approximation-Aware Scheduling on Heterogeneous Multi-Core Architectures"
7B-3: Martin Becker (Tech. Univ. of Munich, Germany), Alejandro Masrur (Software Technology for Embedded Systems, Technical Univ. Chemnitz, Germany), Samarjit Chakraborty (Tech. Univ. of Munich, Germany) "Composing Real-Time Applications from Communicating Black-Box Components"

7C: Design for Manufacturability
Chairs: Shigeki Nojima (Toshiba, Japan), Eric J.-W. Fang (MediaTek, Taiwan) 
7C-1: Zigang Xiao, Yuelin Du, Martin D.F. Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.), He Yi, H.-S. Philip Wong (Stanford Univ., U.S.A.), Hongbo Zhang (Synopsys, U.S.A.) "Contact Pitch and Location Prediction for Directed Self-Assembly Template Verification" 
7C-2: Yunfeng Yang, Wai-Shing Luk (Fudan Univ., China), Hai Zhou (Fudan Univ., China/Northwestern Univ., U.S.A.), Changhao Yan, Xuan Zeng (Fudan Univ., China), Dian Zhou (Fudan Univ., China/Univ. of Texas, Dallas, U.S.A.) "Layout Decomposition Co-Optimization for Hybrid E-Beam and Multipatterning Lithography"
7C-3: Daifeng Guo, Yuelin Du, Martin D.F. Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.) "Polynomial Time Optimal Algorithm for Stencil Row Planning in E-Beam Lithography"
7C-4: Yukihide Kohira (Univ. of Aizu, Japan), Tomomi Matsui (Tokyo Inst. of Tech., Japan), Yoko Yokoyama, Chikaaki Kodama (Toshiba, Japan), Atsushi Takahashi (Tokyo Inst. of Tech., Japan), Shigeki Nojima, Satoshi Tanaka (Toshiba, Japan) "Fast Mask Assignment Using Positive Semidefinite Relaxation in LELECU Triple Patterning Lithography"
7C-5: Shao-Yun Fang (National Taiwan Univ. of Science and Tech., Taiwan), Yi-Shu Tai, Yao-Wen Chang (National Taiwan Univ. of Science and Tech., Taiwan) "Layout Decomposition for Spacer-is-Metal (SIM) Self-Aligned Double Patterning"

Lunch Break (12:20 - 13:50) IEEE CASS/CEDA Luncheon Presentations [Food will be served] (12:30 - 13:30)
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<td>8S</td>
<td>Technology Trend toward 8K Era</td>
<td>Hiroe Iwasaki (NTT, Japan), Chair: Masaitsu Nakajima (Panasonic, Japan)</td>
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<td>8S-1</td>
<td>“The Prospects of Next Generation Television - Japan’s Initiative to 2020 -”</td>
<td>Keiya Motohashi (NetTV Forum, Japan)</td>
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<td>8S-2</td>
<td>“8K LCD : Technologies and Challenges toward the Realization of SUPER Hi-VISION TV”</td>
<td>Takeshi Kumakura (SHARP, Japan)</td>
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<td>8S-3</td>
<td>“The World’s 1st Complete-4K SoC Solution with Hybrid Memory System”</td>
<td>Daisuke Murakami, Yuki Soga, Daisuke Imoto, Yoshiharu Watanabe, Takashi Yamada (Panasonic, Japan)</td>
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<td>8S-4</td>
<td>“H.265/HEVC Encoder for UHDTV”</td>
<td>Mitsuo Ikeda (NTT, Japan)</td>
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<td>8A</td>
<td>Exploring Better Architecture of Your Systems</td>
<td>Rainer Doemer (Univ. of California, Irvine, U.S.A.), Hoeseok Yang (Ajaon Univ., Republic of Korea)</td>
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<td>8A-1</td>
<td>“An Accurate ACOSO Metamodeling Technique for Processor Architecture Design Space Exploration”</td>
<td>Hongwei Wang (Beijing Key Laboratory of Mobile Computing and Pervasive Device/Chinese Academy of Sciences, China), Ziyuan Zhu, Jinglin Shi, Yongtao Su (Beijing Key Laboratory of Mobile Computing and Pervasive Device/Chinese Academy of Sciences, China)</td>
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<td>8A-2</td>
<td>“Speeding Up Single Pass Simulation of PLRU Caches”</td>
<td>Josef Schneider, Jorgen Peddersen, Sri Parameswaran (Univ. of New South Wales, Australia), Jörg Henkel (Karlsruhe Inst. of Tech., Germany), Daisuke Imoto (Univ. of Montpellier II, France)</td>
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<td>8A-3</td>
<td>“ADAPT: An ADaptive Manycore Methodology for Software Pipelined Applications”</td>
<td>Xi Zhang, Haris Javaid (Univ. of New South Wales, Australia), Muhammad Shahique (Karlsruhe Inst. of Tech., Germany), Jude Angelo Ambrose (Univ. of New South Wales, Australia)</td>
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<td>8A-4</td>
<td>“A Trace-Driven Approach for Fast and Accurate Simulation of Manycore Architectures”</td>
<td>Anastasia Butko, Rafael Garibotti, Luciano Laporte, Abdoulaye Gamatie, Gilles Sassatelli (LIRMM/CNRS), Chris Adeniyi-Jones (ARM, U.K.)</td>
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<td>8B</td>
<td>Circuit-Level Modeling and Simulation</td>
<td>Luca Daniel (Massachusetts Inst. of Tech., U.S.A.), Takashi Sato (Kyoto Univ.)</td>
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<td>8B-1</td>
<td>“Compact Modeling of Microbatteries Using Behavioral Linearization and Model-Order Reduction”</td>
<td>Mohammed Shemsu Nesro (Masdar Inst. of Tech., United Arab Emirates), Lizhong Sun (Applied Materials, U.S.A.), Ibrahim (Abe) M. Elfadel (Masdar Inst. of Science and Tech., United Arab Emirates)</td>
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<td>8B-2</td>
<td>“GPU-Accelerated Parallel Monte Carlo Analysis of Analog Circuits by Hierarchical Graph-Based Solver”</td>
<td>Yan Zhu, Sheldon X.-D. Tan (Univ. of California Riverside, U.S.A.)</td>
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<td>8B-3</td>
<td>“Automated Generation of Hybrid System Models for Reachability Analysis of Nonlinear Analog Circuits”</td>
<td>Hyun-Seok Lukas Lee (Leibniz Univ. Hannover, Germany), Matthias Althoff (Tech. Univ. Munchen, Germany), Stefan Heeßelmpf, Markus Olbrich, Erich Barke (Leibniz Univ. Hannover, Germany)</td>
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<td>8C</td>
<td>Reliable and Trustworthy Electronics</td>
<td>Takashi Aikyo (STARC, Japan), Eishi Ibe (Hitachi)</td>
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<td>8C-1</td>
<td>“On Test Syndrome Merging for Reasoning-Based Board-Level Functional Fault Diagnosis”</td>
<td>Zelong Sun (Chinese Univ. of Hong Kong, Hong Kong), Qiang Xu (Chinese Univ. of Hong Kong, Hong Kong), Zhiyuan Wang, Xinli Gu (Huawei Technologies, U.S.A.)</td>
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<td>8C-2</td>
<td>“Event-Driven Transient Error Propagation: A Scalable and Accurate Soft Error Rate Estimation Approach”</td>
<td>Daisuke Fujimoto, Makoto Nagata (Kobe Univ., Japan), Shivam Bhasin, Jean-Luc Danger (Telecom ParisTech, France)</td>
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<td>8C-3</td>
<td>“Hardware Trojan Detection Using Exhaustive Testing of k-bit Subspaces”</td>
<td>Nicole Lesperance, Shrikant Kulkarni, Kwang-Ting Cheng (UC Santa Barbara, U.S.A.)</td>
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<td>Time</td>
<td>Panel Discussion: IP Base SoC Design and IP Design Innovation</td>
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<td>15:50</td>
<td>9A: Power/Thermal Management and Modeling</td>
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<td><strong>Chair:</strong> Donghwa Shin (Yeungnam Univ., Republic of Korea)</td>
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<td><strong>Takashi Nakada</strong> (Univ. of Tokyo, Japan)</td>
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<td>Hironori Ando (Synopsys, Japan)</td>
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<td>Kevin Yee (Cadence, U.S.A.)</td>
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<td>Randy Smith (Sonics, U.S.A.)</td>
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<td>Neil Parris (ARM, U.K.)</td>
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<td><strong>9A-1:</strong> Zih-Ci Huang, Chi-Kang Chen, Ren-Song Tsay (National Tsing Hua Univ., Taiwan) “AROMA: A Highly Accurate Microcomponent-Based Approach for Embedded Processor Power Analysis”</td>
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<td><strong>9A-2:</strong> Yu Peng, Shouyi Yin, Leibo Liu, Shaojun Wei (Tsinghua Univ., China) “Battery-Aware Mapping Optimization of Loop Nests for CGRAs”</td>
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<td><strong>9A-3:</strong> Jinho Lee, Junwhan Ahn, Kiyoung Choi (Seoul National Univ., Republic of Korea), Kyungsu Kang (Samsung Electronics, Republic of Korea) “THOR: Orchestrated Thermal Management of Cores and Networks in 3D Many-Core Architectures”</td>
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<td><strong>9A-4:</strong> Jianlei Yang (Tsinghua Univ./Intel, China), Liwei Ma, Kang Zhao (Intel, China), Yici Cai (Tsinghua Univ., China), Tin-Fook Ngai (Intel, China) “Early Stage Real-Time SOC Power Estimation Using RTL Instrumentation”</td>
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<td>17:30</td>
<td><strong>9B: (Special Session) System-Level Designs and Tools for Multicore Systems</strong></td>
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<td><strong>Organizer:</strong> Chung-Ta King (National Tsing Hua Univ., Taiwan)</td>
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<td><strong>9B-1:</strong> Qiaoshua Zou, Matthew Poremba (Pennsylvania State Univ., U.S.A.), Rui He, Wei Yang, Junfeng Zhao (Huawei Shannon Lab, China), Yuan Xie (Univ. of California, Santa Barbara, U.S.A.) “Heterogeneous Architecture Design with Emerging 3D and Non-Volatile Memory Technologies”</td>
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<td><strong>9B-2:</strong> Zhehui Wang, Jiang X, Peng Yang, Xuan Wang, Zhe Wang, Lun H.K. Duong, Zhifei Wang, Haoran Li, Rafael K.V. Maeda, Xiaowen Wu (Hong Kong Univ. of Science and Tech., Hong Kong), Yaoyao Ye, Qinfen Hao (Huawei Technologies, China) “Alleviate Chip I/O Pin Constraints for Multicore Processors through Optical Interconnects”</td>
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<td><strong>9B-3:</strong> Ting-Shuo Hsu, Jun-Lin Chiu, Chao-Kai Yu, Jing-Jia Lou (National Tsing Hua Univ., Taiwan) “A Fast and Accurate Network-on-Chip Timing Simulator with a Flit Propagation Model”</td>
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<td><strong>9B-4:</strong> Chih-Tsun Huang, Kuan-Chun Tasi, Jun-Shen Lin, Hsiao-Wei Chieh (National Tsing Hua Univ., Taiwan) “Application-Level Embedded Communication Tracer for Many-Core Systems”</td>
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<td><strong>9C: Building Secure Systems</strong></td>
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<td><strong>Chair:</strong> Wenjing Rao (Univ. of Illinois, Chicago, U.S.A.), Sandip Ray (Intel, Portland, U.S.A.)</td>
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<td><strong>9C-1:</strong> Sixing Lu, Minjun Seo, Roman Lysecky (Univ. of Arizona, U.S.A.) “Timing-Based Anomaly Detection in Embedded Systems”</td>
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<td><strong>9C-2:</strong> Carson J Dunbar, Gang Q (Univ. of Maryland, U.S.A.) “Satisfiability Don’t Care Condition Based Circuit Fingerprinting Techniques”</td>
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<td><strong>9C-3:</strong> Soroush Khaleghi, Kai Da Zhao, Wenjing Rao (Univ. of Illinois, Chicago, U.S.A.) “IC Piracy Prevention via Design Withholding and Entanglement”</td>
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<td><strong>9C-4:</strong> Lingxiao Wei, Jie Zhang, Feng Yuan, Yuan Nan Liu (Chinese Univ. of Hong Kong, Hong Kong), Junfeng Fan (Open Security Research, China), Qiang Xu (Chinese Univ. of Hong Kong, Hong Kong) “Vulnerability Analysis for Crypto Devices against Probing Attack”</td>
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FEES

<table>
<thead>
<tr>
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<tbody>
<tr>
<td><strong>Conference</strong></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>*Member</td>
<td>53,000 yen</td>
<td>58,000 yen</td>
<td>60,000 yen</td>
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<td>Non-member</td>
<td>63,000 yen</td>
<td>68,000 yen</td>
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<td>33,000 yen</td>
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<td>40,000 yen</td>
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<tr>
<td><strong>Keynotes + Designers' Forum</strong></td>
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<tr>
<td>* Member of IEEE, ACM SIGDA, IEICE, IPSJ</td>
<td>23,000 yen</td>
<td>28,000 yen</td>
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<tr>
<td><strong>Tutorial</strong></td>
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<tr>
<td>*Member</td>
<td>22,000 yen</td>
<td>26,000 yen</td>
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<td>14,000 yen</td>
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<td><strong>Student Group</strong></td>
<td>10,000 yen</td>
<td>12,000 yen</td>
<td>N/A</td>
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<td>* Member of IEEE, ACM SIGDA, IEICE, IPSJ</td>
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</table>
| **"Student Group" discount is applied to a group of four or more students from the same affiliation (faculty or graduate school). A list of the group members must be submitted. Please check the details in the following registration form.**

The conference fee includes:

- Admission to all sessions including keynote speeches and Designers’ Forum except tutorials
- A conference kit (a final program and an authority to access the download site*** for the conference proceedings)
- One refreshment per break

The Designers’ Forum fee includes:

- Admission to Designers’ Forum sessions and keynote speeches
- A conference kit (a final program and an authority to access the download site*** for the conference proceedings)
- One refreshment per break

CANCELLATION AND REFUND

When written notification of cancellation is received by the conference secretariat by December 12, 2014, 5,000 yen will be deducted from the fees paid to cover administrative costs. No refunds will be made for cancellation requests received after this date. Speakers are not allowed to cancel registrations.

ON-SITE REGISTRATION HOURS

<table>
<thead>
<tr>
<th>Day</th>
<th>January 19</th>
<th>January 20</th>
<th>January 21</th>
<th>January 22</th>
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<tbody>
<tr>
<td>Monday</td>
<td>8:00 – 18:00</td>
<td>7:00 – 17:00</td>
<td>7:30 – 17:00</td>
<td>7:30 – 17:00</td>
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<tr>
<td>Tuesday</td>
<td>7:00 – 17:00</td>
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<tr>
<td>Wednesday</td>
<td>7:30 – 17:00</td>
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<tr>
<td>Thursday</td>
<td>7:30 – 17:00</td>
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</table>

Advance Registration Deadline: Dec. 12th, 2014

The tutorial fee includes:

- Admission to tutorials
- Access to electronic files of tutorial presentations
- One lunch coupon
- One refreshment per break
Information

Proceedings:
ASP-DAC 2015 will be producing an authority to access the download site for the conference proceedings. The site will be open on Jan. 19, 2015. Please note that neither CD-ROM nor USB memory are provided.

Banquet:
Conference registrants are invited to attend a banquet to be held on January 21, 2015. The banquet will be held from 18:00 to 20:00 at the Convention Hall A. Regular Member and Non-member Conference registrants receive a ticket to the banquet when they register at the conference. Full-time students, Designers’ Forum-only registrants, and Tutorial-only registrants wishing to attend the banquet will be required to pay 5,000 yen for a ticket when they register on site.

20th Anniversary Reception:
This year, ASP-DAC marks its 20th anniversary, and we have the 20th Anniversary Reception on January 19, 2015. Conference registrants are invited to the reception. The reception will be held from 18:00 to 19:30 at Room 201. Please come and celebrate the 20th anniversary.

Passport and Visa:
To visit Japan, you must have a valid passport. A visa is required for citizens of countries that do not have visa-exempt agreements with Japan. Please contact the nearest Japanese Embassy or Consulate for visa requirements. The following Web page of Japanese embassy may be helpful. http://www.mofa.go.jp/j_info/visit/visa/

Duty free import:
Personal effects and professional equipment can be brought into Japan duty free as long as their contents and quantities are deemed reasonable by the customs officer. You can also bring in 400 cigarettes, 500 grams of tobacco or 100 cigars; 3 bottles of alcoholic beverages; 2 ounces of perfume; and gifts and souvenirs whose total market price is less than 200,000 yen or its equivalent. Firearms and other types of weapons, and narcotics are strictly prohibited.

Insurance:
The organizer cannot accept responsibility for accidents that might occur. Delegates are encouraged to purchase travel insurance before leaving their home country. Insurance plans typically cover accidental loss of belongings, medical costs in case of injury or illness, and other possible risks of international travel.

Climate:
Average temperature in winter (Jan.):

<table>
<thead>
<tr>
<th>City</th>
<th>T(F)</th>
<th>T(C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sapporo</td>
<td>25.4</td>
<td>-4</td>
</tr>
<tr>
<td>Sendai</td>
<td>34.7</td>
<td>1.5</td>
</tr>
<tr>
<td>Tokyo, Chiba</td>
<td>42.4</td>
<td>5.8</td>
</tr>
<tr>
<td>Nagoya</td>
<td>39.7</td>
<td>4.3</td>
</tr>
<tr>
<td>Kyoto</td>
<td>38.3</td>
<td>3.5</td>
</tr>
<tr>
<td>Osaka</td>
<td>42.4</td>
<td>5.8</td>
</tr>
<tr>
<td>Fukuoka</td>
<td>43.5</td>
<td>6.4</td>
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<tr>
<td>Naha</td>
<td>61.9</td>
<td>16.6</td>
</tr>
</tbody>
</table>

Currency Exchange:
Only Japanese yen (JPY, ¥) is acceptable at regular stores and restaurants. Certain foreign currencies may be accepted at a limited number of hotels, restaurants and souvenir shops. You can buy yen at foreign exchange banks and other authorized money exchangers on presentation of your passport.

Travelers checks and credit cards:
Travelers checks are accepted only by leading banks and major hotels in principal cities, and the use of travelers checks in Japan is not as popular as in some other countries. VISA, MasterCard, Diners Club, and American Express are widely accepted at hotels, department stores, shops, restaurants and nightclubs.

Tipping:
In Japan, tips are not necessary anywhere, even at hotels and restaurants.

Electricity:
Electric voltage is uniformly 100 volts, AC, throughout Japan, but with two different cycles: 50 in Eastern Japan*, and 60 in Western Japan**. Leading hotels in major cities have two outlets of 100 and 220 volts but their sockets usually accept a two-leg plug only.

*Eastern Japan: Tokyo, Chiba, Yokohama, Tohoku, Hokkaido
**Western Japan: Nagoya, Osaka, Kyoto, Hiroshima, Shikoku, Kyushu

Shopping:
Shops and other sales outlets in Japan are generally open on Saturdays, Sundays and national holidays as well as weekdays from 10:00 to 20:00. Department stores, however, are closed on one weekday, differing by store, and certain specialty shops may not open on Sundays and national holidays.

Other Information:
JAPAN NATIONAL TOURISM ORGANIZATION
http://www.jnto.go.jp/
NARITA AIRPORT
HANEDA AIRPORT
YES ! TOKYO
http://tcvb.or.jp/en/
CHIBA, JAPAN TRAVEL GUIDE
Access to Makuhari Messe

- ASP-DAC 2015 Conference will take place at “International Conference Hall.”

- It is located in Makuhari Messe International Convention Complex.