ASP-DAC 2015 Advance Program

20th Asia and South Pacific Design Automation Conference
Date: January, 19-22, 2015
Place: Chiba/Tokyo, Japan

Highlights

Opening and Keynote I

Tuesday, January 20, 2015, 8:30-9:50

Udo Wolz **(Executive Vice President and Director for Engineering and Innovation, Bosch Corporation)** *"The required technologies for Automotive towards 2020"*

Keynote II

Wednesday, January 21, 2015, 9:00-9:50

Atsushi Takahara **(Director of NTT Network Innovation Laboratories)** *"Programmable Network"*

Keynote III

Thursday, January 22, 2015, 9:00-9:50

Noriko Arai **(Professor of Information and Society Research Division, National Institute of Informatics)** *"When and how will an AI be smart enough to design?"*

Special Sessions

1S: (Presentation + Poster Discussion) University Design Contest
Tuesday, January 20, 2015, 10:20-13:40

2S: (Invited Talks) Internet of Things
Tuesday, January 20, 2015, 13:50-15:30

3S: (Invited Talks) New Challenges and Solutions in Nanometer Physical Design
Tuesday, January 20, 2015, 15:50-17:30

4S: (Invited Talks) Machine Learning in EDA: Promises and Challenges in Selected Applications
Wednesday, January 21, 2015, 10:15-12:20

7S: (Invited Talks) The Future of Emerging ReRAM Technology
Thursday, January 22, 2015, 10:15-12:20

9B: (Invited Talks) System-Level Designs and Tools for Multicore Systems
Thursday, January 22, 2015, 15:50-17:30

Designers' Forum

5S: (Oral Session) Car Electronics
Wednesday, January 21, 2015, 13:50-15:30

6S: (Panel Discussion) Challenges in the Era of Big-Data Computing
Wednesday, January 21, 2015, 15:50-17:30

8S: (Oral Session) Technology Trend toward 8K Era
Thursday, January 22, 2015, 13:50-15:30

9S: (Panel Discussion) IP base SoC design and IP design innovation
Thursday, January 22, 2015, 15:50-17:30

Tutorials

ASP-DAC 2015 offers attendees a set of two-hour intense introductions to specific topics. Each tutorial will be presented twice a day to allow attendees to cover multiple topics. If you register for tutorials, you have the option to select three out of the six topics.

Tutorial-1: Ultra-low power ultra-low voltage design techniques in Fully Depleted SOI technologies
Monday, January 19, 2015, 9:30-11:30, 13:00-15:00
Organizer:
Andreia Cathelin (STMicroelectronics)
Speakers:
Giorgio Cesana (STMicroelectronics)
Edith Beigné (CEA-Leti)
Nobuyuki Sugii (LEAP)

Tutorial-2: Leading-Edge Lithography and TCAD
Monday, January 19, 2015, 9:30-11:30, 13:00-15:00
Organizer:
Shigeki Nojima (Toshiba)
Speakers:
Seiji Nagahara (Tokyo Electron)
Tomoyuki Matsuyama (Nikon)
Shigyo Naoyuki (Toshiba)

Tutorial-3: Normally-Off Computing: Synergy of New Non-Volatile Memories and Aggressive Power Management
Monday, January 19, 2015, 9:30-11:30, 15:30-17:30
Organizers:
Hiroshi Nakamura (The University of Tokyo)
Takashi Nakada (The University of Tokyo)
Speakers:
Takashi Nakada (The University of Tokyo)
Shinobu Fujita (Toshiba Corporate R&D Center)

Tutorial-4: Hardware Trust in VLSI Design and Implementations
Monday, January 19, 2015, 9:30-11:30, 15:30-17:30
Organizers:
Kazuo Sakiyama (The University of Electro-Communications)
Makoto Nagata (Kobe University)
Speakers:
Patrick Schaumont (Virginia Tech, US)
Swarup Bhunia (Case Western Reserve University, US)
Kazuo Sakiyama (The University of Electro-Communications, JP)
Makoto Nagata (Kobe University, JP)

Tutorial-5: High-Level Synthesis for FPGAs: From Software to Programmable Hardware
Monday, January 19, 2015, 13:00-15:00, 15:30-17:30
Organizer:
Jason Anderson (University of Toronto)
Speakers:
Jason Anderson (University of Toronto)
Ben Carrion Schafer (Hong Kong Polytechnic University)

Tutorial-6: Electronic Design Automation for Nanotechnologies
Monday, January 19, 2015, 13:00-15:00, 15:30-17:30
Organizers:
Pierre-Emmanuel Gaillardon (EPFL)
Giovanni De Micheli (EPFL)
Speakers:
Pierre-Emmanuel Gaillardon (EPFL)
Luca Amaru (EPFL)
Anupam Chattopadhay (Nanyang Technical University)
Subhasish Mitra (Stanford University)

Monday, January 19, 2015

ASP-DAC 2015 offers attendees a set of two-hour intense introductions to specific topics. Each tutorial will be presented twice a day to allow attendees to cover multiple topics. If you register for tutorials, you have the option to select three out of the six topics.

	Room 102	Room 103	Room 104	Room 105
Registration (8:00 -)				
9:30	**Tutorial 1: Ultra-low power ultra-low voltage design techniques in Fully Depleted SOI technologies** Organizer: Andreia Cathelin (STMicroelectronics) Speakers: Giorgio Cesana (STMicroelectronics), Edith Beigné (CEA-Leti), Nobuyuki Sugii (LEAP)	**Tutorial 2: Leading-Edge Lithography and TCAD** Organizer: Shigeki Nojima (Toshiba) Speakers: Seiji Nagahara (Tokyo Electron), Tomoyuki Matsuyama (Nikon), Shigyo Naoyuki (Toshiba)	**Tutorial 3: Normally-Off Computing: Synergy of New Non-Volatile Memories and Aggressive Power Management** Organizers: Hiroshi Nakamura (The University of Tokyo), Takashi Nakada (The University of Tokyo) Speakers: Takashi Nakada (The University of Tokyo), Shinobu Fujita (Toshiba Corporate R&D Center)	**Tutorial 4: Hardware Trust in VLSI Design and Implementations** Organizers: Kazuo Sakiyama (The University of Electro-Communications), Makoto Nagata (Kobe University) Speakers: Patrick Schaumont (Virginia Tech, US), Swarup Bhunia (Case Western Reserve University, US), Kazuo Sakiyama (The University of Electro-Communications, JP), Makoto Nagata (Kobe University, JP)
11:30				
Lunch Break (11:30 - 13:00)				
13:00	**Tutorial 1: Ultra-low power ultra-low voltage design techniques in Fully Depleted SOI technologies** Organizer: Andreia Cathelin (STMicroelectronics) Speakers: Giorgio Cesana (STMicroelectronics), Edith Beigné (CEA-Leti), Nobuyuki Sugii (LEAP)	**Tutorial 2: Leading-Edge Lithography and TCAD** Organizer: Shigeki Nojima (Toshiba) Speakers: Seiji Nagahara (Tokyo Electron), Tomoyuki Matsuyama (Nikon), Shigyo Naoyuki (Toshiba)	**Tutorial 5: High-Level Synthesis for FPGAs: From Software to Programmable Hardware** Organizer: Jason Anderson (University of Toronto) Speakers: Jason Anderson (University of Toronto), Ben Carrion Schafer (Hong Kong Polytechnic University)	**Tutorial 6: Electronic Design Automation for Nanotechnologies** Organizers: Pierre-Emmanuel Gaillardon (EPFL), Giovanni De Micheli (EPFL) Speakers: Pierre-Emmanuel Gaillardon (EPFL), Luca Amaru (EPFL), Anupam Chattopadhay (Nanyang Technical University), Subhasish Mitra (Stanford University)
15:00				
Coffee Break (15:00 - 15:30)				
15:30	**Tutorial 3: Normally-Off Computing: Synergy of New Non-Volatile Memories and Aggressive Power Management** Organizers: Hiroshi Nakamura (The University of Tokyo), Takashi Nakada (The University of Tokyo) Speakers: Takashi Nakada (The University of Tokyo), Shinobu Fujita (Toshiba Corporate R&D Center)	**Tutorial 4: Hardware Trust in VLSI Design and Implementations** Organizers: Kazuo Sakiyama (The University of Electro-Communications), Makoto Nagata (Kobe University) Speakers: Patrick Schaumont (Virginia Tech, US), Swarup Bhunia (Case Western Reserve University, US), Kazuo Sakiyama (The University of Electro-Communications, JP), Makoto Nagata (Kobe University, JP)	**Tutorial 5: High-Level Synthesis for FPGAs: From Software to Programmable Hardware** Organizer: Jason Anderson (University of Toronto) Speakers: Jason Anderson (University of Toronto), Ben Carrion Schafer (Hong Kong Polytechnic University)	**Tutorial 6: Electronic Design Automation for Nanotechnologies** Organizers: Pierre-Emmanuel Gaillardon (EPFL), Giovanni De Micheli (EPFL) Speakers: Pierre-Emmanuel Gaillardon (EPFL), Luca Amaru (EPFL), Anupam Chattopadhay (Nanyang Technical University), Subhasish Mitra (Stanford University)
17:30				
20th Anniversary Reception (18:00 - 19:30) (All participants are welcome.)				

Tuesday, January 20, 2015

Registration (7:00 -)

8:30 **1K: Opening & Keynote 1**

Chair: Kunio Uchiyama (Hitachi)

9:50 Udo Wolz (Bosch, Japan) *"The Required Technologies for Automotive towards 2020"*

Coffee break (9:50 - 10:20)

10:20

1S: University Design Contest

Chairs: Hiroyuki Ito (Tokyo Inst. of Tech., Japan), Noriyuki Miura (Kobe Univ., Japan)

(The titles of the presentations are listed in the next page)

1A: NoCS I (Performance and Fault Tolerance)

Chairs: Yoshinori Takeuchi (Osaka Univ., Japan), TBD ()

1A-1: Leibo Liu, Yu Ren, Chenchen Deng (Tsinghua Univ., China), Jie Han (Univ. of Alberta, Canada), Shouyi Yin, Shaojun Wei (Tsinghua Univ., China) *"A Novel Approach Using a Minimum Cost Maximum Flow Algorithm for Fault-Tolerant Topology Reconfiguration in NoC Architectures"*

1A-2: Peng Wang, Sheng Ma, Zhiying Wang, Hongyi Lu, Chen Li (National Univ. of Defense Tech., China) *"Adaptive Remaining Hop Count Flow Control: Consider the Interaction between Packets"*

1A-3: Takeshi Soga (ISIT Kyushu, JST CREST, Japan), Hiroshi Sasaki, Tomoya Hirao (Kyushu Univ., Japan), Masaaki Kondo (Univ. of Tokyo, Japan), Koji Inoue (Kyushu Univ., Japan) *"A Flexible Hardware Barrier Mechanism for Many-Core Processors"*

1A-4: Lian Zeng, Takahiro Watanabe (Waseda Univ., Japan) *"A Performance Enhanced Dual-Switch Network-on-Chip Architecture"*

1B: Toward Power Efficient Design

Chairs: Kimiyoshi Usami (Shibaura Inst. of Tech., Japan), Masanori Hashimoto (Osaka Univ., Japan)

1B-1: Alireza Shafaei, Shuang Chen, Yanzhi Wang, Massoud Pedram (Univ. of Southern California, U.S.A.) *"A Cross-Layer Framework for Designing and Optimizing Deeply-Scaled FinFET-Based SRAM Cells under Process Variations"*

1B-2: Adam Teman (EPFL, Switzerland), Davide Rossi (UNIBO, Italy), Pascal Meinerzhagen (EPFL, Switzerland), Luca Benini (UNIBO/ETH, Italy), Andreas Burg (EPFL, Switzerland) *"Controlled Placement of Standard Cell Memory Arrays for Improved Density and Low Power in 28nm FD-SOI"*

1B-3: Jun Shiomi, Tohru Ishihara, Hidetoshi Onodera (Kyoto Univ., Japan) *"Microarchitectural-Level Statistical Timing Models for Near-Threshold Circuit Design"*

1B-4: Shengcheng Wang, Farshad Firouzi, Fabian Oboril, Mehdi B. Tahoori (Karlsruhe Inst. of Tech., Germany) *"Stress-Aware P/G TSV Planning in 3D-ICs"*

1C: Modeling and Design Methodologies of Post-silicon Devices

Chairs: Zili Shao (Hong Kong Polytechnic Univ., Hong Kong), Duo Liu (Chongqing Univ., China)

1C-1: Chao Zhang, Guangyu Sun, Weiqi Zhang (Peking Univ., China), Fan Mi, Hai Li (Univ. of Pittsburgh, U.S.A.), Weisheng Zhao (Beihang Univ., China) *"Quantitative Modeling of Racetrack Memory, A Tradeoff among Area, Performance, and Power"*

1C-2: Peng Gu, Boxun Li, Tianqi Tang (Tsinghua Univ., China), Shimeng Yu, Yu Cao (Arizona State Univ., U.S.A.), Yu Wang, Huazhong Yang (Tsinghua Univ., China) *"Technological Exploration of RRAM Crossbar Array For Matrix-Vector Multiplication"*

1C-3: Yang Zheng, Cong Xu (Pennsylvania State Univ., U.S.A.), Yuan Xie (Univ. of California, Santa Barbara, U.S.A.) *"Modeling Framework for Cross-Point Resistive Memory Design Emphasizing Reliability and Variability Issues"*

1C-4: Ching-Yi Huang, Chian-Wei Liu, Chun-Yao Wang (National Tsing Hua Univ., Taiwan), Yung-Chih Chen (Yuan Ze Univ., Taiwan), Suman Datta, Vijaykrishnan Narayanan (Pennsylvania State Univ., U.S.A.) *"A Defect-Aware Approach for Mapping Reconfigurable Single-Electron Transistor Arrays"*

12:00

Lunch Break (12:00 - 13:50)

University LSI Design Contest Poster Presentation [Food will be served] (12:20 - 13:40)

10:20 **1S: University Design Contest**

Chairs: Hiroyuki Ito (Tokyo Inst. of Tech., Japan), Noriyuki Miura (Kobe Univ., Japan)

<Oral Presentation>

1S-1: Dongsheng Yang, Wei Deng, Tomohiro Ueno, Teerachot Siriburanon, Satoshi Kondo, Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan) *"An HDL-Synthesized Gated-Edge-Injection PLL with A Current Output DAC"*

1S-2: Takehiko Amaki, Masanori Hashimoto, Takao Onoye (Osaka Univ., Japan) *"An Oscillator-Based True Random Number Generator with Process and Temperature Tolerance"*

1S-3: Takanori Machida (Univ. of Electro-Communications, Japan), Dai Yamamoto (Fujitsu Labs., Japan), Mitsugu Iwamoto, Kazuo Sakiyama (Univ. of Electro-Communications, Japan) *"Implementation of Double Arbiter PUF and Its Performance Evaluation on FPGA"*

1S-4: Yohei Umeki, Koji Yanagida (Kobe Univ., Japan), Shusuke Yoshimoto (Stanford Univ., U.S.A.), Shintaro Izumi, Masahiko Yoshimoto, Hiroshi Kawaguchi (Kobe Univ., Japan), Koji Tsunoda, Toshihiro Sugii (Low-Power Electronics Association and Project (LEAP), Japan) *"A Negative-Resistance Sense Amplifier for Low-Voltage Operating STT-MRAM"*

1S-5: Nobuaki Kobayashi, Ryusuke Ito, Tadayoshi Enomoto (Chuo Univ., Japan) *"A High Stability, Low Supply Voltage and Low Standby Power Six-Transistor CMOS SRAM"*

1S-6: Xuan-Thuan Nguyen, Cong-Kha Pham (Univ. of Electro-Communications, Japan) *"An Efficient Multi-Port Memory Controller for Multimedia Applications"*

1S-7: Masanori Hashimoto, Dawood Alnajjar, Hiroaki Konoura (Osaka Univ., Japan), Yukio Mitsuyama (Kochi Univ. of Tech., Japan), Hajime Shimada (Nagoya Univ., Japan), Kazutoshi Kobayashi (Kyoto Inst. of Tech., Japan), Hiroyuki Kanbara (ASTEM, Japan), Hiroyuki Ochi (Ritsumeikan Univ., Japan), Takashi Imagawa (Kyoto Univ., Japan), Kazutoshi Wakabayashi (NEC, Japan), Takao Onoye (Osaka Univ., Japan), Hidetoshi Onodera (Kyoto Univ., Japan) *"Reliability-Configurable Mixed-Grained Reconfigurable Array Compatible with High-Level Synthesis"*

1S-8: Yozaburo Nakai, Shintaro Izumi, Ken Yamashita, Masanao Nakano, Hiroshi Kawaguchi, Masahiko Yoshimoto (Kobe Univ., Japan) *"A 14μA ECG Processor with Noise Tolerant Heart Rate Extractor and FeRAM for Wearable Healthcare Systems"*

1S-9: Xiaowei Ren (Xi'an Jiaotong Univ., China) *"A 128-Way FPGA Platform for the Acceleration of KLMS Algorithm"*

1S-10: Xiaowei Ren (Xi'an Jiaotong Univ., China) *"A Real-Time Permutation Entropy Computation for EEG Signals"*

1S-11: Jiang Yu, Geng Liu, Xin Zhang, Pengju Ren (Xi'an Jiaotong Univ., China) *"A High Efficient Hardware Architecture for Multiview 3DTV"*

1S-12: Hsiao-Wei Chien, Jyun-Long Lai, Chao-Chieh Wu, Chih-Tsun Huang, Ting-Shuo Hsu, Jing-Jia Liou (National Tsing Hua Univ., Taiwan) *"Design of A Scalable Many-Core Processor for Embedded Applications"*

1S-13: Daisuke Fujimoto, Noriyuki Miura (Kobe Univ., Japan), Yu-ichi Hayashi, Naofumi Homma, Takafumi Aoki (Tohoku Univ., Japan), Makoto Nagata (Kobe Univ., Japan) *"A DPA/DEMA/LEMA-Resistant AES Cryptographic Processor with Supply-Current Equalizer and Micro EM Probe Sensor"*

1S-14: Xiwei Huang, Jing Guo, Mei Yan, Hao Yu (Nanyang Technological Univ., Singapore) *"A 64x64 1200fps Dual-Mode CMOS Ion-Image Sensor for Accurate DNA Sequencing"*

1S-16: Toshihiro Ozaki, Tetsuya Hirose, Takahiro Nagai, Keishi Tsubaki, Nobutaka Kuroki, Masahiro Numa (Kobe Univ., Japan) *"A 0.21-V Minimum Input, 73.6% Maximum Efficiency, Fully Integrated 3-Terminal Voltage Converter with MPPT for Low-Voltage Energy Harvesters"*

1S-17: Junki Hashiba, Toru Kawajiri, Yuya Hasegawa, Hiroki Ishikuro (Keio Univ., Japan) *"Dual-Output Wireless Power Delivery System for Small Size Large Volume Wireless Memory Card"*

1S-18: Daisuke Kanemoto (Univ. of Yamanashi, Japan), Keigo Oshiro, Keiji Yoshida, Haruichi Kanaya (Kyushu Univ., Japan) *"A Tri-Level 50MS/s 10-bit Capacitive-DAC for Bluetooth Applications"*

1S-19: Aravind Tharayil Narayanan, Wei Deng, Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan) *"A Tail-Current Modulated VCO with Adaptive-Bias Scheme"*

1S-20: Jili Zhang, Chenluan Wang, Shengxi Diao, Fujiang Lin (Univ. of Science and Tech. of China, China) *"A Low-Power VCO Based ADC with Asynchronous Sigma-Delta Modulator in 65nm CMOS"*

1S-21: Sho Ikeda, Sang_yeop Lee, Shin Yonezawa, Yiming Fang, Motohiro Takayasu, Taisuke Hamada, Yosuke Ishikawa, Hiroyuki Ito, Noboru Ishihara, Kazuya Masu (Tokyo Inst. of Tech., Japan) *"A 0.5-V 5.8-GHz Low-Power Asymmetrical QPSK/OOK Transceiver for Wireless Sensor Network"*

1S-22: Teerachot Siriburanon, Tomohiro Ueno, Kento Kimura, Satoshi Kondo, Wei Deng, Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan) *"A 58.3-to-65.4 GHz 34.2 mW Sub-Harmonically Injection-Locked PLL with a Sub-Sampling Phase Detection"*

1S-23: Akira Okada, Abdul Raziz Junaidi, Yasuhiro Take, Atsutake Kosuge, Tadahiro Kuroda (Keio Univ., Japan) *"Circuit and Package Design for 44GBs DRAMSoC Interface"*

1S-24: Li-Chung Hsu, Yasuhiro Take, Atsutake Kosuge, So Hasegawa, Junichiro Kadamoto, Tadahiro Kuroda (Keio Univ., Japan) *"Design and Analysis for ThruChip Design for Manufacturing (DFM)"*

12:00

Lunch Break (12:00 - 13:50)

University LSI Design Contest Poster Presentation [Food will be served] (12:20 - 13:40)

13:50

2S: (Special Session) Internet of Things	2A: NoCS II (Power and Emerging Technology)	2B: Design Automation for Tomorrow's Circuit Technologies	2C: Emerging Applications
Chair: Li Shang (Univ. of Colorado Boulder, U.S.A.)	Chairs: TBD (), TBD ()	Chairs: Anupam Chattopadhyay (RWTH Aachen Univ., Germany), Shigeru Yamashita (Ritsumeikan Univ.)	Chairs: Juinn-Dar Huang (National Chiao Tung Univ., Taiwan), TBD ()
2S-1: Hyung Gyu Lee (Daegu Univ., Republic of Korea), Naehyuck Chang (KAIST, Republic of Korea) *"Powering the IoT: Storage-Less and Converter-Less Energy Harvesting"*	**2A-1:** Hang Lu (Univ. of Chinese Academy of Sciences, China), Guihai Yan, Yinhe Han, Ying Wang, Xiaowei Li (Chinese Academy of Sciences, China) *"ShuttleNoC: Boosting On-Chip Communication Efficiency by Enabling Localized Power Adaptation"*	**2B-1:** Shuangchen Li (Univ. of California, Santa Barbara, U.S.A.), Ang Li, Yongpan Liu (Tsinghua Univ., China), Yuan Xie (Univ. of California, Santa Barbara, U.S.A.), Huazhong Yang (Tsinghua Univ., China) *"Nonvolatile Memory Allocation and Hierarchy Optimization for High-Level Synthesis"*	**2C-1:** Zipeng Li (Duke Univ., U.S.A.), Tsung-Yi Ho (National Chiao Tung Univ., Taiwan), Krishnendu Chakrabarty (Duke Univ., U.S.A.) *"Design and Optimization of 3D Digital Microfluidic Biochips for the Polymerase Chain Reaction"*
2S-2: Shao-Yi Chien, Wei-Kai Chan, Yu-Hsiang Tseng (National Taiwan Univ., Taiwan), Chia-Han Lee (Academia Sinica, Taiwan), V. Srinivasa Somayazulu, Yen-Kuang Chen (Intel, U.S.A.) *"Distributed Computing in IoT: System-on-a-Chip for Smart Cameras as an Example"*	**2A-2:** Hui LI, Sébastien Le Beux (Lyon Institute of Nanotechnology, France), Gabriela Nicolescu (Ecole Polytechnique de Montréal, Canada), Ian O'Connor (Lyon Institute of Nanotechnology, France) *"Energy-Efficient Optical Crossbars on Chip with Multi-Layer Deposited Silicon"*	**2B-2:** Robert Wille, Oliver Keszocze, Clemens Hopfmuller, Rolf Drechsler (Univ. of Bremen, Germany) *"Reverse BDD-Based Synthesis for Splitter-Free Optical Circuits"*	**2C-2:** Li-xue Xia, Rong Luo, Bin Zhao, Yu Wang, Hua-zhong Yang (Tsinghua Univ., China) *"An Accurate and Low Cost PM¡sub¿2.5¡/sub¿ Estimation Method Based on Artificial Neural Network"*
2S-3: James Williamson, Qi Liu, Wyatt Morhman, Kun Li, Fenglong Lu (Univ. of Colorado Boulder, U.S.A.), Robert P. Dick (Univ. of Michigan, U.S.A.), Li Shang (Univ. of Colorado Boulder, U.S.A.) *"Data Sensing and Analysis: The Challenge for Wearables"*	**2A-3:** Julian Hilgemberg Pontes, Pascal Vivet, Yvain Thonnart (CEA/LETI, France) *"Two-Phase Protocol Converters for 3D Asynchronous 1-of-n Data Links"*	**2B-3:** Aaron Lye, Robert Wille, Rolf Drechsler (Univ. of Bremen, Germany) *"Determining the Minimal Number of SWAP Gates for Multi-Dimensional Nearest Neighbor Quantum Circuits"*	**2C-3:** Zhi Hu, Yibo Fan, Xiaoyang Zeng (Fudan Univ., China) *"Iterative Disparity Voting Based Stereo Matching Algorithm and Its Hardware Implementation"*
	2A-4: Xiaohang Wang, Tengfei Wang (Chinese Academy of Sciences, China), Terrence Mak (Chinese Univ. of Hong Kong, China), Mei Yang, Yingtao Jiang (Univ. of Nevada, Las Vegas, U.S.A.), Masoud Daneshtalab (Univ. of Turku, Finland) *"Fine-Grained Runtime Power Budgeting for Networks-on-Chip"*		**2C-4:** Yu-Wei Wu (National Cheng Kung Univ., Taiwan), Yiyu Shi (Missouri Univ. of Science and Tech., U.S.A.), Sudip Roy (National Cheng Kung Univ., Taiwan), Tsung-Yi Ho (National Chiao Tung Univ., Taiwan) *"Obstacle-Avoiding Wind Turbine Placement for Power-Loss and Wake-Effect Optimization"*

15:30

Coffee break (15:30 - 15:50)

15:50

3S: (Special Session) New Challenges and Solutions in Nanometer Physical Design

Chair: Mark Po-Hung Lin (National Chung Cheng Univ., Taiwan)

3S-1: Haitong Tian, Martin D. F. Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.) *"An Efficient Linear Time Triple Patterning Solver"*

3S-2: Tiago Reimann (Univ. Federal do Rio Grande do Sul, Brazil), Cliff Sze (IBM, U.S.A.), Ricardo Reis (Univ. Federal do Rio Grande do Sul, Brazil) *"Gate Sizing and Threshold Voltage Assignment for High Performance Microprocessor Designs"*

3S-3: Yasuhiro Takashima (Univ. of Kitakyushu, Japan) *"Analytical Placement for Rectilinear Blocks"*

3S-4: Eric Jia-Wei Fang, Terry Chi-Jih Shih, Darton Shen-Yu Huang (MediaTek, Taiwan) *"IR to Routing Challenge and Solution for Interposer-Based Design"*

17:30

3A: Circuits for Performance and Reliability

Chairs: Sri Parameswaran (Univ. of New South Wales, Australia), TBD ()

3A-3: Anteneh Gebregiorgis (TU Delft, Netherlands), Mojtaba Ebrahimi, Saman Kiamehr, Fabian Oboril (Karlsruhe Inst. of Tech., Germany), Said Hamdioui (TU Delft, Netherlands), Mehdi Tahoori (Karlsruhe Inst. of Tech., Germany) *"Aging Mitigation in Memory Arrays Using Self-Controlled Bit-Flipping Technique"*

3A-4: Chang Liu, Xinghua Yang, Fei Qiao, Qi Wei, Huazhong Yang (Tsinghua Univ., China) *"Design Methodology for Approximate Accumulator Based on Statistical Error Model"*

3B: Frontiers in Logic Synthesis

Chairs: Robert Wille (Univ. of Bremen, Germany), Yuko Hara-Azumi (Tokyo Inst. of Tech.)

3B-1: Luca Amaru (Integrated Systems Laboratory - EPFL, Switzerland), Gage Hills (Stanford Univ., U.S.A.), Pierre-Emmanuel Gaillardon (Integrated Systems Laboratory - EPFL, Switzerland), Subhasish Mitra (Stanford Univ., U.S.A.), Giovanni De Micheli (Integrated Systems Laboratory - EPFL, Switzerland) *"Multiple Independent Gate FETs: How Many Gates Do We Need?"*

3B-2: Subhendu Roy (Univ. of Texas, Austin, U.S.A.), Mihir Choudhury, Ruchir Puri (IBM, U.S.A.), David Z Pan (Univ. of Texas, Austin, U.S.A.) *"Polynomial Time Algorithm for Area and Power Efficient Adder Synthesis in High-Performance Designs"*

3B-3: Yusuke Matsunaga (Kyushu Univ., Japan) *"Accelerating SAT-Based Boolean Matching for Heterogeneous FPGAs Using One-Hot Encoding and CEGAR Technique"*

3C: Energy Optimization for Electric Vehicles and Smart Grids

Chairs: Hideki Takase (Kyoto Univ., Japan), Yongpan Liu (Tsinghua Univ., China)

3C-1: Ji Li, Yanzhi Wang, Xue Lin, Shahin Nazarian, Massoud Pedram (USC, U.S.A.) *"Negotiation-Based Task Scheduling and Storage Control Algorithm to Minimize User's Electric Bills under Dynamic Prices"*

3C-2: Matthias Kauer, Swaminathan Narayanaswamy, Sebastian Steinhorst, Martin Lukasiewycz (TUM CREATE, Singapore), Samarjit Chakraborty (TU Munich, Germany) *"Many-to-Many Active Cell Balancing Strategy Design"*

3C-3: Ta-Yang Huang, Chia-Jui Chang (National Cheng Kung Univ., Taiwan), Chung-Wei Lin (Univ. of California, Berkeley, U.S.A.), Sudip Roy (National Cheng Kung Univ., Taiwan), Tsung-Yi Ho (National Chiao Tung Univ., Taiwan) *"Intra-Vehicle Network Routing Algorithm for Weight and Wireless Transmit Power Minimization"*

3C-4: Yusuke Sakumoto (Tokyo Metropolitan Univ., Japan), Ittetsu Taniguchi (Ritsumeikan Univ., Japan) *"An Autonomous Decentralized Mechanism for Energy Interchanges with Accelerated Diffusion Based on MCMC"*

ACM SIGDA Student Research Forum at ASP-DAC 2015 [Food will be served] (18:00 - 20:00)

(The title of the posters are listed in the next page)

18:00 **ACM SIGDA Student Research Forum at ASP-DAC2015**

1: Ahmed Awad (Tokyo Institute of Technology) "*A Fast Process Variation and Pattern Fidelity Aware Mask Optimization Algorithm.*"
2: Alireza Shafaei (University of Southern California) "*Energy Efficient Cache Memories in Deeply-Scaled Technologies*"
3: Boxun Li (Tsinghua University) "*Energy Efficient System Design for Neural Networks*"
4: Ching-Yi Huang (National Tsing Hua University) "*Analysis and Power Optimization for Probabilistic Boolean Circuits*"
5: Donkyu Baek (KAIST) "*Power Consumption Characterization, Modeling and Estimation of Electric Vehicles*"
6: Hayato Mashiko (University of Aizu) "*A Tuning Method of Programmable Delay Element with an Ordered Finite Set of Delays for Yield Improvement*"
7: Jaemin Kim (Seoul National University, KAIST) "*Reconfigurable PV Powered Full Electric Vehicles*"
8: Jan Malburg (University of Bremen) "*Feature Localization and Design Understanding for Hardware Designs*"
9: Jinho Lee (Seoul National University) "*Designing Efficient On-chip Networks: Mapping, Management, and Routing*"
10: Keitaro Takizawa (University of Aizu) "*Development of A Design Environment for Asynchronous Circuits with Bundled-data Implementation on FPGAs*"
11: Mengying Zhao (City University of Hong Kong) "*Endurance and Energy Aware Optimizations for Phase Change Memory*"
12: Renhai Chen (Hong Kong Polytechnic University) "*vFlash: Unied Non-Volatile Memory and NAND Flash Memory Architecture in Smartphones*"
13: Rickard Ewetz (Purdue University) "*Robust Clock Network Synthesis*"
14: Seongbo Shim (KAIST) "*Physical Design Optimization Using Lithography Defect Probability*"
15: Sergej Deutsch (Duke University) "*Contactless Pre-Bond TSV Test and Diagnosis Using Ring Oscillators and Multiple Voltage Levels*"
16: Shengcheng Wang (Karlsruhe Institute of Technology) "*Multi-objective P/G TSV Planning in 3D-ICs*"
17: Shoichi Iizuka (Osaka University) "*Fast Error Rate Estimation with Stochastic Modeling for Adaptive Speed Controlled Circuit*"
18: Trung Anh Dinh (Ritsumeikan University,) "*Design and Optimization for Digital Microfluidic Biochips*"
19: Wan-Yu Wen (National Tsing Hua University) "*Learning Mechanisms with High Power Efficiency Design*"
20: Xiang Chen (University of Pittsburgh) "*Demystify Energy Usage in Smartphones*"
21: Xiao Sheng (Tsinghua University) "*A High-Efficiency Dual-Channel Photovoltaic Power System for Nonvolatile Sensor Nodes*"
22: Xiao Zhu (Chongqing University) "*Understanding Swapping in Mobile Systems*"
23: Xiwei Huang (Nanyang Technological University) "*A Contact-Imaging Based Microfluidic Cytometer with Machine-Learning for Single-Frame Super-Resolution Processing*"
24: Zaid Al-bayati (McGill University) "*Model-based Design for Mixed-Criticality Systems*"

20:00

Wednesday, January 21, 2015

Registration (7:30 -)

9:00 **2K: Keynote 2**

Chair: Kunio Uchiyama (Hitachi)

Atsushi Takahara (NTT, Japan) *"Programmable Network"*

9:50

Coffee break (9:50 - 10:15)

10:15

4S: (Special Session) Machine Learning in EDA: Promises and Challenges in Selected Applications

Chair: Li-C. Wang (Univ. of California, Santa Barbara, U.S.A.)

4S-1: Bei Yu, David Z. Pan (Univ. of Texas, Austin, U.S.A.), Tetsuaki Matsunawa (Toshiba, Japan), Xuan Zeng (Fudan Univ., China) *"Machine Learning and Pattern Matching in Physical Design"*

4S-2: Fangming Ye, Krishnendu Chakrabarty (Duke Univ., U.S.A.), Zhaobo Zhang, Xinli Gu (Huawei Technologies, U.S.A.) *"Self-Learning and Adaptive Board-Level Functional Fault Diagnosis"*

4S-3: Shupeng Sun, Xin Li (Carnegie Mellon Univ., U.S.A.) *"Fast Statistical Analysis of Rare Circuit Failure Events for Memory Circuits in High-Dimensional Variation Space"*

4S-4: Li-C. Wang (Univ. of California, Santa Barbara, U.S.A.) *"Data Mining in Functional Test Content Optimization"*

4A: Efficient NVM Management, from Register to Disk

Chairs: kyoungwoo Lee (Yonsei Univ., Republic of Korea), TBD ()

4A-1: Mimi Xie, Chen Pan, Jingtong Hu (Oklahoma State Univ., U.S.A.), Chengmo Yang (Univ. of Delaware, U.S.A.), Yiran Chen (Univ. of Pittsburgh, U.S.A.) *"Checkpoint-Aware Instruction Scheduling for Non-volatile Processor with Multiple Functional Units"*

4A-2: Linbo Long, Duo Liu, Xiao Zhu, Kan Zhong (Chongqing Univ., China), Zili Shao (Hong Kong Polytechnic Univ., Hong Kong), Edwin Sha (Chongqing Univ., China) *"Balloonfish: Utilizing Morphable Resistive Memory in Mobile Virtualization"*

4A-3: Yanbin Li, Xin Li, Lei Ju, Zhiping Jia (Shandong Univ., China) *"A Three-Stage-Write Scheme with Flip-Bit for PCM Main Memory"*

4A-4: Min Huang (Harbin Inst. of Tech., China), Yi Wang (Shenzhen Univ., China), Zhaoqing Liu, Liyan Qiao (Harbin Inst. of Tech., China), Zili Shao (Hong Kong Polytechnic Univ., Hong Kong) *"A Garbage Collection Aware Stripping Method for Solid-State Drives"*

4A-5: Renhai Chen (Hong Kong Polytechnic Univ., Hong Kong), Yi Wang (Shenzhen Univ., China), Jingtong Hu (Oklahoma State Univ., U.S.A.), Duo Liu (Chongqing Univ., China), Zili Shao (Hong Kong Polytechnic Univ., Hong Kong), Yong Guan (Capital Normal Univ., China) *"Unified Non-Volatile Memory and NAND Flash Memory Architecture in Smartphones"*

4B: Robust Timing, and P/G Modeling and Design

Chairs: Ray Cheung (City Univ. of Hong Kong, Hong Kong), Fan Yang (Fudan Univ., China)

4B-1: Palkesh Jain (Qualcomm India Pvt, India), Sachin S. Sapatnekar (Univ. of Minnesota, U.S.A.), Jordi Cortadella (Univ. Politècnica de Catalunya, Spain) *"A Retargetable and Accurate Methodology for Logic-IP-Internal Electromigration Assessment"*

4B-2: Hai-Bao Chen, Sheldon X.-D. Tan, Xin Huang (Univ. of California, Riverside, U.S.A.), Valeriy Sukharev (Mentor Graphics, U.S.A.) *"New Electromigration Modeling and Analysis Considering Time-Varying Temperature and Current Densities"*

4B-3: Zahi Moudallal, Farid N Najm (Univ. of Toronto, Canada) *"Generating Circuit Current Constraints to Guarantee Power Grid Safety"*

4B-4: Aadithya Karthik (UC Berkeley, U.S.A.), Sayak Ray (Princeton Univ., U.S.A.), Jaijeet Roychowdhury (UC Berkeley, U.S.A.) *"BEE: Predicting Realistic Worst Case and Stochastic Eye Diagrams by Accounting for Correlated Bitstreams and Coding Strategies"*

4B-5: Chung-Hao Tsai, Wai-Kei Mak (National Tsing Hua Univ., Taiwan) *"A Fast Parallel Approach for Common Path Pessimism Removal"*

4C: New Issues in Placement and Routing

Chairs: Shigetoshi Nakatake (Univ. of Kitakyushu, Japan), TBD ()

4C-1: Chau-Chin Huang, Chien-Hsiung Chiou, Kai-Han Tseng, Yao-Wen Chang (National Taiwan Univ., Taiwan) *"Detailed-Routing-Driven Analytical Standard-Cell Placement"*

4C-2: Shih-Ying Liu (NCTU, Taiwan), Tung-Chieh Chen (Synopsys, Taiwan), Hung-Ming Chen (NCTU, Taiwan) *"An Approach to Anchoring and Placing High Performance Custom Digital Designs"*

4C-3: Po-Ya Hsu, Yao-Wen Chang (National Taiwan Univ., Taiwan) *"Non-Stitch Triple Patterning-Aware Routing Based on Conflict Graph Pre-Coloring"*

4C-4: Shao-Yun Fang (National Taiwan Univ. of Science and Tech., Taiwan) *"Cut Mask Optimization with Wire Planning in Self-Aligned Multiple Patterning Full-Chip Routing"*

4C-5: Ran Zhang, Tieyuan Pan, Li Zhu, Takahiro Watanabe (Waseda Univ., Japan) *"A Length Matching Routing Method for Disordered Pins in PCB Design"*

12:20

Lunch Break (12:20 - 13:50)

13:50

5S: (Designers' Forum) Car Electronics	**5A: Optimization and Exploration for Caches**	**5B: CAD for Analog/RF/Mixed-Signal Design**	**5C: Next-Generation Clock Network Synthesis**
Organizers: Shinichi Shibahara (Renesas Electronics, Japan), Chair: Koji Inoue (Kyushu Univ., Japan)	Chairs: Hiroyuki Tomiyama (Ritsumeikan Univ., Japan), Lin Meng (Ritsumeikan Univ., Japan)	Chairs: Sheldon Tan (Univ. of California, Riverside, U.S.A.), Mark Po-Hung Lin (National Chung Cheng Univ., Taiwan)	Chairs: Atsushi Takahashi (Tokyo Inst. of Tech.), David Z. Pan (Univ. of Texas, Austin, U.S.A.)
5S-1: Hidekazu Nishimura (Keio Univ., Japan) *"Systems Modeling for Additional Development in Automotive E/E Architecture"*	**5A-1:** Haifeng Xu (Univ. of Pittsburgh, U.S.A.), Yong Li (VMware, U.S.A.), Rami Melhem, Alex K. Jones (Univ. of Pittsburgh, U.S.A.) *"Multilane Racetrack Caches: Improving Efficiency Through Compression and Independent Shifting"*	**5B-1:** Ying-Chih Wang, Shihui Yin, Minhee Jun, Xin Li, Larry Pileggi, Tamal Mukherjee, Rohit Negi (Carnegie Mellon Univ., U.S.A.) *"Accurate Passivity-Enforced Macromodeling for RF Circuits via Iterative Zero/Pole Update Based on Measurement Data"*	**5C-1:** Juyeon Kim, Taewhan Kim (Seoul National Univ., Republic of Korea) *"Useful Clock Skew Scheduling Using Adjustable Delay Buffers in Multi-Power Mode Designs"*
5S-2: Nau Ozaki, Masato Uchiyama, Yasuki Tanabe, Shuichi Miyazaki, Takaaki Sawada, Takanori Tamai, Moriyasu Banno (Toshiba, Japan) *"Implementation and Evaluation of Image Recognition Algorithm for An Intelligent Vehicle using Heterogeneous Multi-Core SoC"*	**5A-2:** Zimeng Zhou, Lei Ju, Zhiping Jia, Xin Li (Shandong Univ., China) *"Managing Hybrid On-Chip Scratchpad and Cache Memories for Multi-Tasking Embedded Systems"*	**5B-2:** Volker Meyer zu Bexten, Markus Tristl (Infineon Technologies AG, Germany), Goeran Jerke (Robert Bosch GmbH, Germany), Hartmut Marquardt (Mentor Graphics, Germany), Dina Medhat (Mentor Graphics, Egypt) *"Physical Verification Flow for Hierarchical Analog IC Design Constraints"*	**5C-2:** Rickard Ewetz (Purdue Univ., U.S.A.), Shankarshana Janarthanan (NVIDIA, U.S.A.), Cheng-Kok Koh (Purdue Univ., U.S.A.) *"Fast Clock Skew Scheduling Based on Sparse-Graph Algorithms"*
5S-3: Khalid Hussein, Akira Fujita, Katsumi Sato (Mitsubishi Electric, Japan) *"Trend in Power Devices for Electric and Hybrid Electric Vehicles"*	**5A-3:** Guantao Liu, Tim Schmidt, Rainer Doemer (Univ. of California, Irvine, U.S.A.), Ajit Dingankar, Desmond Kirkpatrick (Intel, U.S.A.) *"Optimizing Thread-to-Core Mapping on Manycore Platforms with Distributed Tag Directories"*	**5B-3:** Zhijian Pan, Chuan Qin, Zuochang Ye, Yan Wang (Tsinghua Univ., China) *"Automatic Design for Analog/RF Front-End System in 802.11ac Receiver"*	**5C-3:** Wulong Liu (Tsinghua Univ., China), Guoqing Chen (Research Lab, Advanced Micro Devices, China), Yu Wang, Huazhong Yang (Tsinghua Univ., China) *"Modeling and Optimization of Low Power Resonant Clock Mesh"*
	5A-4: Mohammad Shihabul Haque, Ang Li (National Univ. of Singapore, Singapore), Qingsong Wei (Data Storage Institute, Singapore), Akash Kumar (National Univ. of Singapore, Singapore) *"Accelerating Non-Volatile/Hybrid Processor Cache Design Space Exploration for Application Specific Embedded Systems"*	**5B-4:** Qicheng Huang, Xiao Li, Fan Yang, Xuan Zeng (Fudan Univ., China), Xin Li (Fudan Univ., U.S.A.) *"SIPredict: Efficient Post-Layout Waveform Prediction via System Identification"*	**5C-4:** Seyong Ahn, Minseok Kang (Seoul National Univ., Republic of Korea), Marios Papaefthymiou (Univ. of Michigan, U.S.A.), Taewhan Kim (Seoul National Univ., Republic of Korea) *"Synthesis of Resonant Clock Networks Supporting Dynamic Voltage / Frequency Scaling"*

15:30

Coffee break (15:30 - 15:50)

15:50	**6S: (Designers' Forum) Panel Discussion: Challenges in the Era of Big-Data Computing** Organizers: Koji Inoue (Kyushu Univ., Japan), Moderator: Koichiro Yamashita (Fujitsu Labs., Japan) Panelists: Kento Aida (NII, Japan) Derek Chiou (Microsoft, U.S.A.) Hiroshi Nakamura (Univ. of Tokyo, Japan) Hiroyuki Tanaka (Nippon Telegraph and Telephone, Japan) Iwao Yamazaki (Fujitsu, Japan)	**6A: Optimization Techniques for Non-Volatile Memory based Systems** Chairs: Guangyu Sun (Peking Univ., China), TBD ()	**6B: Test for Higher Quality** Chairs: Tomokazu Yoneda (NAIST, Japan), Stefan Holst (Kyushu Inst. of Tech.)	**6C: Reliability** Chairs: Xuan Zeng (Fudan Univ., China), Martin Wong (UIUC, U.S.A.)
		6A-1: Xiaoxiao Liu, Mengjie Mao, Xiuyuan Bi, Hai Li, Yiran Chen (Univ. of Pittsburgh, U.S.A.) *"An Efficient STT-RAM-Based Register File in GPU Architectures"*	**6B-1:** Songwei Pei, Ye Geng (Beijing Univ. of Chemical Tech., China), Huawei Li (Key Laboratory of Computer System and Architecture, Institute of Computing Technology, China), Jun Liu (Hefei Univ. of Tech., China), Song Jin (North China Electric Power Univ., China) *"Enhanced LCCG: A Novel Test Clock Generation Scheme for Faster-than-at-Speed Delay Testing"*	**6C-1:** Minjie Lv, Hongbin Sun, Jingmin Xin, Nanning Zheng (Xi'an Jiaotong Univ., China) *"Logic-DRAM Co-Design to Efficiently Repair Stacked DRAM With Unused Spares"*
		6A-2: Masashi Tawada, Shinji Kimura, Masao Yanagisawa, Nozomu Togawa (Waseda Univ., Japan) *"A Bit-Write Reduction Method based on Error-Correcting Codes for Non-Volatile Memories"*	**6B-2:** Kuen-Jong Lee, Liang-Che Li, Wen-Hsuan Hsu (National Cheng Kung Univ., Taiwan), Chun-Lung Hsu (ITRI, Taiwan) *"An Efficient 3D-ICs On-chip Test Framework to Embed TSV Testing in Memory BIST"*	**6C-2:** Jiwoo Pak (Cadence Design Systems, U.S.A.), Bei Yu, David Pan (Univ. of Texas, Austin, U.S.A.) *"Electromigration-Aware Redundant via Insertion"*
		6A-3: Mengying Zhao (City Univ. of Hong Kong, Hong Kong), Yuan Xue, Chengmo Yang (Univ. of Delaware, U.S.A.), Chun Jason Xue (City Univ. of Hong Kong, Hong Kong) *"Minimizing MLC PCM Write Energy for Free through Profiling-Based State Remapping"*	**6B-3:** Nima Aghaee, Zebo Peng, Petru Eles (Linköping Univ., Sweden) *"An Integrated Temperature-Cycling Acceleration and Test Technique for 3D Stacked ICs"*	**6C-3:** Yuankai Chen (Synopsys, U.S.A.), Hai Zhou (Northwestern Univ., U.S.A.) *"Synthesis of Resilient Circuits from Guarded Atomic Actions"*
		6A-4: Hoda Aghaei Khouzani, Chengmo Yang (Univ. of Delaware, U.S.A.), Jingtong Hu (Oklahoma State Univ., U.S.A.) *"Improving Performance and Lifetime of DRAM-PCM Hybrid Main Memory through a Proactive Page Allocation Strategy"*	**6B-4:** Sergej Deutsch, Krishnendu Chakrabarty (Duke Univ., U.S.A.) *"Software-Based Test and Diagnosis of SoCs Using Embedded and Wide-I/O DRAM"*	**6C-4:** Yen-Lung Chen (National Central Univ., Taiwan), Wei Wu (Univ. of California, Los Angeles, U.S.A.), Chien-Nan Jimmy Liu (National Central Univ., Taiwan), Lei He (Univ. of California, Los Angeles, U.S.A.) *"Incremental Latin Hypercube Sampling for Lifetime Stochastic Behavioral Modeling of Analog Circuits"*
17:30				
Banquet (18:00 - 20:00)				

Thursday, January 22, 2015

Registration (7:30 -)

9:00 **3K: Keynote 3**

Chair: Kunio Uchiyama (Hitachi)

Noriko Arai (NII, Japan) *"When and How Will an AI Be Smart Enough to Design?"*

9:50

Coffee break (9:50 - 10:15)

10:15

7S: (Special Session) The Future of Emerging ReRAM Technology

Organizers: Guangyu Sun (Peking Univ., China), Yuan Xie (Univ. of California, Santa Barbara, U.S.A.)

7S-1: Amirali Ghofrani, Miguel Lastras, K.-T. Tim Cheng (Univ. of California, Santa Barbara, U.S.A.) *"Toward Large-Scale Access-Transistor-Free Memristive Crossbars"*

7S-2: Meng-Fan Chang, Albert Lee, Chien-Chen Lin (National Tsing Hua Univ., Taiwan), Mon-Shu Ho (National Chung Hsin Univ., Taiwan), Ping-Cheng Chen (I-Shou Univ., Taiwan) *"Read Circuits for Resistive Memory (ReRAM) and Memristor-Based Nonvolatile Logics"*

7S-3: Sung Hyun Jo, Tanmay Kumar, Mehdi Asnaashari, Wei D. Lu, Hagop Nazarian (Crossbar, U.S.A.) *"3D ReRAM with Field Assisted Super-Linear Threshold (FAST) Technology for Super-Dense, Low Power, Low Latency Data Storage Systems"*

7S-4: J. F. Kang, H. T. Li, P. Huang, Z. Chen, B. Gao, X. Y. Liu (Peking Univ., China), Z. Z. Jiang, H.-S. P. Wong (Stanford Univ., U.S.A.) *"Modeling and Design Optimization of RRAM"*

7A: Ensuring the Correctness of System Integration

Chairs: Takeshi Matsumoto (Ishitawa National College of Tech.), Akash Kumar (Natioanl Univ. of Singapore, Singapore)

7A-1: Biao Hu, Kai Huang, Gang Chen, Alois Knoll (Technical Univ. of Muenchen, Germany) *"Evaluation of Runtime Monitoring Methods for Real-Time Event Streams"*

7A-2: Li-chun Chen (Ambarella, Taiwan), Hsin-I Wu, Ren-Song Tsay (National Tsing Hua Univ., Taiwan) *"Automatic Timing-Coherent Transactor Generation for Mixed-Level Simulations"*

7A-3: Hsuan-Ming Chou, Hong-Chang Wu, Yi-Chiao Chen, Jean Tsao, Shih-Chieh Chang (National Tsing Hua Univ., Taiwan) *"Hybrid Coverage Assertions for Efficient Coverage Analysis Across Simulation and Emulation Environments"*

7A-4: Luis Gabriel Murillo, Robert Lajos Buecs, Daniel Hincapie, Rainer Leupers, Gerd Ascheid (RWTH Aachen Univ., Germany) *"SWAT: Assertion-Based Debugging of Concurrency Issues at System Level"*

7A-5: Che-Wei Chang, Rainer Doemer (Univ. of California, Irvine, U.S.A.) *"Communication Protocol Analysis of Transaction-Level Models Using Satisfiability Modulo Theories"*

7B: Orchestrating Tasks, Cores, and Communication

Chairs: Zili Shao (Hong Kong Polytechnic Univ., Hong Kong), Masanori Hashimoto (Osaka Univ., Japan)

7B-1: Laura A Rozo Duque, Chengmo Yang (Univ. of Delaware, U.S.A.) *"Guiding Fault-Driven Runtime Adaption in Multicore Systems through Pre-Optimized Reliability-Aware Task Schedules"*

7B-2: Cheng Tan, Thannirmalai Somu Muthukaruppan, Tulika Mitra (National Univ. of Singapore, Singapore), Lei Ju (Shandong Univ., China) *"Approximation-Aware Scheduling on Heterogeneous Multi-Core Architectures"*

7B-3: Martin Becker (Tech. Univ. of Munich, Germany), Alejandro Masrur (Software Technology for Embedded Systems, Technical Univ. Chemnitz, Germany), Samarjit Chakraborty (Tech. Univ. of Munich, Germany) *"Composing Real-Time Applications from Communicating Black-Box Components"*

7B-4: Zaid Al-bayati (McGill Univ., Canada), Qingling Zhao (Zhejiang Univ., China), Ahmed Youssef, Haibo Zeng (McGill Univ., Canada), Zonghua Gu (Zhejiang Univ., China) *"Enhanced Partitioned Scheduling of Mixed-Criticality Systems on Multicore Platforms"*

7B-5: Jiaxing Zhang, Sanyuan Tang, Gunar Schirner (Northeastern Univ., U.S.A.) *"Reducing Dynamic Dispatch Overhead (DDO) of SLDL-Synthesized Embedded Software"*

7C: Design for Manufacturability

Chairs: Shigeki Nojima (Toshiba, Japan), Eric J.-W. Fang (MediaTek, Taiwan)

7C-1: Zigang Xiao, Yuelin Du, Martin D.F. Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.), He Yi, H.-S. Philip Wong (Stanford Univ., U.S.A.), Hongbo Zhang (Synopsys, U.S.A.) *"Contact Pitch and Location Prediction for Directed Self-Assembly Template Verification"*

7C-2: Yunfeng Yang, Wai-Shing Luk (Fudan Univ., China), Hai Zhou (Northwestern Univ., U.S.A.), Changhao Yan, Xuan Zeng, Dian Zhou (Fudan Univ., China) *"Layout Decomposition Co-Optimization for Hybrid E-Beam and Multiple Patterning Lithography"*

7C-3: Daifeng Guo, Yuelin Du, Martin D.F. Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.) *"Polynomial Time Optimal Algorithm for Stencil Row Planning in E-Beam Lithography"*

7C-4: Yukihide Kohira (Univ. of Aizu, Japan), Tomomi Matsui (Tokyo Inst. of Tech., Japan), Yoko Yokoyama, Chikaaki Kodama (Toshiba, Japan), Atsushi Takahashi (Tokyo Inst. of Tech., Japan), Shigeki Nojima, Satoshi Tanaka (Toshiba, Japan) *"Fast Mask Assignment Using Positive Semidefinite Relaxation in LELECUT Triple Patterning Lithography"*

7C-5: Shao-Yun Fang (National Taiwan Univ. of Science and Tech., Taiwan), Yi-Shu Tai, Yao-Wen Chang (National Taiwan Univ., Taiwan) *"Layout Decomposition for Spacer-is-Metal (SIM) Self-Aligned Double Patterning"*

12:20

Lunch Break (12:20 - 13:50)

13:50

8S: (Designers' Forum) Technology Trend toward 8K Era

Organizers: Hiroe Iwasaki (NTT, Japan), Chair: Masaitsu Nakajima (Panasonic, Japan)

8S-1: Keiya Motohashi (NetTV Forum, Japan) *"The Prospects of Next Generation Television - Japan's Initiative to 2020 -"*

8S-2: Takeshi Kumakura (SHARP, Japan) *"8K LCD : Technologies and Challenges toward the Realization of SUPER Hi-VISION TV"*

8S-3: Daisuke Murakami, Yuki Soga, Daisuke Imoto, Yoshiharu Watanabe, Takashi Yamada (Panasonic, Japan) *"The World's 1st Complete-4K SoC Solution with Hybrid Memory System"*

8S-4: Mitsuo Ikeda (NTT, Japan) *"H.265/HEVC Encoder for UHDTV"*

8A: Exploring Better Architecture of Your Systems

Chairs: Rainer Doemer (Univ. of California, Irvine, U.S.A.), Hoeseok Yang (Ajou Univ., Republic of Korea)

8A-1: Hongwei Wang (Univ. of Chinese Academy of Sciences, China), Ziyuan Zhu, Jinglin Shi, Yongtao Su (Chinese Academy of Sciences, China) *"Accurate and Efficient ACOSSO Regression Modeling for Processor Architecture Design Space Exploration"*

8A-2: Josef Schneider, Jorgen Peddersen, Sri Parameswaran (Univ. of New South Wales, Australia) *"Speeding Up Single Pass Simulation of PLRUt Caches"*

8A-3: Xi Zhang, Haris Javaid (Univ. of New South Wales, Australia), Muhammad Shafique (Karlsruhe Inst. of Tech., Germany), Jude Angelo Ambrose (Univ. of New South Wales, Australia), Jörg Henkel (Karlsruhe Inst. of Tech., Germany), Sri Parameswaran (Univ. of New South Wales, Australia) *"ADAPT: An ADAptive Manycore Methodology for Software Pipelined ApplicaTions"*

8A-4: Anastasiia Butko, Rafael Garibotti, Luciano Ost, Vianney Lapotre, Abdoulaye Gamatie, Gilles Sassatelli (LIRMM/CNRS/Univ. of Montpellier II, France), Chris Adeniyi-Jones (ARM, U.K.) *"A Trace-Driven Approach for Fast and Accurate Simulation of Manycore Architectures"*

8B: Circuit-Level Modeling and Simulation

Chairs: Luca Daniel (Massachusetts Inst. of Tech., U.S.A.), Takashi Sato (Kyoto Univ.)

8B-1: Mohammed Shemsu Nesro (Masdar Inst. of Tech., United Arab Emirates), Lizhong Sun (Applied Materials, U.S.A.), Ibrahim (Abe) M. Elfadel (Masdar Inst. of Science and Tech., United Arab Emirates) *"Compact Modeling of Microbatteries Using Behavioral Linearization and Model-Order Reduction"*

8B-2: Yan Zhu, Sheldon X.-D. Tan (Univ. of California, Riverside, U.S.A.) *"GPU-Accelerated Parallel Monte Carlo Analysis of Analog Circuits by Hierarchical Graph-Based Solver"*

8B-3: Hyun-Sek Lukas Lee (Leibniz Univ. Hannover, Germany), Matthias Althoff (Tech. Univ. München, Germany), Stefan Hoelldampf, Markus Olbrich, Erich Barke (Leibniz Univ. Hannover, Germany) *"Automated Generation of Hybrid System Models for Reachability Analysis of Nonlinear Analog Circuits"*

8B-4: Shoichi Iizuka, Yuma Higuchi, Masanori Hashimoto, Takao Onoye (Osaka Univ., Japan) *"Area Efficient Device-Parameter Estimation Using Sensitivity-Configurable Ring Oscillator"*

8C: Reliable and Trustworthy Electronics

Chairs: TBD (), Gang Qu (Univ. of Maryland, U.S.A.)

8C-1: Zelong Sun (Chinese Univ. of Hong Kong, Hong Kong), Li Jiang (Shanghai Jiao Tong Univ., China), Qiang Xu (Chinese Univ. of Hong Kong, Hong Kong), Zhaobo Zhang, Zhiyuan Wang, Xinli Gu (Huawei Technologies, U.S.A.) *"On Test Syndrome Merging for Reasoning-Based Board-Level Functional Fault Diagnosis"*

8C-2: Mojtaba Ebrahimi, Razi Seyyedi, Liang Chen, Mehdi Tahoori (Karlsruhe Inst. of Tech., Germany) *"Event-Driven Transient Error Propagation: A Scalable and Accurate Soft Error Rate Estimation Approach"*

8C-3: Shivam Bhasin (Telecom Paristech, France), Daisuke Fujimoto, Makoto Nagata (Kobe Univ., Japan), Jean-Luc Danger (Telecom Paristech, France) *"A Novel Methodology for Testing Hardware Security and Trust Exploiting On-Chip Power Noise Measurement"*

8C-4: Nicole Lesperance, Shrikant Kulkarni, Kwang-Ting Cheng (UC Santa Barbara, U.S.A.) *"Hardware Trojan Detection Using Exhaustive Testing of k-bit Subspaces"*

15:30

Coffee break (15:30 - 15:50)

15:50

17:30

9S: (Designers' Forum) Panel Discussion: IP Base SoC Design and IP Design Innovation

Organizers: Nobuyuki Nishiguchi (Cadence Design Systems, Japan), Moderator: Toshihiro Hattori (Renesas System Design, Japan)

Panelists:

John Koeter (Synopsys, U.S.A.)
Kevin Yee (Cadence, U.S.A.)
Randy Smith (Sonics, U.S.A.)
Neil Parris (ARM, U.K.)

9A: Power/Thermal Management and Modeling

Chairs: Donghwa Shin (Yeungnam Univ., Republic of Korea), Takashi Nakada (Univ. of Tokyo, Japan)

9A-1: Zih-Ci Huang, Chi-Kang Chen, Ren-Song Tsay (National Tsing Hua Univ., Taiwan) *"AROMA: A Highly Accurate Microcomponent-Based Approach for Embedded Processor Power Analysis"*

9A-2: Yu Peng, Shouyi Yin, Leibo Liu, Shaojun Wei (Tsinghua Univ., China) *"Battery-Aware Mapping Optimization of Loop Nests for CGRAs"*

9A-3: Jinho Lee, Junwhan Ahn, Kiyoung Choi (Seoul National Univ., Republic of Korea), Kyungsu Kang (Samsung Electronics, Republic of Korea) *"THOR: Orchestrated Thermal Management of Cores and Networks in 3D Many-Core Architectures"*

9A-4: Jianlei Yang (Tsinghua Univ., China), Liwei Ma, Kang Zhao (Intel, China), Yici Cai (Tsinghua Univ., China), Tin-Fook Ngai (Intel, China) *"Early Stage Real-Time SoC Power Estimation Using RTL Instrumentation"*

9B: (Special Session) System-Level Designs and Tools for Multicore Systems

Organizer: Chung-Ta King (National Tsing Hua Univ., Taiwan)

9B-1: Qiaosha Zou, Matthew Poremba (Penn State Univ., U.S.A.), Rui He, Wei Yang, Junfeng Zhao (Huawei Shannon Lab, China), Yuan Xie (Univ. of California, Santa Barbara, U.S.A.) *"Heterogeneous Architecture Design with Emerging 3D and Non-Volatile Memory Technologies"*

9B-2: Zhehui Wang, Jiang Xu, Peng Yang, Xuan Wang, Zhe Wang, Duong H.K. Luan, Zhifei Wang, Haoran Li, Rafael K.V. Maeda, Xiaowen Wu (Hong Kong Univ. of Science and Tech., Hong Kong), Yaoyao Ye, Qinfen Hao (Huawei Technologies, China) *"Alleviate Chip I/O Pin Constraints for Multicore Processors through Optical Interconnects"*

9B-3: Ting-Shuo Hsu, Jun-Lin Chiu, Chao-Kai Yu, Jing-Jia Liou (National Tsing Hua Univ., Taiwan) *"A Fast and Accurate Network-on-Chip Timing Simulator with a Flit Propagation Model"*

9B-4: Chih-Tsun Huang, Kuan-Chun Tasi, Jun-Shen Lin, Hsiao-Wei Chien (National Tsing Hua Univ., Taiwan) *"Application-Level Embedded Communication Tracer for Many-Core Systems"*

9C: Building Secure Systems

Chairs: Wenjing Rao (Univ. of Illinois, Chicago, U.S.A.), Sandip Ray (Intel, Portland, U.S.A.)

9C-1: Sixing Lu, Minjun Seo, Roman Lysecky (Univ. of Arizona, U.S.A.) *"Timing-Based Anomaly Detection in Embedded Systems"*

9C-2: Carson J Dunbar, Gang Qu (Univ. of Maryland, U.S.A.) *"Satisfiability Don't Care Condition Based Circuit Fingerprinting Techniques"*

9C-3: Soroush Khaleghi, Kai Da Zhao, Wenjing Rao (Univ. of Illinois, Chicago, U.S.A.) *"IC Piracy Prevention via Design Withholding and Entanglement"*

9C-4: Lingxiao Wei, Jie Zhang, Feng Yuan, Yannan Liu (Chinese Univ. of Hong Kong, Hong Kong), Junfeng Fan (Open Security Research, China), Qiang Xu (Chinese Univ. of Hong Kong, Hong Kong) *"Vulnerability Analysis for Crypto Devices against Probing Attack"*

Registration

Conference pre-registration through Web is available. Please visit the Online Registration page:

http://www.aspdac.com/

FEES

Category	By Dec.12,2014	From Dec.13,2014 to Jan.15,2015	On site
[Conference]			
∗Member	53,000 yen	58,000 yen	60,000 yen
Non-member	63,000 yen	68,000 yen	70,000 yen
Full-time Student	33,000 yen	38,000 yen	40,000 yen
[Keynotes + Designers' Forum]			
	23,000 yen	28,000 yen	30,000 yen

∗ **Member of IEEE, ACM SIGDA, IEICE, IPSJ**

Category	By Dec.12,2014	From Dec.13,2014 to Jan.15,2015	On site
[Tutorial]			
∗Member	22,000 yen	26,000 yen	26,000 yen
Non-member	26,000 yen	30,000 yen	30,000 yen
Full-time Student	14,000 yen	16,000 yen	16,000 yen
∗∗Student Group	10,000 yen	12,000 yen	N/A

∗ **Member of IEEE, ACM SIGDA, IEICE, IPSJ**

∗∗ "Student Group" discount is applied to a group of four or more students from the same affiliation (faculty or graduate school). A list of the group members must be submitted. Please check the details in the following registration form.

The conference fee includes:

- Admission to all sessions including keynote speeches and Designers' Forum except tutorials
- A conference kit (a final program and an authority to access the download site*** for the conference proceedings)
  (*** The site will be open on Jan. 19, 2015. Please note that neither CD-ROM nor USB memory are provided.)
- One refreshment per break

The Designers' Forum fee includes:

- Admission to Designers' Forum sessions and keynote speeches
- A conference kit (a final program and an authority to access the download site*** for the conference proceedings)
  (*** The site will be open on Jan. 19, 2015. Please note that neither CD-ROM nor USB memory are provided.)
- One refreshment per break

The tutorial fee includes:

- Admission to tutorials
- Access to electronic files of tutorial presentations
- One lunch coupon
- One refreshment per break

CANCELLATION AND REFUND

When written notification of cancellation is received by the conference secretariat by December 12, 2014, 5,000 yen will be deducted from the fees paid to cover administrative costs. No refunds will be made for cancellation requests received after this date. Speakers are not allowed to cancel registrations.

ON-SITE REGISTRATION HOURS

Monday,	January 19:	8:00 – 18:00
Tuesday,	January 20:	7:00 – 17:00
Wednesday,	January 21:	7:30 – 17:00
Thursday,	January 22:	7:30 – 17:00

Advance Registration Deadline: Dec. 12th, 2014

Information

Proceedings:

ASP-DAC 2015 will be producing an authority to access the download site for the conference proceedings. The site will be open on Jan. 19, 2015. Please note that neither CD-ROM nor USB memory are provided.

Banquet:

Conference registrants are invited to attend a banquet to be held on January 21, 2015. The banquet will be held from 18:00 to 20:00 at the Convention Hall A. Regular Member and Non-member Conference registrants receive a ticket to the banquet when they register at the conference. Full-time students, Designers' Forum-only registrants, and Tutorial-only registrants wishing to attend the banquet will be required to pay 5,000 yen for a ticket when they register on site.

Passport and Visa:

To visit Japan, you must have a valid passport. A visa is required for citizens of countries that do not have visa-exempt agreements with Japan. Please contact the nearest Japanese Embassy or Consulate for visa requirements. The following Web page of Japanese embassy may be helpful.
http://www.mofa.go.jp/j_info/visit/visa/

Duty free import:

Personal effects and professional equipment can be brought into Japan duty free as long as their contents and quantities are deemed reasonable by the customs officer. You can also bring in 400 cigarettes, 500 grams of tobacco or 100 cigars; 3 bottles of alcoholic beverages; 2 ounces of perfume; and gifts and souvenirs whose total market price is less than 200,000 yen or its equivalent. There is no allowance for tobacco or alcoholic beverages for persons aged 19 years or younger. Firearms and other types of weapons, and narcotics are strictly prohibited.

Insurance:

The organizer cannot accept responsibility for accidents that might occur. Delegates are encouraged to purchase travel insurance before leaving their home country. Insurance plans typically cover accidental loss of belongings, medical costs in case of injury or illness, and other possible risks of international travel.

Climate:

Average temperature in winter (Jan.):

	T(F)	T(C)
Sapporo	26.4	-4.1
Sendai	34.7	1.5
Tokyo, Chiba	42.4	5.8
Nagoya	39.7	4.3
Kyoto	38.3	3.5
Osaka	42.4	5.8
Fukuoka	43.5	6.4
Naha	61.9	16.6

Currency Exchange:

Only Japanese yen (JPY, ¥) is acceptable at regular stores and restaurants. Certain foreign currencies may be accepted at a limited number of hotels, restaurants and souvenir shops. You can buy yen at foreign exchange banks and other authorized money exchangers on presentation of your passport.

Travelers checks and credit cards:

Travelers checks are accepted only by leading banks and major hotels in principal cities, and the use of travelers checks in Japan is not as popular as in some other countries. VISA, MasterCard, Diners Club, and American Express are widely accepted at hotels, department stores, shops, restaurants and nightclubs.

Tipping:

In Japan, tips are not necessary anywhere, even at hotels and restaurants.

Electricity:

Electric voltage is uniformly 100 volts, AC, throughout Japan, but with two different cycles: 50 in Eastern Japan*, and 60 in Western Japan**. Leading hotels in major cities have two outlets of 100 and 220 volts but their sockets usually accept a two-leg plug only.

*Eastern Japan :**Tokyo, Chiba**, Yokohama, Tohoku, Hokkaido

**Western Japan :Nagoya, Osaka, Kyoto, Hiroshima, Shikoku, Kyushu

Shopping:

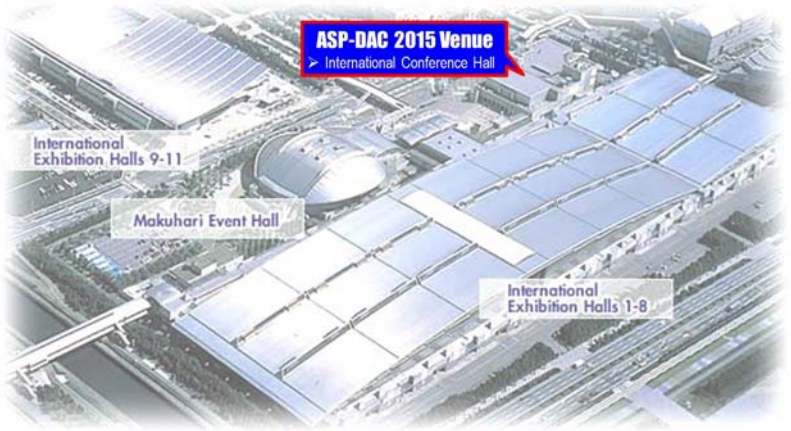
Shops and other sales outlets in Japan are generally open on Saturdays, Sundays and national holidays as well as weekdays from 10:00 to 20:00. Department stores, however, are closed on one weekday, differing by store, and certain specialty shops may not open on Sundays and national holidays.

Other Information:

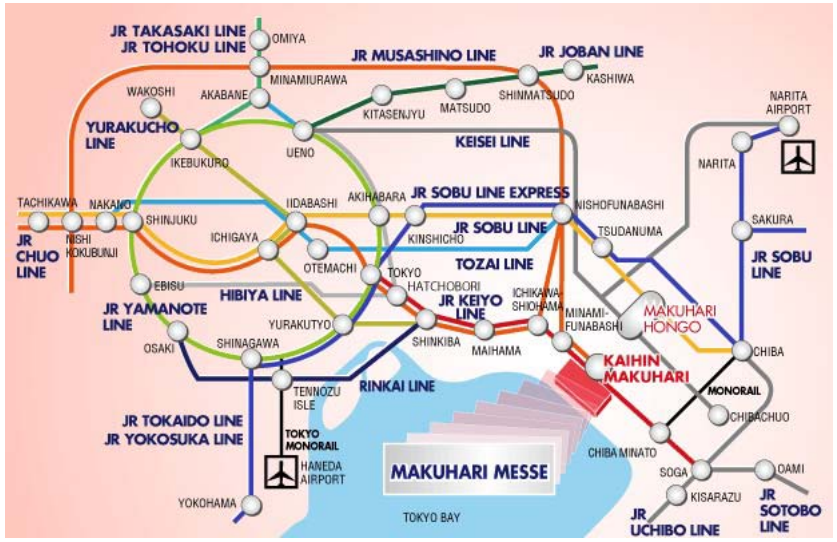
JAPAN NATIONAL TOURISM ORGANIZATION
http://www.jnto.go.jp/
NARITA AIRPORT
http://www.narita-airport.jp/en/
HANEDA AIRPORT
http://www.haneda-airport.jp/en/
YES ! TOKYO
http://tcvb.or.jp/en/
CHIBA, JAPAN TRAVEL GUIDE
http://japan-chiba-guide.com/en/

Access to Makuhari Messe

- ASP-DAC 2015 Conference will take place at “International Conference Hall.”



- It is located in Makuhari Messe International Convention Complex.



Visit our web site
http://www.aspdac.com/

ASP-DAC 2015 SECRETARIAT
Japan Electronics Show Association
5F Ote Center Bldg.,
1-1-3 Otemachi, Chiyoda-ku, Tokyo 100-0004 Japan
Phone: +81-3-6212-5231 Fax: +81-3-6212-5225
E-mail: aspdac2015-sec@mls.aspdac.com