ASP-DAC 2015

20th Asia and South Pacific Design Automation Conference

FINAL PROGRAM

Date: January 19-22, 2015
Place: Makuhari Messe
Chiba/Tokyo, Japan

Sponsored by

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ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE

http://www.aspdac.com/

ASP-DAC 2015

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Wednesday, January 21, 2015, 9:00-9:50

Atsushi Takahara **(Director of NTT Network Innovation Laboratories)** *"Programmable Network"*

Keynote III

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Noriko Arai **(Professor of Information and Society Research Division, National Institute of Informatics)** *"When and how will an AI be smart enough to design?"*

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Tutorials

ASP-DAC 2015 offers attendees a set of two-hour intense introductions to specific topics. Each tutorial will be presented twice a day to allow attendees to cover multiple topics. If you register for tutorials, you have the option to select three out of the six topics.

Tutorial-1: Ultra-low power ultra-low voltage design techniques in Fully Depleted SOI technologies

Monday, January 19, 2015, 9:30-11:30, 13:00-15:00

Organizer:

Andreia Cathelin (STMicroelectronics)

Speakers:

Giorgio Cesana (STMicroelectronics), Edith Beigné (CEA-Leti), Nobuyuki Sugii (LEAP)

Tutorial-2: Leading-Edge Lithography and TCAD

Monday, January 19, 2015, 9:30-11:30, 13:00-15:00

Organizer:

Shigeki Nojima (Toshiba)

Speakers:

Seiji Nagahara (Tokyo Electron), Tomoyuki Matsuyama (Nikon), Shigyo Naoyuki (Toshiba)

Tutorial-3: Normally-Off Computing: Synergy of New Non-Volatile Memories and Aggressive Power Management

Monday, January 19, 2015, 9:30-11:30, 15:30-17:30

Organizers:

Hiroshi Nakamura (The University of Tokyo), Takashi Nakada (The University of Tokyo)

Speakers:

Takashi Nakada (The University of Tokyo), Shinobu Fujita (Toshiba Corporate R&D Center)

Tutorial-4: Hardware Trust in VLSI Design and Implementations

Monday, January 19, 2015, 9:30-11:30, 15:30-17:30

Organizers:

Kazuo Sakiyama (The University of Electro-Communications), Makoto Nagata (Kobe University)

Speakers:

Patrick Schaumont (Virginia Tech, US), Swarup Bhunia (Case Western Reserve University, US),
Kazuo Sakiyama (The University of Electro-Communications, JP), Makoto Nagata (Kobe University, JP)

Tutorial-5: High-Level Synthesis for FPGAs: From Software to Programmable Hardware

Monday, January 19, 2015, 13:00-15:00, 15:30-17:30

Organizer:

Jason Anderson (University of Toronto)

Speakers:

Jason Anderson (University of Toronto), Ben Carrion Schafer (Hong Kong Polytechnic University)

Tutorial-6: Electronic Design Automation for Nanotechnologies

Monday, January 19, 2015, 13:00-15:00, 15:30-17:30

Organizers:

Pierre-Emmanuel Gaillardon (EPFL), Giovanni De Micheli (EPFL)

Speakers:

Pierre-Emmanuel Gaillardon (EPFL), Luca Amaru (EPFL),
Anupam Chattopadhay (Nanyang Technical University), Subhasish Mitra (Stanford University)

Welcome to ASP-DAC 2015

On behalf of the Organizing Committee, I would like to invite all of the engineers on the LSI design and design automation areas to the 20-th Asia and South Pacific Design Automation Conference (ASP-DAC 2015). ASP-DAC 2015 will be held from January 19th (Mon.) to January 22nd (Thur.), 2015 at Makuhari Messe, Chiba, Japan.

ASP-DAC 2015 is a high-quality and premium conference on Electronic Design Automation (EDA) area like other sister conferences such as Design Automation Conference (DAC), Design, Automation & Test in Europe (DATE), and International Conference on Computer Aided Design (ICCAD). ASP-DAC has been started at 1995 and continuously offers the opportunity to know the recent advanced technologies on LSI design and design automation areas, and to communicate each other for researchers and designers around Asia and South Pacific regions.

The conference site is Makuhari Messe, which is one of the biggest international convention complexes in Japan and a memorable place where the first ASP-DAC was held in 1995. Hundreds of companies are accumulated around the complex, and big events on various industrial fields including semiconductor and electronics are held every year. As Makuhari Messe is close to Tokyo, about 30 minutes by train, you can easily access the venue from Narita or Haneda international airport. Joining the conference and participating in technological discussions, you can also enjoy many attractions in Tokyo area, such as Tokyo Disneyland, the world-highest tower called Tokyo Sky Tree, Akihabara, etc.

ASP-DAC 2015 received 318 submissions from 27 countries all over the world. Based on rigorous and thorough reviews and a full-day face-to-face meeting by the Technical Program Committee, 106 papers have been accepted and 26 technical sessions have been organized. 5 Special Sessions have also been organized based on invited talks by the Technical Program Committee.

We have arranged 3 Keynote speakers at the beginning of each day to know the future directions of this area. The first Keynote speaker Dr. Udo Wolz, Executive Vice President of Bosch, will talk about "The required technologies for Automotive towards 2020." The second Keynote speaker Dr. Atsushi Takahara, Director of NTT Network Innovation Laboratories, will introduce future "Programmable Network" technologies. The third keynote speech will be from Dr. Noriko Arai, Professor of National Institute of Informatics. "When and how will an AI be smart enough to design?" will be discueed in her talk.

The Designers' Forum is a unique program that will share design experience and solutions of actual product designs of the industries. This year's program includes the invited talks on the next generation car electronics and 4K/8K TV technologies, and also includes panel disussions on data-centric computing platform and IP-based SoC design and IP design innovations.

The University Design Contest is also an important annual event of ASP-DAC where more than 20 high-quality designs all including actual silicon proof were selected for presentation at Tuesday, January 20.

Six tutorials have been arranged on Monday, January 19. Each tutorial has 2 hour presentation, and will be held 2 times. Registrants can take any 3 of 6 tutorials with the reduced tutorial fee depending on their interests and can obtain wider perspective on the recent hot topics on FD-SOI, Leading-Edge Lithography and TCAD, Normally-Off Computing, Hardware Trust in VLSI Design and Implementation, High-Level Synthesis for FPGAs, Electric Design Automation for Nanotechnologies.

ASP-DAC 2015 offers you an ideal opportunity to touch the recent technologies and the future directions on the LSI design and design automation areas. You will be able to meet and discuss with a lot of researchers and designers on this area, so please do not miss ASP-DAC 2015. Finally, we would like to express our sincere appreciation to sponsors and supporters.

Kunio Uchiyama
General Chair, ASP-DAC 2015

Message from the Technical Program Committee


Naehyuck Chang


TingTing Hwang


Yasuhiro Takashima

Congratulations on the 20th Anniversary of the Asia and South Pacific Design Automation Conference (ASP-DAC)!

On behalf of the Technical Program Committee of the Asia and South Pacific Design Automation Conference (ASP-DAC) 2015, we would like to welcome all of you to the conference scheduled for January 19 to 22, 2015 at Chiba/Tokyo, Japan. This year ASP-DAC is its 20th Anniversary, and the Technical Program Committee proudly announce the 20th technical program.

The Technical Program Committee put a special effort for the 20th technical program. First, we elaborated on the Call for Papers. We performed major revision in the Subcommittees and formally defined their subtopic categories. The purpose of revision is to help authors select the right Subcommittees for their paper submissions without confusion and minimize paper migrations among Subcommittees after papers are submitted. We migrated Technical Program Committee members instead of the papers while ensuring their expertise so that the submitted papers to be reviewed in the original Subcommittees keeping the review workload balance among Subcommittees. However, some papers have been migrated to avoid competition among topics rather than their technical content qualities. This year technical program is also lined up with the sister conference, Design Automation Conference. We also create a new Subcommittee for Security to accommodate the new initiatives of the future Electronics Design Automation (EDA).

We organize the Technical Program Committee with 104 world-leading experts from 14 countries/regions. This year ASP-DAC received 318 submissions from 27 countries/regions with major contribution from Asia, North America and Europe. All committee members contributed to in-depth and thorough reviews. The review process ensured fairness through a rigorous double-blind review process and resolved all the conflict of interest. This year face-to-face Technical Program Committee meeting was organized as a full two-day program together with the EDA Workshop. The venue of the Technical Program Committee meeting was Daejeon Convention Center in Daejeon, Korea. Among 104 Technical Program Committee members, 94 Technical Program Committee members physically attended, and some members joined via teleconferencing due to their personal emergency. Thanks to the support from the Daejeon Convention Center, this year Technical Program Committee also provided quality supplements for the meeting.

This year paper selection was a real challenge thanks to the quality and highly competitive submissions. This year technical program consists of 106 high-quality papers among 318 submissions that corresponds to a very competitive acceptance rate of 33.3%. The complete conference program consists of the regular papers, invitation of keynote speeches and special sessions, which is compiled into a three-day, four parallel-session program. The regular papers are presented in 26 sessions on tracks A, B, and C. The University LSI Design Contest session is allocated on the first day following the tradition.

The technical sessions begins with a keynote address every morning. We have nine special sessions on Tracks S and B (2S through 9S and 9B), which again consist of invited talks on the state-of-the-art topics and industry provided designers' forums. The topics of invited talks are EDA and methodologies focusing on internet of things, nanometer physical design, applying machine learning in EDA, emerging memory technology, and system-level designs and tools for multicore systems.

Each Subcommittee was eligible to nominate one best paper candidate. The Best Paper Award Committee screened the nominees and finally selected seven best paper candidate papers. These best paper candidates went through a careful evaluation process by the Best Paper Award Committee composed of 18 TPC members. The Best Paper Award Committee finally selected the ASP-DAC 2015 Best Paper Award winner.

The fruitful technical program of the ASP-DAC 2015 was not possible without hard working of the authors and reviewers as well as the Technical Program Committee. We pay special thanks to the authors, reviewers, the Technical Program Committee members, and Technical Program Committee Secretaries for their excellent jobs. Finally, we also would like to thank the members of the Organizing Committee for their extraordinary services.

We hope you join us congratulating the 20th Anniversary of the ASP-DAC, enjoy the ASP-DAC 2015 technical program and exchange your visions for the next decade ASP-DAC and EDA research.

Naehyuck Chang
TPC Chair, ASP-DAC 2015

TingTing Hwang
TPC Vice Chair

Yasuhiro Takashima
TPC Vice Chair

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IEICE ESS (Institute of Electronics, Information and Communication Engineers – Engineering Sciences Society)
http://www.ieice.org/eng/

IPSJ SIGSLDM (Information Processing Society of Japan – SIG System and LSI Design Methodology)
http://www.ipsj.or.jp/english/

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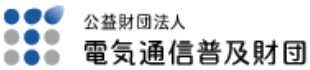
http://www.jeita.or.jp/english/

STARC (Semiconductor Technology Academic Research Center)
http://www.starc.jp/about/profile-e/



The Telecommunications Advancement Foundation
http://www.taf.or.jp/

SCAT (Support Center for Advanced Telecommunications Technology Research, Foundation)
http://www.scat.or.jp/english/

Tateishi Science and Technology Foundation
http://www.tateisi-f.org/

Chiba Prefecture
http://www.pref.chiba.lg.jp/international/

Chiba City
http://www.city.chiba.jp/front/foreign.html

Chiba Convention Bureau and International Center
http://www.ccb.or.jp/e/

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Yi-Yu Liu (Yuan Ze University)

Subcommittees and Subcommittee Chairs (* : Subcommittee Chairs)

[1] System-Level Modeling and Design Methodologies

* **Soonhoi Ha** (Seoul National University, Korea)
Ing-Jer Huang (National Sun Yat-Sen University, Taiwan)
Yosinori Watanebe (Cadence Design Systems, USA)
Hoeseok Yang (Ajou University, Korea)
Makoto Sugihara (Kyushu University, Japan)
Akash Kumar (National University of Singapore, Singapore)
Fan Dongrui (Chinese Academy of Sciences, China)

[2] Embedded System Architectures and Design

* **Tulika Mitra** (National University of Singapore, Singapore)
Hiroyuki Tomiyama (Ritsumeikan University, Japan)
Muhammad Shafique (Karlsruhe Institute of Technology, Germany)
Wei Zhang (Hong Kong University of Science and Technology, Hong Kong)
Guangyu Sun (Peking University, China)
Preeti Ranjan Panda (IIT Delhi, India)
Dongkun Shin (Sungkyunkwan University, Korea)

[3] On-chip Communication and Networks-on-Chips

* **Mehdi Tahoori** (Karlsruhe Institute of technology, Germany)
Jiang XU (Hong Kong University of Science and Technology, Hong Kong)
Romain Lemaire (CEA-LETI, France)
Koushik Chakraborty (Utah State University, USA)
Yoshinori Takeuchi (Osaka University, Japan)
Masoud Daneshtalab (University of Turku, Finland)

[4] System-on-Chip Architectures and Design

* **Sri Parameswaran** (University of New South Wales, Australia)
Paul Bogdon (University of Southern California, USA)
Angelo Ambrose (University of New South Wales, Australia)
Lars Bauer (Karlsruhe Institute of Technology, Germany)

[5] Device/Circuit-Level Modeling, Simulation and Verification

* **Luca Daniel** (Massachusetts Institute of Technology, USA)
Jaijeet Roychowdhury (University of California at Berkeley, USA)
Wenjian Yu (Tsinghua University., China)
Ibrahim (Abe) Elfadel (Masdar University, United Arab Emirates)
Dipanjan Gope (Indian Institute of Science, India)
Roberto Suaya (Univ. Tecn. Nacion. Buenos Aires, Argentina)

[6] Logic/Behavioral/High-Level Synthesis and Optimizations

* **Robert Wille** (University of Bremen, Germany)
Zhiru Zhang (Cornell University, USA)
Anupam Chattopadhyay (RWTH Aachen University, Germany)
Iris Hui-Ru Jiang (National Chiao Tung University, China)
Mineo Kaneko (JAIST, Japan)
Thambipillai Srikanthan (Nanyang Technological University, Singapore)

[7] Analog, RF and Mixed Signals

* **Sheldon Tan** (University of California, Riverside, USA)
Guoyong Shi (Shanghai Jiatong University, China)
Hai Wang (University of Electronic Science and Technology of China, China)
Mark Lin (National Chung Cheng University, Taiwan)
Zuochang Ye (Tsinghua University, China)

[8] System-Level Power and Thermal Management

* **Chia-Lin Yang** (National Taiwan University, Taiwan)
Jae-Joon Kim (Posetech, Korea)
Danella Zhao (University of Louisiana at Lafayette, USA)
Takashi Nakada (University of Tokyo, Japan)
Guihai Yan (ICT , China)
Donghwa Shin (Yeungnam University, Korea)
Yu Wang (Tsinghua University, China)

[9] Device/Circuit/Gate-Level Low Power Design

* **Masanori Hashimoto** (Osaka University, Japan)
Yiyu Shi (Missouri University of Science and Technology, USA)
Bong Hyun Lee (Samsung, Korea)
Kimiyoshi Usami (Shibaura Institute of Technology, Japan)
Bing Li (Technical University of Munich, Germany)

[10] Embedded Software

* **Jason Xue** (City University of Hong Kong, China)
Chengmo Yang (University of Delaware, USA)
Nan Guan (Northeastern University, China)
Qi Zhu (University of California at Riverside, USA)
Zili Shao (Hong Kong Polytechnic University, Hong Kong)
Kyoungwoo Lee (Yonsei University, Korea)
Sidharta Andalam (TUM, Singapore)

[11] Physical Design

* **David Z. Pan** (University of Texas, Austin, USA)
Guojie Luo (Peking University, China)
Tung-Chieh Chen (Synopsys, USA)
Ting-Chi Wang (National Tsing Hua University, Taiwan)
Shigetoshi Nakatake (Univ. of Kitakyushu, Korea)
Yongchan (James) Ban (LG Electronics, Korea)

[12] Timing and Signal/Power Integrity

* **Hao Yu** (Nanyang Technological University, Singapore)
Ray Cheung (City University of Hong Kong, Hong Kong)
Fan Yang (Fudan University, China)
Yungseon Eo (Hanyang University, Korea)

[13] Design for Manufacturability and Reliability

* **Evangeline Young** (Chinese University at Hong Kong, China)
Shigeki Nojima (Toshiba Corporation, Japan)
Jae-seok Yang (Samsung, Korea)
Zhuo Feng (Michigan Technological University, USA)
Xuan Zeng (Fudan University, China)
Martin Wong (University of Illinois at Urbana-Champaign, USA)
Charles Chiang (Synopsys, USA)

[14] Test and Design for Testability

* **Tomokazu Yoneda** (NAIST, Japan)
Kohei Miyase (Kyushu Institute of Technology, Japan)
Chien-Mo Li (National Taiwan University, Taiwan)
Yu Huang (Mentor Graphics, USA)
Sungho Kang (Yonsei University, Korea)

[15] Security and Fault-Tolerant Systems

* **Swarup Bhunia** (Case Western Reserve University, USA)
Patrick Schaumont (Virginia Tech., USA)
Yongdae Kim (KAIST, Korea)
Jongsun Park (Korea University, Korea)
Kenneth Mai (Carnegie Mellon University, USA)

[16] Emerging Technologies

* **Yiran Chen** (University of Pittsburgh, USA)
Weisheng Zhao (Universite Paris-Sud, France)
Danghui Wang (Northwestern Polytechnical University, China)
Jingtong Hu (Oklahoma State University, USA)
Duo Liu (Chongqing University, China)

[17] Emerging Applications I (Bio+nano+3D+quantum)

* **Tsung-Yi Ho** (National Cheng Kung University, Taiwan)
Dajiang Zhou (Waseda University, Japan)
Juinn-Dar Huang (National Chiao Tung University, Taiwan)
Yasushi Sugama (Fujitsu, Japan)

[18] Emerging Applications II (Energy+EV+IoT+Smart grid+ Data center)

* **Tohru Ishihara** (Kyoto University, Japan)
Sehwan (Paul) Kim (Dankook University, Korea)
Ittetsu Taniguchi (Ritsumeikan University, Japan)
Yongpan Liu (Tsinghua University, China)

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Masaitsu Nakajima (Panasonic, Japan)
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University LSI Design Contest

The University LSI Design Contest has been conceived as a unique program at ASP-DAC. The purpose of the contest is to encourage research in LSI design at universities and its realization on a chip by providing opportunities to present and discuss the innovative and state-of-the-art design. The scope of the contest covers circuit techniques for (1) Analog / RF / Mixed-Signal Circuits, (2) Digital Signal Processor, (3) Microprocessors, (4) Custom Application Specific Circuits / Memories, and methodologies for (a) Full-Custom / Cell-Based LSIs, (b) Gate Arrays, (c) Field Programmable Devices.

This year, the University LSI Design Contest Committee received 30 designs from five countries/areas, and selected 23 designs out of them. The selected designs will be disclosed in Session 1S at four-minute presentations, followed by interactive discussions in front of their posters with light meals. To outstanding two designs, The Best Design Award and The Special Feature Award will be presented in the opening session. We sincerely acknowledge the other contributions to the contest, too.

It is our earnest belief to promote and enhance research and education in LSI design in academic organizations. Please come to the University LSI Design Contest and enjoy the stimulating discussions.

Date: Tuesday, January 20, 2015
Place: Makuhari Messe International Convention Complex, International Conference Hall, 1F

Oral Presentation: Room 103 (10:20-12:00)
Poster Presentation: Lobby [Food will be served] (12:20-13:40)

University LSI Design Contest Committee Co-Chairs:

Hiroyuki Ito
(Tokyo Institute of Technology)

Noriyuki Miura
(Kobe University)

Designers' Forum

The Designers' Forum is a unique program that will share design experience and solutions of actual product designs of the industries. This year's program includes the invited talks on the next generation car electronics and 4K/8K TV technologies, and also includes panel discussions on data-centric computing platform and IP-based SoC design and IP design innovations.

Oral Sessions:	(5S) Car Electronics
	(8S) Technology Trend toward 8K Era
Panel Discussions:	(6S) Challenges in the Era of Big-Data Computing
	(9S) IP base SoC design and IP design innovation

Session 5S (13:50-15:30, Jan. 21st)

[Car Electronics]

Three practical design examples of up-to-date automobile developments based on car electronics are described. For designing automobiles accurately and effectively, this session covers vertical integration from systems modeling to verify top level architecture of the automobile system to power devices for fundamental energy conversion.

Session 6S (15:50-17:30, Jan. 21st)

[Challenges in the Era of Big-Data Computing]

The advent of big data era may require a paradigm shift for designing computing systems. The amount of data to be obtained from real world increases exponentially every year, whereas the speed of performance improvements of conventional computing systems is quite slow compared to such rapid grows of big-data applications. So, now it is the time to revisit computer system architecture and its design. The panel discusses the direction of computing platforms in order to satisfy such performance requirements on next generation big-data era.

Session 8S (13:50-15:30, Jan. 22nd)

[Technology Trend toward 8K Era]

From 2014, 4K/UHD CS digital test broadcasting has been already started, and 4K VOD services will be started in 2015 by adopting the latest CODEC standard, H.265/HEVC. Not only 4K, 8K terrestrial test digital broadcasting and 8K terrestrial practical digital broadcasting are planned to be started in 2016 and 2018 respectively. In this session, technology trend toward 8K era will be discussed from various perspective. Four very interesting talks from the key persons of NexTV forum, 8K panel provider, SoC provider and CODEC researcher will be presented.

Session 9S (15:50-17:30, Jan. 22nd)

[IP base SoC design and IP design innovation]

Recent SoC uses a lot of IP's. This session discusses what innovation will happen in the next generation of SoC design with IP's and IP design itself. Four major IP vendors are invited and will talk their views for future design innovation of SoC with their IP's which include numbers and types of IP's such as digital, analog, RF and even a MEMS, variety such as CPU, GPU, memory, bus, interface and so on, usage models in design hierarchy and its modeling and integration methods of those IP's. And also in order to achieve the SoC design innovation they will mention IP itself design methodology including planning, specification, implementation, verification, validation and qualification.

Designers' Forum Co-Chairs:

Yoshio Masubuchi
(Toshiba Corp., Japan)

Koji Inoue
(Kyushu University, Japan)

ACM SIGDA Student Research Forum at ASP-DAC 2015

The Student Research Forum at the ASP-DAC is renovated from a traditional poster session hosted by ACM SIGDA for students to present and discuss their dissertation research with experts in system design and design automation community. Starting from this year, the forum will include both Ph.D. and M.S. students, offering great opportunity for the students to establish contacts for their future career. In addition, the forum helps the companies and academic institutes to get an overview of the latest research and discover the extraordinary candidates for their employment.

Date and Time: 18:00-20:00, January 20, 2015
Location: Room 201 [Food will be served.]

We would like to thank the following committee members for their support and contribution to this forum.

Confirmed committee members:
Yuko Hara-Azumi (Tokyo Institute of Technology)
Tsung-Yi Ho (National Chiao Tung University)
Jingtong Hu (Oklahoma State University)
Yuzi Kanazawa (Fujitsu Laboratories)
Yukihide Kohira (University of Aizu)
Xin Li (Carnegie Mellon University)
Ting Li (Huawei Technologies Co. Ltd.)
Duo Liu (Chongqing University)
Koji Maeda (Hitachi)
Akihiko Miyazaki (NTT)
Shinobu Nagayama (Hiroshima City University)
Yoshinori Okajima (Panasonic)
Qinru Qiu (Syracuse University)
Zili Shao (The Hong Kong Polytechnic University)
Muhammad Shafique (Karlsruhe Institute of Technology)
Yiyu Shi (Missouri University of Science and Technology)
Seiya Shibata (NEC)
Chun-Yao Wang (National Tsing Hua University)
Hai Wang (University of Electronic Science and Technology of China)
Yu Wang (Tsinghua University)
Shu Xu (Huawei Technologies Co. Ltd.)
Chun (Jason) Xue (City University of Hong Kong)
Haibo Zeng (Virginia Polytechnic Institute and State University)
Qi Zhu (University of California, Riverside)

ASP-DAC liaison:
Yukihide Kohira (University of Aizu)

The sponsors of this forum are ACM SIGDA and Huawei Co. Ltd. We would also like to thank ASP-DAC 2015 for supporting this forum.

ACM SIGDA Student Research Forum Chair:

Yiran Chen
(University of Pittsburgh)

ACM SIGDA Student Research Forum Co-Chair:

Yasuhiro Takashima
(University of Kitakyushu)

Best Paper Award

Award Winner

1C-1: **" Quantitative Modeling of Racetrack Memory, A Tradeoff among Area, Performance, and Power"**
Chao Zhang, Guangyu Sun, Weiqi Zhang (CECA, Peking University, China), Fan Mi, Hai Li (University of Pittsburgh, U.S.A.), Weisheng Zhao (Spintronics Interdisciplinary Center, Beihang University, China)

Candidates

2A-1: **"ShuttleNoC: Boosting On-Chip Communication Efficiency by Enabling Localized Power Adaptation"**
Hang Lu (Univ. of Chinese Academy of Sciences, China), Guihai Yan, Yinhe Han, Ying Wang, Xiaowei Li (Chinese Academy of Sciences, China)

3C-3: **"Intra-Vehicle Network Routing Algorithm for Weight and Wireless Transmit Power Minimization"**
Ta-Yang Huang, Chia-Jui Chang (National Cheng Kung Univ., Taiwan), Chung-Wei Lin (Univ. of California, Berkeley, U.S.A.), Sudip Roy (National Cheng Kung Univ., Taiwan), Tsung-Yi Ho (National Chiao Tung Univ., Taiwan)

4A-4: **"A Garbage Collection Aware Stripping Method for Solid-State Drives"**
Min Huang (Harbin Inst. of Tech., China), Yi Wang (Shenzhen Univ., China), Zhaoqing Liu, Liyan Qiao (Harbin Inst. of Tech., China), Zili Shao (Hong Kong Polytechnic Univ., Hong Kong)

4B-2: **"New Electromigration Modeling and Analysis Considering Time-Varying Temperature and Current Densities"**
Hai-Bao Chen, Sheldon X.-D. Tan, Xin Huang (Univ. of California, Riverside, U.S.A.), Valeriy Sukharev (Mentor Graphics, U.S.A.)

5C-1: **"Useful Clock Skew Scheduling Using Adjustable Delay Buffers in Multi-Power Mode Designs"**
Juyeon Kim, Taewhan Kim (Seoul National Univ., Republic of Korea)

8C-1: **"On Test Syndrome Merging for Reasoning-Based Board-Level Functional Fault Diagnosis"**
Zelong Sun (Chinese Univ. of Hong Kong, Hong Kong), Li Jiang (Shanghai Jiao Tong Univ., China), Qiang Xu (Chinese Univ. of Hong Kong, Hong Kong), Zhaobo Zhang, Zhiyuan Wang, Xinli Gu (Huawei Technologies, U.S.A.)

University LSI Design Contest Award

Best Design Award

1S-1: **"An HDL-Synthesized Gated-Edge-Injection PLL with A Current Output DAC"**
Dongsheng Yang, Wei Deng, Tomohiro Ueno, Teerachot Siriburanon, Satoshi Kondo, Kenichi Okada, Akira Matsuzawa (Tokyo Institute of Technology, Japan)

Special Feature Award

1S-23: **"Circuit and Package Design for 44GBs DRAMSoC Interface"**
Akira Okada, Abdul Raziz Junaidi, Yasuhiro Take, Atsutake Kosuge, Tadahiro Kuroda (Keio Univ., Japan)

10-Year Retrospective Most Influential Paper Award

Award Winner

(ASP-DAC 2005)

2A-2: **"Thermal-Driven Multilevel Routing for 3-D ICs"**,
Jason Cong, Yan Zhang (UCLA)

Candidates

1B-1: **"Mapping and Physical Planning of Networks-on-Chip Architectures with Quality-of-Service Guarantees"**
Srinivasan Murali (Stanford University), Luca Benini (University of Bologna), Giovanni De Micheli (Stanford University)

3B-3: **"Speed and Voltage Selection for GALS Systems based on Voltage/Frequency Islands"**
Koushik Niyogi, Diana Marculescu (Carnegie Mellon University)

7B-5s: **"A Fast VLSI Architecture for Full-Search Variable Block Size Motion Estimation in MPEG-4 AVC/H.264"**
Minho Kim, Ingu Hwang, Soo-Ik Chae (Seoul National University)

PIII-3: **"Redundant-via enhanced maze routing for yield improvement"**
Gang Xu (UT Austin), Li-Da Huang (Texas Instruments), David Z. Pan (UT Austin), Martin D. F. Wong (UIUC)

Awards sponsored by ASP-DAC

ASP-DAC Foundation Award

- Dr. Tokinori Kozawa
- Dr. Kenji Yoshida
- Prof. Tatsuo Ohtsuki

ASP-DAC Leadership Award

- General Chairs from 1st ASP-DAC to 20th ASP-DAC

1st (1995) : Prof. Tatsuo Ohtsuki
2nd (1997) : Prof. Isao Shirakawa
3rd (1998) : Dr. Tokinori Kozawa
4th (1999) : Prof. Richard M. M. Chen, Prof. Qian-Ling Zhang
5th (2000) : Dr. Kenji Yoshida
6th (2001) : Prof. Satoshi Goto
7th (2002) : Dr. Sunil D. Sherlekar
8th (2003) : Prof. Hiroto Yasuura
9th (2004) : Prof. Masaharu Imai
10th (2005) : Prof. Ting-Ao Tang
11th (2006) : Dr. Fumiyasu Hirose
12th (2007) : Prof. Hidetoshi Onodera
13th (2008) : Prof. Chong-Min Kyung
14th (2009) : Dr. Kazutoshi Wakabayashi
15th (2010) : Prof. Youn-Long Lin
16th (2011) : Prof. Kunihiro Asada
17th (2012) : Prof. Sri Parameswaran
18th (2013) : Prof. Shinji Kimura
19th (2014) : Prof. Yong Lian, Prof. Yajun Ha
20th (2015) : Dr. Kunio Uchiyama

ASP-DAC Most Frequent Author Award

- Prof. Xianlong Hong

ASP-DAC Frequent Author Award

- Prof. Massoud Pedram
- Prof. Martin D. F. Wong

ASP-DAC Most Frequently Cited Paper Award

- Jingcao Hu, and Radu Marculescu, *"Energy-aware mapping for tile-based NoC architectures under performance constraints,"* ASP-DAC 2003, pp.233-239, 2003.

ASP-DAC Frequently Cited Paper Award

- Kanishka Lahiri, Sujit Dey, Debashis Panigrahi, and Anand Raghunathan, *"Battery-driven system design: a new frontier in low power design,"* ASP-DAC 2002, pp.261-267, 2002.
- Flavius Gruian and Krzysztof Kuchcinski, *"LEneS: task scheduling for low-energy systems using variable supply voltage processors,"* ASP-DAC 2001, pp.449-455, 2001.

ASP-DAC Most Frequently Cited Author Award

- Prof. Jason Cong

ASP-DAC Frequently Cited Author Award

- Prof. Andrew B. Kahng
- Prof. David Z. Pan

Award presented by ACM SIGDA, IEEE CEDA, and Sister Conferences (DAC/DATE/ICCAD)

Distinguished Service Award for ASP-DAC

- Prof. Tatsuo Ohtsuki
- Prof. Hiroto Yasuura
- Prof. Hidetoshi Onodera

Invitation to ASP-DAC 2016

On behalf of the Organizing Committee, it is our great pleasure and honor to welcome you to the 21st ASP-DAC, to be held in Macao, China, February 1-4, 2016. Macao is one of the two special administrative regions of China which lies on the western side of the Pearl River Delta (PRD), bordering Guangdong province in the north and facing the South China Sea in the east and south.

Macau has a rich heritage from both its Chinese and Portuguese past that includes many outstanding examples of western and oriental art and culture. Here you will find Chinese temples, catholic churches; ancient forts and other historical relics within a modern environment that bear testimony to a cultural blend of east and west. The Historic Centre of Macao, which includes twenty-five historic monuments and public squares, was officially listed as a World Heritage Site by UNESCO in 2005. There are also many sightseeing points in Macao such as: Ruins of St. Paul's Church, Macau Tower, A-Ma Temple, Grand Prix Museum, Mandarin's House, etc. Macao has also a notable tourism industry that boasts a wide range of hotels, resorts, stadiums, restaurants and casinos, which probably will bring ASP-DAC 2016 participants a wonderful trip.

Holding ASP-DAC 2016 in Macao will help the local academia and the worldwide academia and semiconductor industry to get closer and exchange electronic design knowledge and experience in Macao and learn from the ASP-DAC community.

We warmly welcome participants from all around the world to meet and exchange our visions in the future design automation and embedded system design related technologies. Your active submissions are highly appreciated in order to contribute for an excellent technical program of ASP-DAC 2016.

Last but not least, we hope to see you all in Macao ASP-DAC 2016 !

Rui P. Martins
General Chair, ASP-DAC 2016

Tutorials

ASP-DAC 2015 offers attendees a set of two-hour intense introductions to specific topics. Each tutorial will be presented twice a day to allow attendees to cover multiple topics. If you register for tutorials, you have the option to select three out of the six topics.

	Monday, January 19			
	Room 102	Room 103	Room 104	Room 105
9:30	**Tutorial-1:** Ultra-low power ultra-low voltage design techniques in Fully Depleted SOI technologies	**Tutorial-2:** Leading-Edge Lithography and TCAD	**Tutorial-3:** Normally-Off Computing: Synergy of New Non-Volatile Memories and Aggressive Power Management	**Tutorial-4:** Hardware Trust in VLSI Design and Implementations
11:30	Lunch Break [coupon]			
13:00	**Tutorial-1:** Ultra-low power ultra-low voltage design techniques in Fully Depleted SOI technologies	**Tutorial-2:** Leading-Edge Lithography and TCAD	**Tutorial-5:** High-Level Synthesis for FPGAs: From Software to Programmable Hardware	**Tutorial-6:** Electronic Design Automation for Nanotechnologies
15:00	Break			
15:30	**Tutorial-3:** Normally-Off Computing: Synergy of New Non-Volatile Memories and Aggressive Power Management	**Tutorial-4:** Hardware Trust in VLSI Design and Implementations	**Tutorial-5:** High-Level Synthesis for FPGAs: From Software to Programmable Hardware	**Tutorial-6:** Electronic Design Automation for Nanotechnologies
17:30				

Tutorial-1 Monday, January 19, 9:30 - 11:30, 13:00 - 15:00@Room 102

Ultra-low power ultra-low voltage design techniques in Fully Depleted SOI technologies

Organizer:
Andreia Cathelin (STMicroelectronics)
Speakers:
Giorgio Cesana (STMicroelectronics), **Edith Beigné** (CEA-Leti), **Nobuyuki Sugii** (LEAP)

Tutorial Outline:

Electronics is more and more pervasive in everyday life: smartphones, connected cars, wearable, Internet of Things... After decades of steady gradual evolution, the semiconductor industry is now facing its biggest and most interesting challenge: while in the last few years the number of mobile devices has significantly grown year after year, the revolution of the Internet of Things promises an exponential growth of connected devices. Semiconductor technology is the key enabler of today applications, making possible the impossible by allowing device miniaturization and co-integration. Traditional planar CMOS technology is mature and low cost, but limited in power consumption efficiency and performances from the 28nm node. These 3 talks tutorial event will bring a highlight in planar thin film fully depleted CMOS technologies that enhance innovative solutions for very energy efficient systems.

The first talk will focus on the UTBB FDSOI technology from STMicroelectronics, presenting the latest technology highlights and mapped on the system design needs for energy efficient logic and also analog/RF designs. The second talk, by CEA-Leti, will get in-deep of complex digital circuit design, focusing on a 32-bit VLIW DSP exhibiting outstanding silicon results in terms of speed and energy. All the design techniques enhancing exceptional energy efficient operation will be carefully detailed.

And finally, the third talk from LEAP will also present ultra-low power system design in the SOTB FDSOI technology. Design techniques will be highlighted in the frame of an energy efficient micro-controller design.

- Theme 1: Planar UTBB FD-SOI technology for highly energy efficient devices
  Giorgio Cesana (STMicroelectronics)
- Theme 2: FDSOI circuit design for a better energy efficiency: Wide operating range and ULP applications
  Edith Beigné (CEA-Leti)
- Theme 3: Ultra low-power system design based on SOTB FDSOI Technology
  Nobuyuki Sugii (LEAP)

Tutorial-2 Monday, January 19, 9:30 - 11:30, 13:00 - 15:00@Room 103

Leading-Edge Lithography and TCAD

Organizer:
Shigeki Nojima (Toshiba)
Speakers:
Seiji Nagahara (Tokyo Electron), **Tomoyuki Matsuyama** (Nikon), **Shigyo Naoyuki** (Toshiba)

Tutorial Outline:

As feature size becomes below the resolution limit of lithography, several complementary techniques of lithography and process have emerged, such as multiple patterning technology and block co-polymer directed self-assembly (DSA). Since these techniques start with ArF immersion lithography, the exposure system is still one of the keys for the fine patterning. For example, overlay error of an exposure system directly causes CD variation on the multiple patterning and pattern shift from the ideal position on DSA. In addition, the shrink of the feature size causes serious statistical process fluctuation, which has influence on device and circuit performance. As virtual manufacturing, TCAD is one of useful tools for robust designs of process, device and circuit.

This tutorial will provide the overview of cutting-edge technologies for ArF immersion exposure system, DSA and TCAD. The topics will cover recent development status, challenges and possible future directions. Furthermore, a design considering manufacturability becomes much important when the new technologies are applied. In this tutorial, design for manufacturability, such as DSA friendly design, will also be discussed.

Tutorial-3 Monday, January 19, 9:30 - 11:30@Room 104, 15:30 - 17:30@Room 102

Normally-Off Computing: Synergy of New Non-Volatile Memories and Aggressive Power Management

Organizers:
Hiroshi Nakamura (The University of Tokyo), **Takashi Nakada** (The University of Tokyo)
Speakers:
Takashi Nakada (The University of Tokyo), **Shinobu Fujita** (Toshiba Corporate R&D Center)

Tutorial Outline:

Normally-off computing is a way of computing where inactive components of computer systems are aggressively powered off with the help of new non-volatile memories (NVMs). Simple power gating cannot fully take the chances of power reduction since volatile memories lose data when power supply is off. With new NVMs, they can maintain their content without power supply. Thereore, a synergetic effect for power gating is highly expected. Hence, this tutorial presents basic design methodologies for normally-off computing, discusses major challenges and approaches in it and introduces key features related to power gating and new generation NVMs. Regarding power gating, granularity of power domain and performance/energy overheads are major concerns. For non-volatile memory, access time and read/write energy are important problems. Essentially, it is important to understand what kind of characteristics affect the performance and energy consumption. There are trade-offs, such as break even time (BET), not only within each technology but also cross-technologies. For example, when the scheduling of a task is changed, the optimal power management may also be different. Thus, to realize normally-off computing, hardware/software co-design and co-optimization are required. This is key for not only system designers, but also hardware engineers and software developers.

Tutorial-4 Monday, January 19, 9:30 - 11:30@Room 105, 15:30 - 17:30@Room 103

Hardware Trust in VLSI Design and Implementations

Organizers:
Kazuo Sakiyama (The University of Electro-Communications), **Makoto Nagata** (Kobe University)
Speakers:
Patrick Schaumont (Virginia Tech, US), **Swarup Bhunia** (Case Western Reserve University, US),
Kazuo Sakiyama (The University of Electro-Communications, JP), **Makoto Nagata** (Kobe University, JP)

Tutorial Outline:

This tutorial provides introductory perspectives of hardware trust in the design and implementation of VLSI systems for security applications. The talks by four experts cover the front-end understandings of threats and countermeasures to the back-end knowledge including counterfeiting, active and passive attacks through side channels of IC chips.

- Talk-1: Threats and Countermeasures from Protocols to Secure Hardware Implementation
  Patrick Schaumont (Virginia Tech, US)
- Talk-2: IC Counterfeiting: Challenges and Solutions (PUFs, Aging Sensors, and Integrity Analysis)
  Swarup Bhunia (Case Western Reserve University, US)
- Talk-3: Fault Analysis for Cryptosystems: Introduction to Differential Fault Analysis and Fault Sensitivity Analysis
  Kazuo Sakiyama (The University of Electro-Communications, JP)
- Talk-4: Side Channel Leakage in Cryptographic Modules: Introduction to Physical Origins and Attack Models
  Makoto Nagata (Kobe University, JP)

Tutorial-5 Monday, January 19, 13:00 - 15:00, 15:30 - 17:30@Room 104

High-Level Synthesis for FPGAs: From Software to Programmable Hardware

Organizer:

Jason Anderson (University of Toronto)

Speakers:

Jason Anderson (University of Toronto), **Ben Carrion Schafer** (Hong Kong Polytechnic University)

Tutorial Outline:

High-level synthesis (HLS) was first proposed in the 1980s, and after spending decades in the shadows of mainstream digital design, there has been tremendous "buzz" around HLS technology in recent years. Indeed, HLS has been gaining traction as a design methodology for field-programmable gate arrays (FPGAs) to improve designer productivity and ultimately, to make FPGA technology accessible to software engineers possessing limited hardware expertise. The hope is that down the road, software developers could use HLS to realize FPGA-based accelerators customized to applications that work in tandem with standard processors to raise computational throughput and energy efficiency. Both of the main FPGA vendors have been investing heavily in HLS in recent years and in this tutorial, we provide a crash course on FPGA HLS, from both the academic research and industrial perspectives. We review the core steps taken by modern HLS tools and the underlying algorithms used inside. We then consider how the style of the high-level language code input to HLS influences the circuit produced and its performance. Special attention will be given to the differences in HLS for FPGAs, custom ASICs, and other IC media, such as coarse-grained arrays. We discuss the typical "knobs" available to an HLS user to enable design-space exploration, for example, to control loop pipelining, resource sharing, and other optimizations. We conclude by discussing current HLS research and mention some of the remaining challenges for HLS that possibly hinder its broader update in the digital design community.

The tutorial will be of interest to be EDA researchers, as well as current and future users of FPGA HLS.

Tutorial-6 Monday, January 19, 13:00 - 15:00, 15:30 - 17:30@Room 105

Electronic Design Automation for Nanotechnologies

Organizers:

Pierre-Emmanuel Gaillardon (EPFL), **Giovanni De Micheli** (EPFL)

Speakers:

Pierre-Emmanuel Gaillardon (EPFL), **Luca Amaru** (EPFL),
Anupam Chattopadhay (Nanyang Technical University), **Subhasish Mitra** (Stanford University)

Tutorial Outline:

Nanoscale emerging technologies hold the promises of drastic improvements of the key design metrics, i.e., area, delay and power consumption, of near-future computing systems. In addition to a pure improvement of the device parameters, many novel technologies exploit unconventional physical phenomena leading to larger computation capabilities at the device level. Such fundamental paradigm change precludes standard CMOS design techniques to fully leverage the performances of advanced devices. In addition to unlocking the logic capabilities of the devices from a logic synthesis perspective, the design methodologies should also consider carefully the manufacturing of the technology, i.e., the physical design, to maximize the fabrication yield.

In this tutorial, we will introduce the importance for tight links between design methodologies and technology to fully exploit emerging devices. The tutorial will cover 3 principal themes: logic optimization and underlying data structures, technology mapping and physical design. To get a direct sense on the importance of design automation for nanotechnologies, each theme will be associated and discussed through a specific technology: controllable-polarity nanowire transistors, quantum gates and carbon nanotubes transistors respectively.

- Theme 1: Logic Optimization - Majority and Biconditional Logic:
  Dr. Pierre-Emmanuel Gaillardon, Mr. Luca Amaru, EPFL, Lausanne, Switzerland
- Theme 2: Technology Mapping - Reversible Logic Synthesis:
  Pr. Anupam Chattopadhay, Nanyang Technical University, Singapore
- Theme 3: Physical Design - Robust System Design at the Nanoscale:
  Pr. Subhasish Mitra, Stanford University, USA

At a glance

Monday, January 19

18:00 – 19:30	**20th Anniversary Reception** (Room 201 [2F])

Tuesday, January 20

	S (Room 103)	A (Room 102)	B (Room 104)	C (Room 105)
8:30 – 9:50	**Opening & Keynote I** (International Conference Room [2F])			
9:50 – 10:20	Coffee Break			
10:20 – 12:00	1S: University Design Contest	1A: NoCS I (Performance and Fault Tolerance)	1B: Toward Power Efficient Design	1C: Modeling and Design Methodologies of Post-silicon Devices
12:00 – 13:50	Lunch Break / **University Design Contest Poster Discussion** (Lobby)			
13:50 – 15:30	2S: **(Special Session)** Internet of Things	2A: NoCS II (Power and Emerging Technology)	2B: Design Automation for Tomorrow's Circuit Technologies	2C: Emerging Applications
15:30 – 15:50	Coffee Break			
15:50 – 17:30	3S: **(Special Session)** New Challenges and Solutions in Nanometer Physical Design	3A: Circuits for Performance and Reliability	3B: Frontiers in Logic Synthesis	3C: Energy Optimization for Electric Vehicles and Smart Grids
17:30 – 18:00	Break			
18:00 – 20:00	ACM SIGDA Student Research Forum at ASP-DAC 2015 (Room 201 [2F])			

Wednesday, January 21

	S (Room 103)	A (Room 102)	B (Room 104)	C (Room 105)
9:00 – 9:50	**Keynote II** (International Conference Room [2F])			
9:50 – 10:15	Coffee Break			
10:15 – 12:20	4S: **(Special Session)** Machine Learning in EDA: Promises and Challenges in Selected Applications	4A: Efficient NVM Management, from Register to Disk	4B: Robust Timing, and P/G Modeling and Design	4C: New Issues in Placement and Routing
12:20 – 13:50	Lunch Break			
13:50 – 15:30	5S: **(Designers' Forum)** Car Electronics	5A: Optimization and Exploration for Caches	5B: CAD for Analog/RF/Mixed-Signal Design	5C: Next-Generation Clock Network Synthesis
15:30 – 15:50	Coffee Break			
15:50 – 17:30	6S: **(Designers' Forum)** Panel Discussion: Challenges in the Era of Big-Data Computing	6A: Optimization Techniques for Non-Volatile Memory based Systems	6B: Test for Higher Quality	6C: Reliability
17:30 – 18:00	Break			
18:00 – 20:00	**Banquet** (Convention Hall A [2F])			

Thursday, January 22

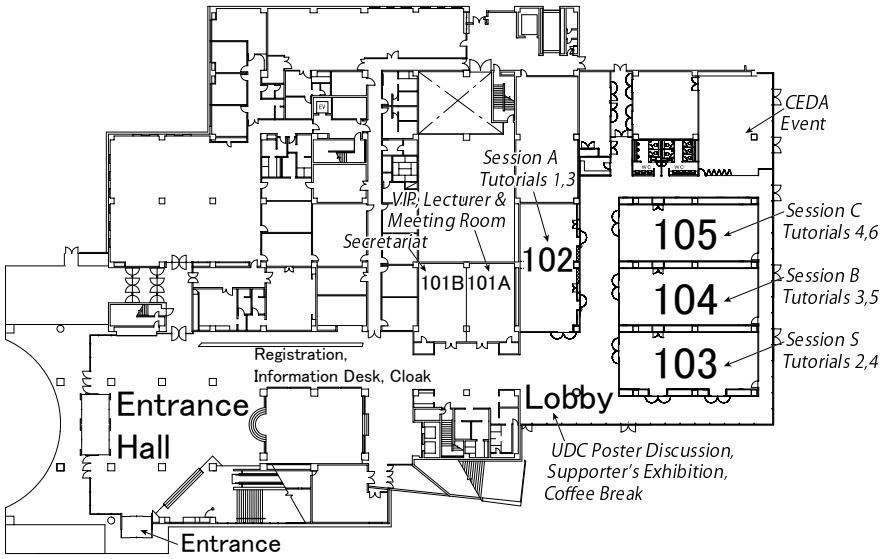
	S (Room 103)	A (Room 102)	B (Room 104)	C (Room 105)
9:00 – 9:50	**Keynote III** (International Conference Room [2F])			
9:50 – 10:15	Coffee Break			
10:15 – 12:20	7S: **(Special Session)** The Future of Emerging ReRAM Technology	7A: Ensuring the Correctness of System Integration	7B: Orchestrating Tasks, Cores, and Communication	7C: Design for Manufacturability
12:20 – 13:50	Lunch Break / IEEE CASS/CEDA Luncheon Presentations			
13:50 – 15:30	8S: **(Designers' Forum)** Technology Trend toward 8K Era	8A: Exploring Better Architecture of Your Systems	8B: Circuit-Level Modeling and Simulation	8C: Reliable and Trustworthy Electronics
15:30 – 15:50	Coffee Break			
15:50 – 17:30	9S: **(Designers' Forum)** Panel Discussion: IP Base SoC Design and IP Design Innovation	9A: Power/Thermal Management and Modeling	9B: **(Special Session)** System-Level Designs and Tools for Multicore Systems	9C: Building Secure Systems

Room Assignment

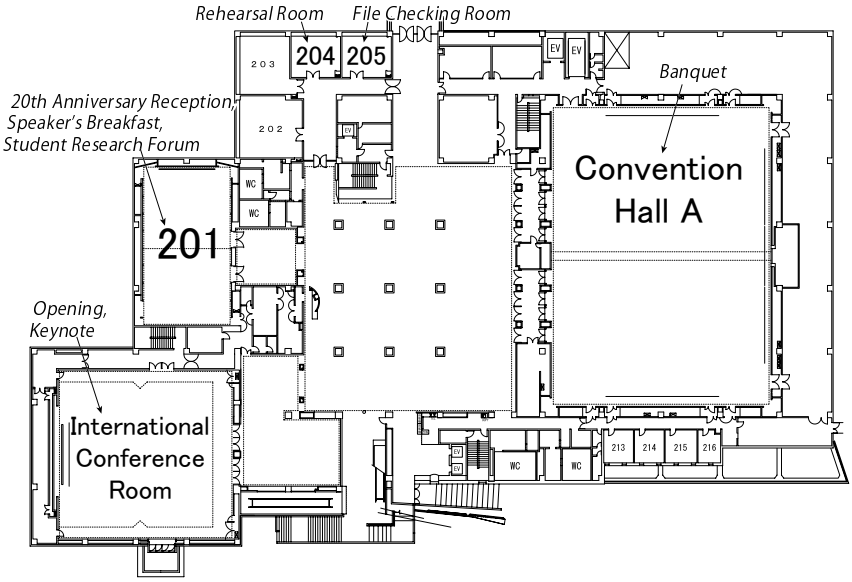
Room Assignment

Location	Event
Entrance Hall (1F)	Registration, Information Desk, and Cloak
International Conference Room (2F)	Opening and Keynote I,II,III
103 (1F)	Session S, Tutorials 2,4, and University Design Contest
102 (1F)	Session A and Tutorials 1,3
104 (1F)	Session B and Tutorials 3,5
105 (1F)	Session C and Tutorials 4,6
Lobby (1F)	Poster Discussion, Supporter's Exhibition, and Coffee Break
Convention Hall A (2F)	Banquet
201 (2F)	20th Anniversary Reception, Speaker's Breakfast, and ACM SIGDA Student Research Forum
204 (2F)	Rehearsal Room
205 (2F)	File Checking Room

International Conference Hall 1F



International Conference Hall 2F



Keynote Addresses

Opening & Keynote I

Tuesday, January 20, 8:30-9:50

"The required technologies for Automotive towards 2020"
Dr. Udo Wolz

Executive Vice President and Director for Engineering and Innovation, Bosch Corporation

This keynote speech deals with the future of the automotive industry and the requirements out of new applications and technologies. The mobility of the future will be electric, automated and connected. Until 2020 the internal combustion engine will still dominate the powertrain with approximately 90% share. This includes systems with mild electrification such as start/stop. For stronger electrified vehicles like hybrids, plug-in hybrids and full EV, battery technologies and battery management are key. Automated driving is already on the way with driver assistance functions and will end up with fully automated driving. Surround sensing of cars and connection between cars and cars to infrastructure will lead to extremely high needs of computing power. Information and Communication Technology is key here. For safety functions extremely short reaction times in milliseconds are necessary. Security mechanisms to ensure proper, unimpaired operation are a must. Seamless communication from home to car and to other parts of life is expected. This leads to smart phone connectivity with the car, car with the cloud, etc.. The car will be part of the Internet. The technologies to achieve this are currently already penetrating from consumer electronics and IT technologies to cars and vice versa. E.g. MEMS, highly reliable micromechanical sensors since long utilized for automotive applications, now entered the market for consumer electronics: Bosch sensors can be found in more than every second Smartphone worldwide. With increasing electrification, automation and connectivity, the requirements and the market demand for VLSI and embedded systems' computing power will increase continuously.

Keynote II

Wednesday, January 21, 9:00-9:50

"Programmable Network"
Dr. Atsushi Takahara

Director of NTT Network Innovation Laboratories

Network Virtualization such as SDN (Software Defined Network) or NFV (Network Functions Virtualization) is the important technology in the new generation network architecture. This provides flexible networking for various kinds of network usage demand. Network virtualization requires the definition of a user specific network called as "slice" and the method for programming a slice design of programmable forwarding nodes in network. The key aspect is to introduce the programmability in network. This can provide new value for users and application providers by working together with computation and peripheral technologies such as cloud computing, Internet of Things, mobile devices and so on. Also, the delivery time of a slice can be shorter than in existing network. "Programmable Network" has huge potential to change the games in creating network service. In this talk, the R&D activities of network virtualization and its programmability methods are introduced to explain how the flexibility is realized as hardware and software system. Then, we discuss how we utilize programmable network for creating network services. The several use cases such as 4K/8K contents distribution, resiliency of network system, and edge distributed computing are introduced to show the possibility of creating new value by Programmable Network. Finally, we discuss the possibility of applying EDA technologies for supporting the design flow of a user specific network in Programmable Network.

Keynote III

Thursday, January 22, 9:00-9:50

“When and how will an AI be smart enough to design?”

Dr. Noriko Arai

Professor of Information and Society Research Division, National Institute of Informatics

The current rise of AI has mainly two origins. The first one is, of course, the invention of machine learning. Statistics and optimization deliver their theories to the machine learning. The combination of the big data and the massively parallel computing enables the machines to ”learn” from the data existing on the web, the network and the database, though there is only small hope that machine learning technologies help the machine to solve the design problem like design automation. Another rather inconspicuous origin is the sophistication of the traditional logical approach. The virtue of the logical approach is in its ability to express complex input-output relations, such as the mapping form natural language text to its meaning and the logical relation between a premise and its consequence, in a way that a human can understand. In this talk, I introduce AI grand challenge, ”Todai Robot Project” (Can an AI get into the University of Tokyo?), initiated by National Institute of Informatics in 2011, and discuss the impact of near-term AI technologies on design automation.

Tuesday, January 20, 2015

1K Opening & Keynote I

Time: 8:30 - 9:50, Tuesday, January 20, 2015
Location: International Conference Room
Chair: Kunio Uchiyama (Hitachi)

1S University Design Contest

Time: 10:20 - 12:10, Tuesday, January 20, 2015
Location: Room 103
Chairs: Hiroyuki Ito (Tokyo Inst. of Tech., Japan), Noriyuki Miura (Kobe Univ., Japan)

Tuesday, January 20, 2015

Tuesday, January 20, 2015

1A NoCS I (Performance and Fault Tolerance)

Time: 10:20 - 12:00, Tuesday, January 20, 2015
Location: Room 102
Chairs: Yoshinori Takeuchi (Osaka Univ., Japan), Takashi Miyamori (Toshiba)

1B Toward Power Efficient Design

Time: 10:20 - 12:00, Tuesday, January 20, 2015
Location: Room 104
Chairs: Kimiyoshi Usami (Shibaura Inst. of Tech., Japan), Masanori Hashimoto (Osaka Univ., Japan)

1C Modeling and Design Methodologies of Post-silicon Devices

Time: 10:20 - 12:00, Tuesday, January 20, 2015
Location: Room 105
Chairs: Zili Shao (Hong Kong Polytechnic Univ., Hong Kong), Duo Liu (Chongqing Univ., China)

Tuesday, January 20, 2015

2S (Special Session) Internet of Things

Time: 13:50 - 15:30, Tuesday, January 20, 2015
Location: Room 103
Chair: Li Shang (Univ. of Colorado Boulder, U.S.A.)

2A NoCS II (Power and Emerging Technology)

Time: 13:50 - 15:30, Tuesday, January 20, 2015
Location: Room 102
Chairs: Mehdi Tahoori (Karlsruhe Inst. of Tech., Germany), Tomoya Horiguchi (Toshiba)

Tuesday, January 20, 2015

2B Design Automation for Tomorrow's Circuit Technologies

Time: 13:50 - 15:30, Tuesday, January 20, 2015
Location: Room 104
Chairs: Anupam Chattopadhyay (RWTH Aachen Univ., Germany), Shigeru Yamashita (Ritsumeikan Univ.)

2C Emerging Applications

Time: 13:50 - 15:30, Tuesday, January 20, 2015
Location: Room 105
Chairs: Juinn-Dar Huang (National Chiao Tung Univ., Taiwan), Youhua Shi (Waseda Univ.)

3S (Special Session) New Challenges and Solutions in Nanometer Physical Design

Time: 15:50 - 17:30, Tuesday, January 20, 2015
Location: Room 103
Chair: Mark Po-Hung Lin (National Chung Cheng Univ., Taiwan)

Tuesday, January 20, 2015

3A Circuits for Performance and Reliability

Time: 15:50 - 16:40, Tuesday, January 20, 2015
Location: Room 102
Chairs: Sri Parameswaran (Univ. of New South Wales, Australia), Chengmo Yang (Univ. of Delaware)

3B Frontiers in Logic Synthesis

Time: 15:50 - 17:30, Tuesday, January 20, 2015
Location: Room 104
Chairs: Robert Wille (Univ. of Bremen, Germany), Yuko Hara-Azumi (Tokyo Inst. of Tech.)

3C Energy Optimization for Electric Vehicles and Smart Grids

Time: 15:50 - 17:30, Tuesday, January 20, 2015
Location: Room 105
Chairs: Hideki Takase (Kyoto Univ., Japan), Yongpan Liu (Tsinghua Univ., China)

Tuesday, January 20, 2015

3C-4 (Time: 17:05 - 17:30)

SRF ACM SIGDA Student Research Forum at ASP-DAC2015

Time: 18:00 - 20:00, Tuesday, January 20, 2015

SRF-1: A Fast Process Variation and Pattern Fidelity Aware Mask Optimization Algorithm
Ahmed Awad (Tokyo Institute of Technology)

SRF-2: Energy Efficient Cache Memories in Deeply-Scaled Technologies
Alireza Shafaei (University of Southern California)

SRF-3: Energy Efficient System Design for Neural Networks
Boxun Li (Tsinghua University)

SRF-4: Analysis and Power Optimization for Probabilistic Boolean Circuits
Ching-Yi Huang (National Tsing Hua University)

SRF-5: Power Consumption Characterization, Modeling and Estimation of Electric Vehicles
Donkyu Baek (KAIST)

SRF-6: A Tuning Method of Programmable Delay Element with an Ordered Finite Set of Delays for Yield Improvement
Hayato Mashiko (University of Aizu)

SRF-7: Reconfigurable PV Powered Full Electric Vehicles
Jaemin Kim (Seoul National University, KAIST)

SRF-8: Feature Localization and Design Understanding for Hardware Designs
Jan Malburg (University of Bremen)

SRF-9: Designing Efficient On-chip Networks: Mapping, Management, and Routing
Jinho Lee (Seoul National University)

SRF-10: Development of A Design Environment for Asynchronous Circuits with Bundled-data Implementation on FPGAs
Keitaro Takizawa (University of Aizu)

SRF-11: Endurance and Energy Aware Optimizations for Phase Change Memory
Mengying Zhao (City University of Hong Kong)

SRF-12: vFlash: Unied Non-Volatile Memory and NAND Flash Memory Architecture in Smartphones
Renhai Chen (Hong Kong Polytechnic University)

SRF-13: Robust Clock Network Synthesis
Rickard Ewetz (Purdue University)

SRF-14: Physical Design Optimization Using Lithography Defect Probability
Seongbo Shim (KAIST)

SRF-15: Contactless Pre-Bond TSV Test and Diagnosis Using Ring Oscillators and Multiple Voltage Levels
Sergej Deutsch (Duke University)

SRF-16: Multi-objective P/G TSV Planning in 3D-ICs
Shengcheng Wang (Karlsruhe Institute of Technology)

SRF-17: Fast Error Rate Estimation with Stochastic Modeling for Adaptive Speed Controlled Circuit
Shoichi Iizuka (Osaka University)

SRF-18: Design and Optimization for Digital Microfluidic Biochips
Trung Anh Dinh (Ritsumeikan University,)

SRF-19: Learning Mechanisms with High Power Efficiency Design
Wan-Yu Wen (National Tsing Hua University)

SRF-20: Demystify Energy Usage in Smartphones
Xiang Chen (University of Pittsburgh)

SRF-21: A High-Efficiency Dual-Channel Photovoltaic Power System for Nonvolatile Sensor Nodes
Xiao Sheng (Tsinghua University)

SRF-22: Understanding Swapping in Mobile Systems
Xiao Zhu (Chongqing University)

SRF-23: A Contact-Imaging Based Microfluidic Cytometer with Machine-Learning for Single-Frame Super-Resolution Processing
Xiwei Huang (Nanyang Technological University)

SRF-24: Model-based Design for Mixed-Criticality Systems
Zaid Al-bayati (McGill University)

Wednesday, January 21, 2015

2K Keynote II

Time: 9:00 - 9:50, Wednesday, January 21, 2015
Location: International Conference Room
Chair: Kunio Uchiyama (Hitachi)

4S (Special Session) Machine Learning in EDA: Promises and Challenges in Selected Applications

Time: 10:15 - 12:20, Wednesday, January 21, 2015
Location: Room 103
Chair: Li-C. Wang (Univ. of California, Santa Barbara, U.S.A.)

4A Efficient NVM Management, from Register to Disk

Time: 10:15 - 12:20, Wednesday, January 21, 2015
Location: Room 102
Chairs: Kyoungwoo Lee (Yonsei Univ., Republic of Korea), Koji Nii (Renesas Electronics)

4B Robust Timing, and P/G Modeling and Design

Time: 10:15 - 12:20, Wednesday, January 21, 2015
Location: Room 104
Chairs: Ray Cheung (City Univ. of Hong Kong, Hong Kong), Fan Yang (Fudan Univ., China)

4C New Issues in Placement and Routing

Time: 10:15 - 12:20, Wednesday, January 21, 2015
Location: Room 105
Chairs: Shigetoshi Nakatake (Univ. of Kitakyushu, Japan), Yuzi Kanazawa (Fujitsu Labs.)

Wednesday, January 21, 2015

5S (Designers' Forum) Car Electronics

Time: 13:50 - 15:30, Wednesday, January 21, 2015
Location: Room 103
Organizer: Shinichi Shibahara (Renesas Electronics, Japan), Chair: Koji Inoue (Kyushu Univ., Japan)

5A Optimization and Exploration for Caches

Time: 13:50 - 15:30, Wednesday, January 21, 2015
Location: Room 102
Chairs: Hiroyuki Tomiyama (Ritsumeikan Univ., Japan), Lin Meng (Ritsumeikan Univ., Japan)

5B CAD for Analog/RF/Mixed-Signal Design

Time: 13:50 - 15:30, Wednesday, January 21, 2015
Location: Room 104
Chairs: Sheldon Tan (Univ. of California, Riverside, U.S.A.), Mark Po-Hung Lin (National Chung Cheng Univ., Taiwan)

5C Next-Generation Clock Network Synthesis

Time: 13:50 - 15:30, Wednesday, January 21, 2015
Location: Room 105
Chairs: Atsushi Takahashi (Tokyo Inst. of Tech.), David Z. Pan (Univ. of Texas, Austin, U.S.A.)

6S (Designers' Forum) Panel Discussion: Challenges in the Era of Big-Data Computing

Time: 15:50 - 17:30, Wednesday, January 21, 2015
Location: Room 103
Organizer: Koji Inoue (Kyushu Univ., Japan), Moderator: Koichiro Yamashita (Fujitsu Labs., Japan)

6A Optimization Techniques for Non-Volatile Memory based Systems

Time: 15:50 - 17:30, Wednesday, January 21, 2015
Location: Room 102
Chairs: Guangyu Sun (Peking Univ., China), Ju Lei (Shandong Univ.)

6B Test for Higher Quality

Time: 15:50 - 17:30, Wednesday, January 21, 2015
Location: Room 104
Chairs: Tomokazu Yoneda (NAIST, Japan), Stefan Holst (Kyushu Inst. of Tech.)

6C Reliability

Time: 15:50 - 17:30, Wednesday, January 21, 2015
Location: Room 105
Chairs: Xuan Zeng (Fudan Univ., China), Martin Wong (UIUC, U.S.A.)

Thursday, January 22, 2015

3K Keynote III

Time: 9:00 - 9:50, Thursday, January 22, 2015
Location: International Conference Room
Chair: Kunio Uchiyama (Hitachi)

7S (Special Session) The Future of Emerging ReRAM Technology

Time: 10:15 - 12:20, Thursday, January 22, 2015
Location: Room 103
Chairs: Guangyu Sun (Peking Univ., China), Yuan Xie (Univ. of California, Santa Barbara, U.S.A.)

7A Ensuring the Correctness of System Integration

Time: 10:15 - 12:20, Thursday, January 22, 2015
Location: Room 102
Chairs: Takeshi Matsumoto (Ishitawa National College of Tech.), Akash Kumar (Natioanl Univ. of Singapore, Singapore)

Thursday, January 22, 2015

7B Orchestrating Tasks, Cores, and Communication

Time: 10:15 - 12:20, Thursday, January 22, 2015
Location: Room 104
Chairs: Zili Shao (Hong Kong Polytechnic Univ., Hong Kong), Masanori Hashimoto (Osaka Univ., Japan)

7C Design for Manufacturability

Time: 10:15 - 12:20, Thursday, January 22, 2015
Location: Room 105
Chairs: Shigeki Nojima (Toshiba, Japan), Eric J.-W. Fang (MediaTek, Taiwan)

Thursday, January 22, 2015

8S (Designers' Forum) Technology Trend toward 8K Era

Time: 13:50 - 15:30, Thursday, January 22, 2015
Location: Room 103
Organizer: Hiroe Iwasaki (NTT, Japan), Chair: Masaitsu Nakajima (Panasonic, Japan)

8A Exploring Better Architecture of Your Systems

Time: 13:50 - 15:30, Thursday, January 22, 2015
Location: Room 102
Chairs: Rainer Doemer (Univ. of California, Irvine, U.S.A.), Hoeseok Yang (Ajou Univ., Republic of Korea)

8B Circuit-Level Modeling and Simulation

Time: 13:50 - 15:30, Thursday, January 22, 2015
Location: Room 104
Chairs: Luca Daniel (Massachusetts Inst. of Tech., U.S.A.), Takashi Sato (Kyoto Univ.)

8C Reliable and Trustworthy Electronics

Time: 13:50 - 15:30, Thursday, January 22, 2015
Location: Room 105
Chairs: Takashi Aikyo (STARC, Japan), Eishi Ibe (Hitachi)

9S (Designers' Forum) Panel Discussion: IP Base SoC Design and IP Design Innovation

Time: 15:50 - 17:30, Thursday, January 22, 2015
Location: Room 103
Organizer: Nobuyuki Nishiguchi (Cadence Design Systems, Japan), Moderator: Toshihiro Hattori (Renesas System Design, Japan)

9A Power/Thermal Management and Modeling

Time: 15:50 - 17:30, Thursday, January 22, 2015
Location: Room 102
Chairs: Donghwa Shin (Yeungnam Univ., Republic of Korea), Takashi Nakada (Univ. of Tokyo, Japan)

Thursday, January 22, 2015

9B (Special Session) System-Level Designs and Tools for Multicore Systems

Time: 15:50 - 17:30, Thursday, January 22, 2015
Location: Room 104
Chair: Chung-Ta King (National Tsing Hua Univ., Taiwan)

9C Building Secure Systems

Time: 15:50 - 17:30, Thursday, January 22, 2015
Location: Room 105
Chairs: Wenjing Rao (Univ. of Illinois, Chicago, U.S.A.), Sandip Ray (Intel, Portland, U.S.A.)

Supporter's Exhibition

Supporter's exhibition is held by three companies which support ASP-DAC 2015 and have exhibition booths. The supporter's exhibition is presented at International Conference Hall 1F Lobby from January 20 through January 22.

Exhibit Hours: **10:00 – 17:30, January 20 / 10:00 – 17:30, January 21 / 10:00 – 16:00, January 22**
Location: **1F Lobby**

cadence® Cadence Design Systems, Japan http://www.cadence.co.jp/	System Design Enablement by Cadence Multi Domain/Language Simulation Platform Cadence Simulation Platform supports wide range of system design domains for automotive, medical, industrial and many more applications. Supported domains: SW/HW co-simulation, mixed digital/analog mixed design, electronics-mechanics coupled simulation, fault injection, thermal/power/noise analysis, etc. Supported languages: C/C++, SystemC, SystemVerilog, VHDL, Verilog, VHDL-AMS, Verilog-AMS and SPICE, etc.
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TOOL TOOL CORPORATION http://www.tool.co.jp/	Showcased is LAVIS-plus that is a full-chip caliber IC design visualization system having electrical characteristics analysis, verification error display, and simple editing capabilities. LAVIS-plus also provides open APIs for facilitating its customization. The API enables you to use general syntax and libraries, so that you can easily create all sorts of scripts ranging from basic ones to advanced ones. Visit our booth and learn more about our EDA solutions.
The Partner for Success ZUKEN ZUKEN Inc. http://www.zuken.co.jp/	Zuken will exhibit at ASP-DAC their next generation EDA solution, CR-8000 Design Force. Design Force enables system-level co-design of the chip, package, and board with a native 3D database, and offers automated features to conduct upfront trade-off studies. Top-down and bottom-up flows can be managed with ease with Design Force by creating any simple or advanced hierarchical system structures to optimize IO connectivity and signal performance. Furthermore, Design Force is a new system developed for the latest hardware, software and 3D graphic technologies, so design teams can innovate with the highest performing and quality software, and reduce the product development time for any technology, including 2.5/3D IC, system-in-package (SiP), and embedding active devices within the substrate.
JEITA JEITA EDA Technical Committee http://www.jeita.or.jp/	JEITA EDA Technical Committee is involved in promoting technologies and international standards related to the Electronic Design Automation (EDA) for designing semiconductor devices, electronic devices and systems, as a part of the activities of JEITA (the Japan Electronics and Information Technology Industries Association). At ASP-DAC2015, we show one of our standardization activities in IEEE, "P2401- Standard Format for LSI-Package-Board Interoperable Design." The general purpose of this standard is to develop a common format that LSI-Package-Board (LPB) design tools can use to exchange information/data seamlessly, as opposed to having to work with multiple different input and output formats. The format provides a common way to specify information/data about the project management, net lists, components, design rules, and geometries used in LSI-Package-Board (LPB) designs. For more information, please visit at http://www.jeita-edatc.com/ and http://standards.ieee.org/develop/project/2401.html .
TOPPAN TOPPAN PRINTING CO., LTD. http://www.toppan.co.jp/	Toppan Technical Design Center Co., Ltd. (TDC) ,as a LSI designing partner for leading semiconductor manufacturers and as a Turnkey partner for electrical, industrial, and medical equipment manufacturers, has been providing a design and a development of LSI for over the past forty years. We provide a variety of LSI designing such as from logic to analog, from circuit to layout, from 28nm to 1um.We also provide Turnkey solutions to our customers with analog/mixed-signal design technology as our core competence. Our turnkey business is the one stop solution. We provide either simple shuttle service or a full service option that ranges from prototyping to production and includes selection of the optimum silicon foundry, support for packaging and testing, process management and quality assurance. Making use of our analog/mixed-signal LSI design know-how, we have had accumulated experience in sensing, data transfer, RF, power management and many other specialized IC applications.
Open Processor Foundation Open Processor Foundation (OPF) http://0pf.org/	Open Processor Foundation (OPF): A public benefit nonprofit organization is dedicated to promote the universal freedom to create, distribute and modify microprocessor design. Clean-Room Design: The first open source CPU core is called "J1 core" together with associated logic. 32/64bit J series processors leverage 20+ year old technologies and cutting edge design tools, process and methodologies. J series users can leverage software tools, OSes and applications accumulated over 20 years.

IEEE CASS/CEDA Luncheon Presentations

IEEE CASS/CEDA Joint Seminar at 20th Anniversary of ASP-DAC

Date and Time: 12:30-13:35, January 22, 2015
Location: General Purpose Room (1F)

Meeting Agenda:

(1) Lecture 1: 12:35-13:05

Title: My Take on ASP-DAC at its 20th Anniversary

Speaker: **David Z. Pan** (The University of Texas at Austin)

(2) Lecture 2: 13:05-13:35

Title: Design for Manufacturability for the Next Decade and Beyond

Speaker: **Yao-Wen Chang** (National Taiwan University)

sponsored by IEEE CASS Japan/Fukuoka/Kansai/Shikoku Chapters, IEEE CEDA All Japan Joint Chapter
No Admission Charge.
Limited Lunch (probably 50 box-lunches) will be served on a first-come-first-serve basis.

Information

Proceedings:

ASP-DAC 2015 will be producing an authority to access the download site for the conference proceedings. The site will be open on Jan. 19, 2015. Please note that neither CD-ROM nor USB memory are provided.

Banquet:

Conference registrants are invited to attend a banquet to be held on January 21, 2015. The banquet will be held from 18:00 to 20:00 at the Convention Hall A. Regular Member and Non-member Conference registrants receive a ticket to the banquet when they register at the conference. Full-time students, Designers' Forum-only registrants, and Tutorial-only registrants wishing to attend the banquet will be required to pay 5,000 yen for a ticket when they register on site.

Climate:

The temperature in Chiba/Tokyo during the period of the Conference ranges between 5°C and 12°C.

Currency Exchange:

Only Japanese yen (JPY, ¥) is acceptable at regular stores and restaurants. Certain foreign currencies may be accepted at a limited number of hotels, restaurants and souvenir shops. You can buy yen at foreign exchange banks and other authorized money exchangers on presentation of your passport.

Travelers checks and credit cards:

Travelers checks are accepted only by leading banks and major hotels in principal cities, and the use of travelers checks in Japan is not as popular as in some other countries. VISA, MasterCard, Diners Club, and American Express are widely accepted at hotels, department stores, shops, restaurants and nightclubs.

Tipping:

In Japan, tips are not necessary anywhere, even at hotels and restaurants.

Electricity:

Electric voltage is uniformly 100 volts, AC, throughout Japan, but with two different cycles: 50 in Eastern Japan*, and 60 in Western Japan**. Leading hotels in major cities have two outlets of 100 and 220 volts but their sockets usually accept a two-leg plug only.

*Eastern Japan :**Tokyo, Chiba**, Yokohama, Tohoku, Hokkaido

**Western Japan :Nagoya, Osaka, Kyoto, Hiroshima, Shikoku, Kyushu

Shopping:

Shops and other sales outlets in Japan are generally open on Saturdays, Sundays and national holidays as well as weekdays from 10:00 to 20:00. Department stores, however, are closed on one weekday, differing by store, and certain specialty shops may not open on Sundays and national holidays.

Other Information:

JAPAN NATIONAL TOURISM ORGANIZATION
http://www.jnto.go.jp/
NARITA AIRPORT
http://www.narita-airport.jp/en/
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http://www.haneda-airport.jp/en/
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http://tcvb.or.jp/en/
CHIBA, JAPAN TRAVEL GUIDE
http://japan-chiba-guide.com/en/

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