An Automatic Place-and-Routed Two-Stage Fractional-*N* Injection-Locked PLL Using Soft Injection

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Synthesizable Analog Circuits

HDL

```
module PLL
(CLK, …, OUT)
…
endmodule
```

Digital design flow

e.g. Encounter, IC Complier, Design Compiler, PrimeTime, Commercial P&R tools…

GDS
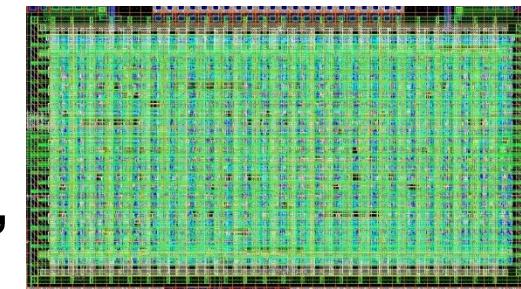
with a standard-cell library
**without any custom-designed cells**
without manual placement

[W. Deng, *et al.*, ISSCC 2014]

Integer-*N* IL-PLL Operation

Reference

e.g. *N*=3+(1/M)

Reference

VCO

Phase Domain (Integer-*N*)

ϕ_{PLL}

$f_{PLL}=N\cdot f_{ref}$

$4N\cdot 2\pi$ — P0

$3N\cdot 2\pi$ — P0

$2N\cdot 2\pi$ — P0

$N\cdot 2\pi$ — P0

P0

t

T_{ref} $2\cdot T_{ref}$ $3\cdot T_{ref}$ $4\cdot T_{ref}$ $5\cdot T_{ref}$
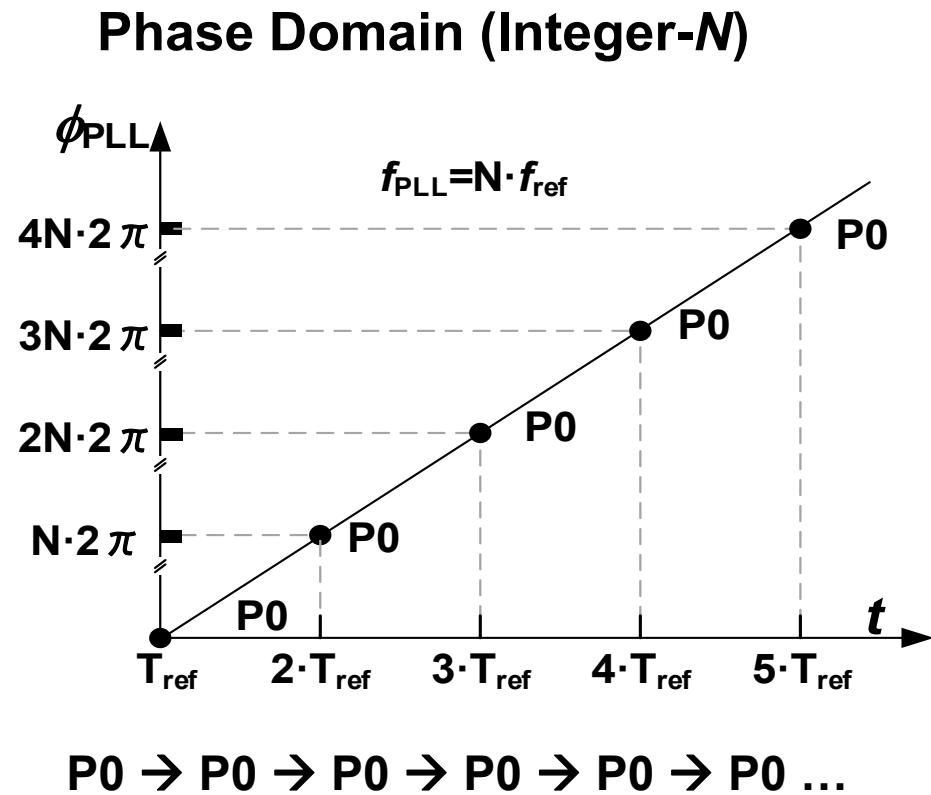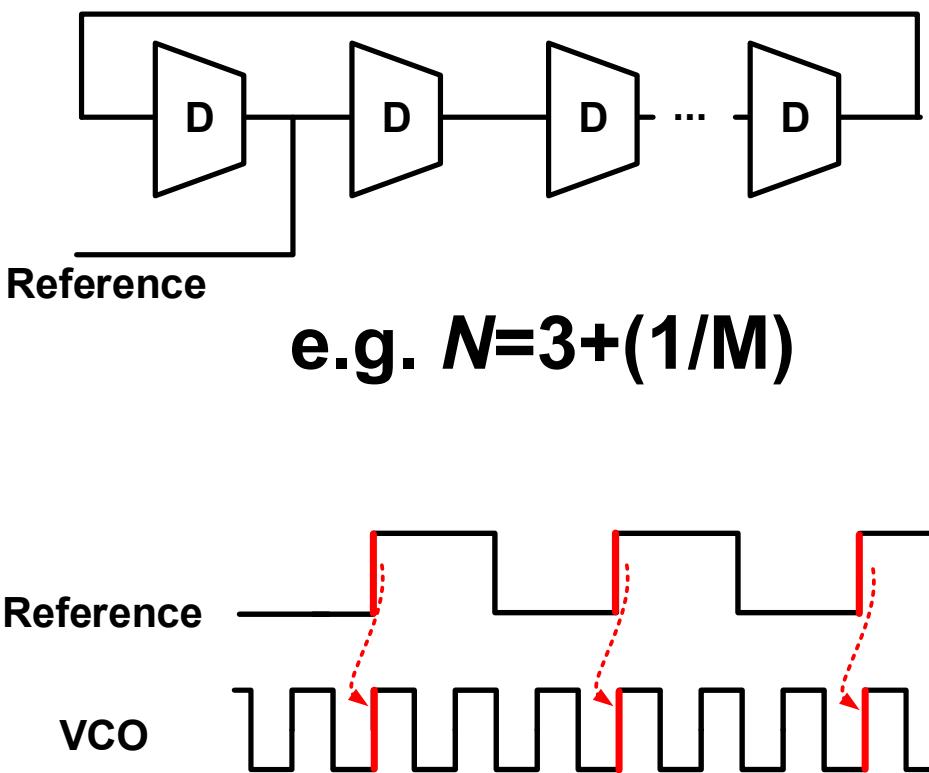
P0 → P0 → P0 → P0 → P0 → P0 …

Sub-Integer-*N* IL-PLL Operation
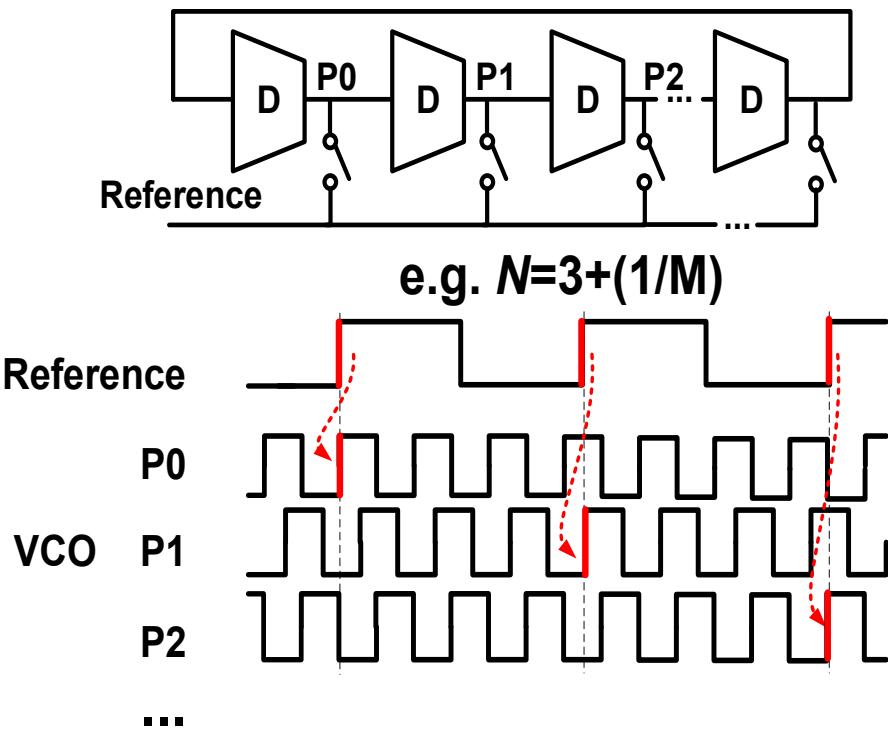
Phase Domain (Sub-Integer-*N*)

e.g. *N*=3+(1/M)

$f_{PLL}=(N+1/M)\cdot f_{ref}$

$4\cdot(N+1/M)\cdot 2\pi$

$3\cdot(N+1/M)\cdot 2\pi$

$2\cdot(N+1/M)\cdot 2\pi$

$(N+1/M)\cdot 2\pi$

P0 → P1 → P2 → P3 → … → P0 → P1 …

[P. Park, *et al.,* ISSCC 2012]
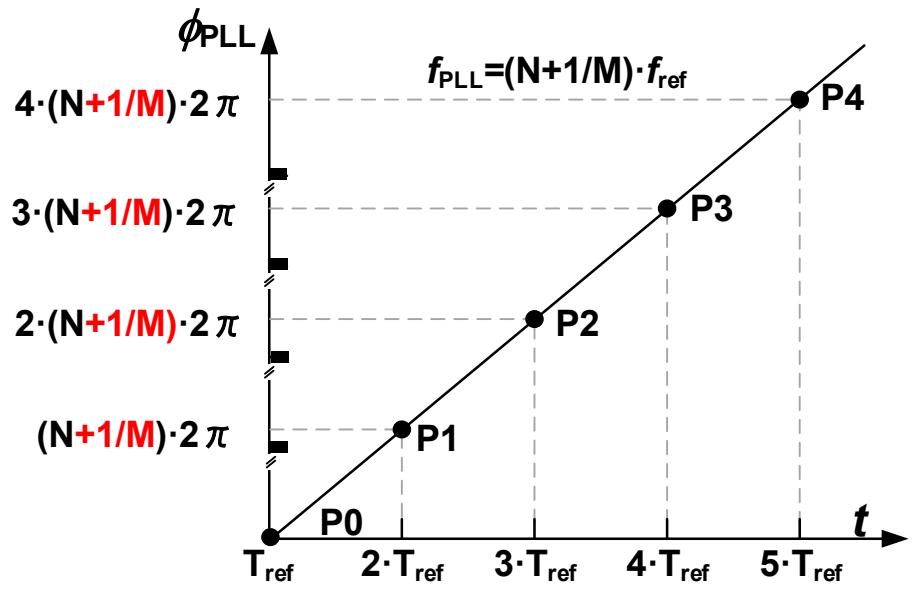
Phase Domain (Fractional-*N*)

$f_{PLL}=(N+0.5/M)\cdot f_{ref}$

ϕ_{PLL}

$(4\cdot N+2/M)\cdot 2\pi$ — P2

$(3\cdot N+1/M)\cdot 2\pi$ — P1

$(2\cdot N+1/M)\cdot 2\pi$ — P1

$N\cdot 2\pi$ — P0

P0

T_{ref} $2\cdot T_{ref}$ $3\cdot T_{ref}$ $4\cdot T_{ref}$ $5\cdot T_{ref}$ t
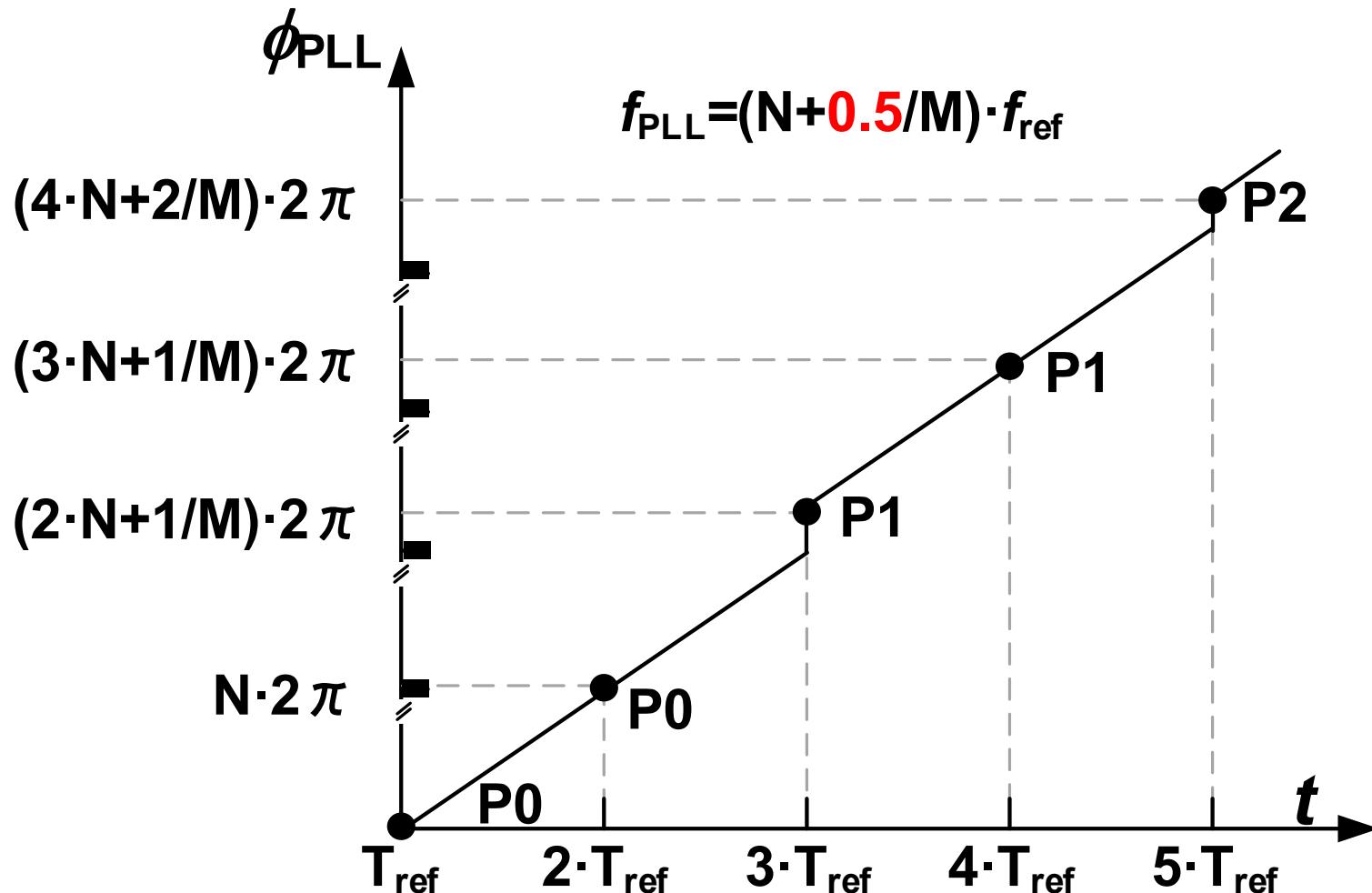
P0 → P0 → P1 → P1 → P2 → P2 → P3 …

Proposed Soft Injection

Proposed Soft Injection

Injection at ϕ_0
(D_{sub}=0, D_{DSM}=0)

Injection at ϕ_8
(D_{sub}=7, D_{DSM}=1)

Reference

ϕ_8 w/o injection

T_{VCO}

ϕ_8 w/ injection

"hard" injection

$\frac{27}{28}T_{VCO}$

Soft injection

ϕ_8 w/ injection1

"soft" injection

ϕ_8 w/ injection2

[W. Deng, *et al.*, ISSCC 2015]
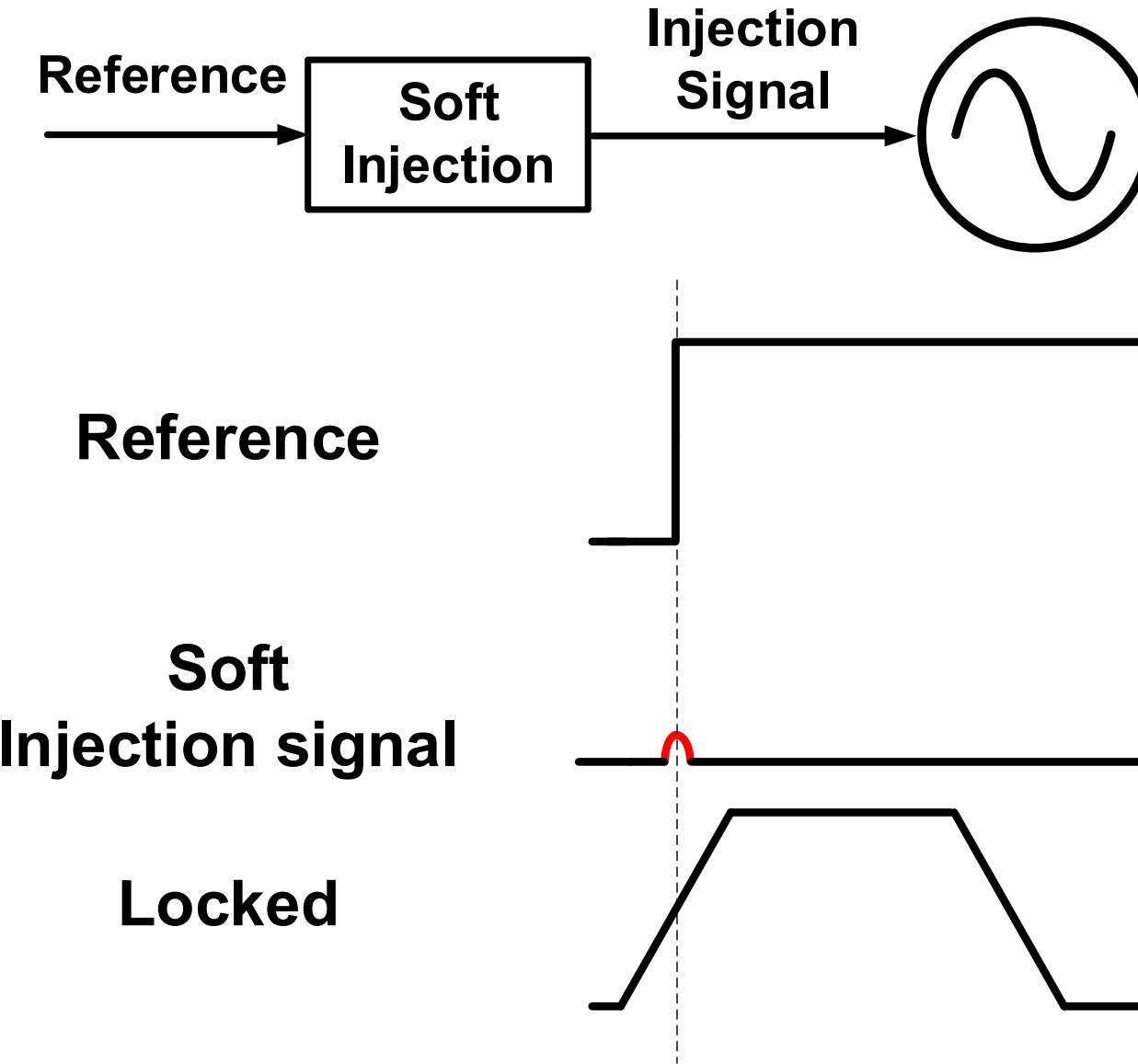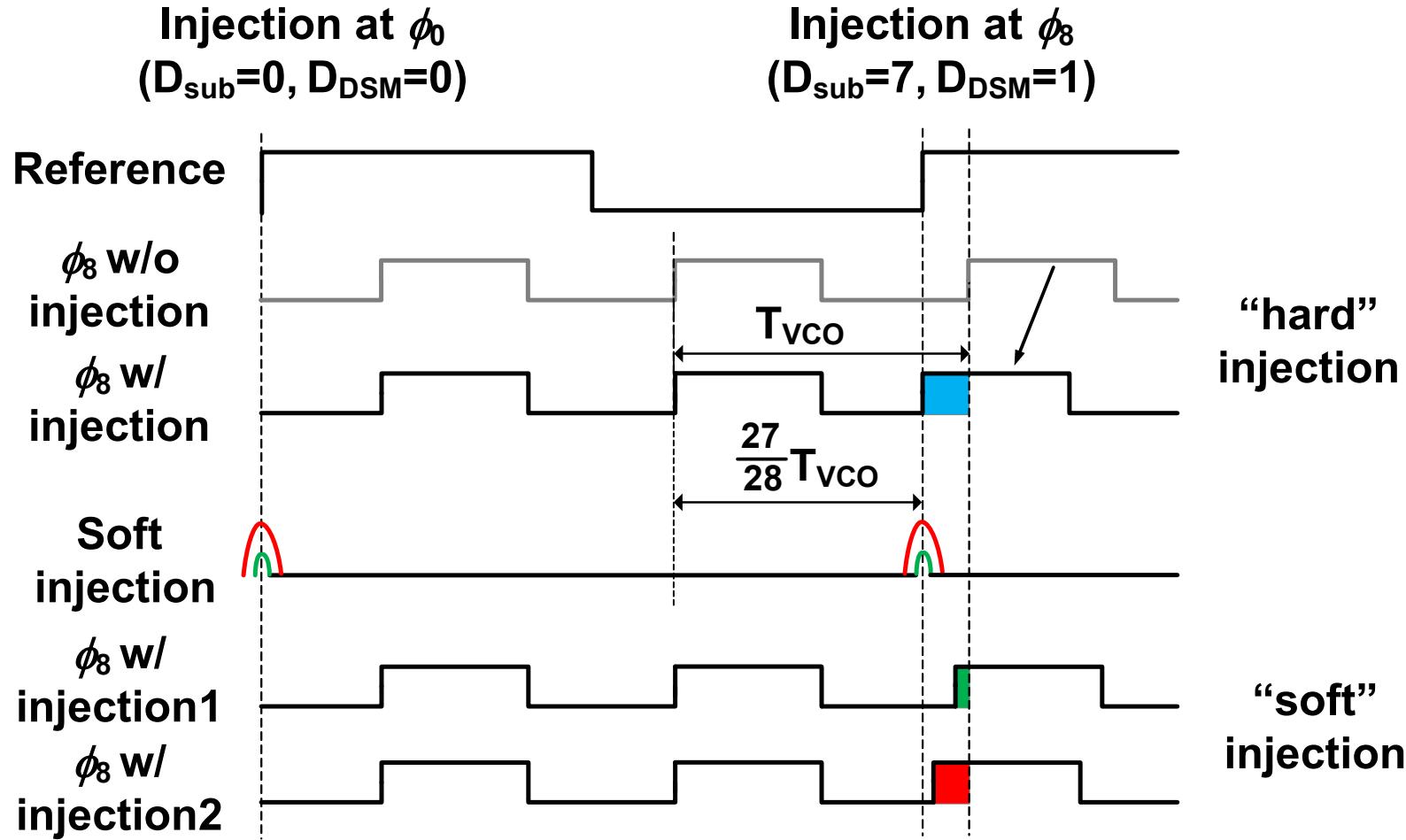
Design Procedure and Chip Microphoto
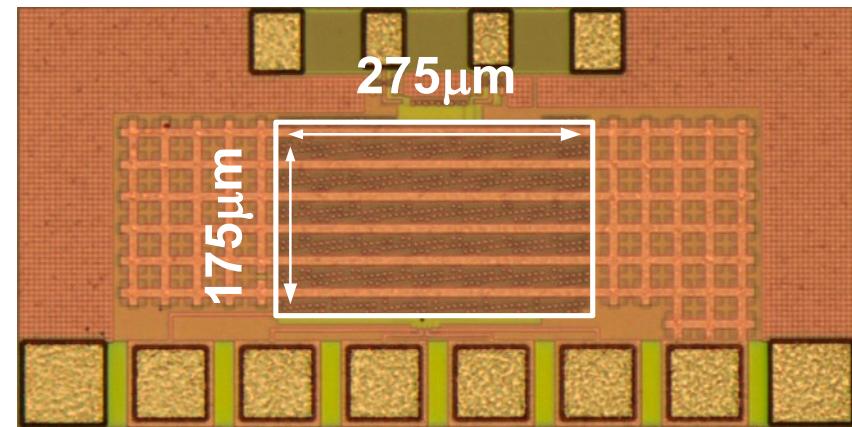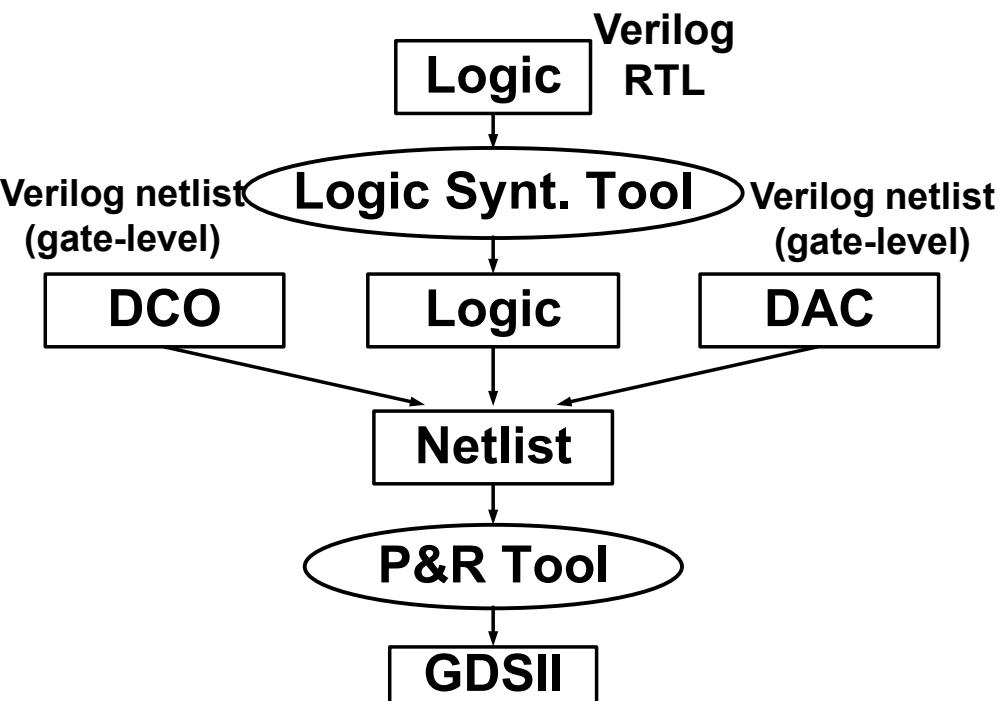
Design Procedure

CMOS 65nm technology

Performance Comparison

	This work	Deng ISSCC2014	Marucci ISSCC2014	Elkholy ISSCC2014
CMOS Tech.	65nm	65nm	65nm	65nm
Power [mW]	3 @1.5222GHz	0.78 @0.9GHz	3 @1.7GHz	10.5 @0.58GHz
Spur [dBc]	**-53**	-47	-51	N/A
FoM [dB]	-224.2	-236.5	-232	-221.9
Type	**Frac-*N***	Int-*N*	Frac-*N*	Frac-*N*
Topology	**Soft Injection**	Injection locking	DTC-based MDLL	Injection locking

*FOM is calculated based on RMS jitter. $FoM=10\log[(\sigma_t/1s)^2(P_{DC}/1mW)]$

Conclusion

- A synthesizable fractional-*N* IL-PLL with a <u>**soft-injection locking**</u> technique is presented.

- The proposed <u>**fractional-N IL-PLL**</u> can <u>**achieve fine resolution, low spur with comparable FoM.**</u>